

OVERVIEW

The CF5012 series are low-current consumption 3rd-harmonic crystal oscillator module ICs. Internal circuit optimization means these devices have reduced current consumption in comparison with our existing 3rd-harmonic oscillator devices. The crystal oscillator circuit has a built-in thin-film feedback resistor with good temperature characteristics and built-in capacitors with excellent frequency response, resulting in a stable 3rd-order overtone oscillator with only the connection of a crystal element.

FEATURES

- 3rd-harmonic oscillation
- 2.7 to 3.6V operating supply voltage range
- 30 to 45MHz recommended operating frequency range
- Inverter amplifier feedback resistor built-in
- Oscillator capacitors C_G , C_D built-in
- Output three-state function (high impedance in standby mode)
- f_O output frequency (oscillator frequency)
- 8mA output drive capability ($V_{DD} = 2.7V$)
- 6.5mA (typ) low current consumption ($V_{DD} = 3V$, $C_L = 15pF$, $f = 40MHz$)
- CMOS output duty level
- Chip form (CF5012xxx)

SERIES CONFIGURATION

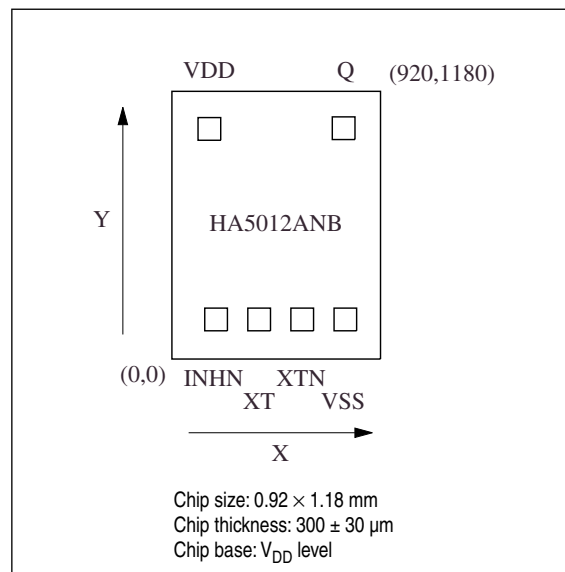
Version	Recommended operating frequency [MHz]	gm ratio	Built-in capacitance [pF]		R_f [k Ω]
			C_G	C_D	
CF5012ANB	30 to 45	1.0	8	15	3.1

Note: Recommended operating frequency is not the guaranteed value but is measured using NPC's standard crystal.

ORDERING INFORMATION

Device	Package
CF5012xxx-1	Chip form

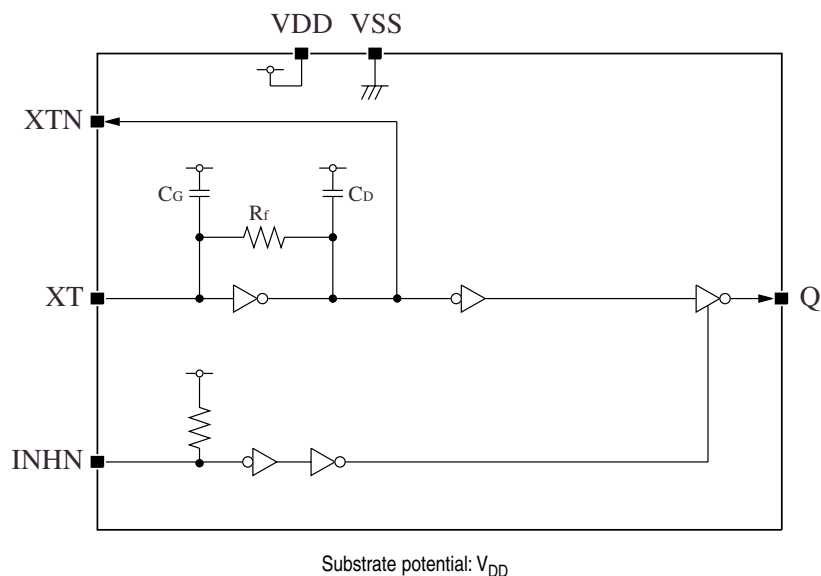
PAD LAYOUT

(Unit: μm)

PIN DESCRIPTION and PAD DIMENSIONS

Name	I/O	Description		Pad dimensions [μm]	
				X	Y
INHN	I	Output state control input. High impedance when LOW. Pull-up resistor built in		195	174.4
XT	I	Amplifier input	Crystal oscillator connection pins. Crystal oscillator connected between XT and XTN	385	174.4
XTN	O	Amplifier output		575	174.4
VSS	–	Ground		765	174.4
Q	O	Output. Output frequency. High impedance in standby mode		757.6	1017.6
VDD	–	Supply voltage		165.4	1014.6

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		−0.5 to +7.0	V
Input voltage range	V_{IN}		−0.5 to $V_{DD} + 0.5$	V
Output voltage range	V_{OUT}		−0.5 to $V_{DD} + 0.5$	V
Operating temperature range	T_{opr}		−40 to +85	°C
Storage temperature range	T_{stg}		−65 to +150	°C
Output current	I_{OUT}		25	mA

Recommended Operating Conditions

$V_{SS} = 0V$, $f \leq 45MHz$, $C_L = 15pF$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.7	–	3.6	V
Input voltage	V_{IN}		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}		−20	–	+80	°C

Electrical Characteristics

$V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+80^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, $V_{DD} = 2.7V$, $I_{OH} = 8mA$	2.2	2.4	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, $V_{DD} = 2.7V$, $I_{OL} = 8mA$	–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, $INHN = LOW$, $V_{DD} = 3.6V$	$V_{OH} = V_{DD}$	–	10	μA
			$V_{OL} = V_{SS}$	–	10	μA
HIGH-level input voltage	V_{IH}	$INHN$	$0.7V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	$INHN$	–	–	$0.3V_{DD}$	V
Current consumption	I_{DD}	Measurement cct 3, load cct 1, $INHN = open$, $C_L = 15pF$, $f = 40MHz$	–	6.5	13	mA
$INHN$ pull-up resistance	R_{UP}	Measurement cct 4	40	100	250	$k\Omega$
Feedback resistance	R_f	Measurement cct 5	2.63	3.1	3.57	$k\Omega$
Built-in capacitance	C_G	Design value, determined by the internal wafer pattern	7	8	9	pF
	C_D		13	15	17	pF

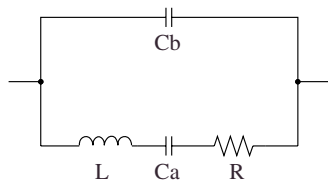
Switching Characteristics

$V_{DD} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+80^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_r	Measurement cct 3, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$, $C_L = 15pF$	–	2.0	4.0	ns
Output fall time	t_f	Measurement cct 3, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$, $C_L = 15pF$	–	2.0	4.0	ns
Output duty cycle ¹	Duty	Measurement cct 3, load cct 1, $T_a = 25^{\circ}C$, $V_{DD} = 3.0V$, $C_L = 15pF$, $f = 40MHz$	40	–	60	%
Output disable delay time	t_{PLZ}	Measurement cct 3, load cct 1, $T_a = 25^{\circ}C$, $V_{DD} = 3.0V$, $C_L = 15pF$	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. Monitored in sample lots.

Current consumption and Output waveform with NPC's standard crystal



f (MHz)	R (Ω)	L (mH)	Ca (fF)	Cb (pF)
40	20.53	11.34	1.396	3.989

FUNCTIONAL DESCRIPTION

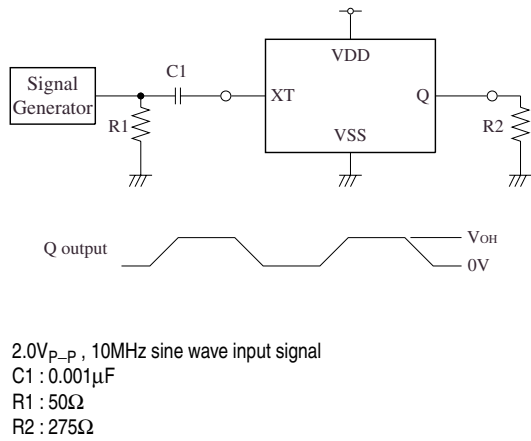
Standby Function

When INHN goes LOW, the oscillator output on Q goes high impedance.

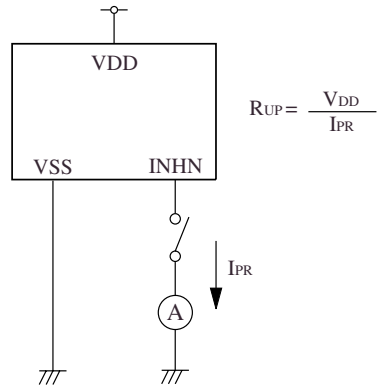
INHN	Q	Oscillator
HIGH (or open)	f_O output frequency	Normal operation
LOW	High impedance	Normal operation

MEASUREMENT CIRCUITS

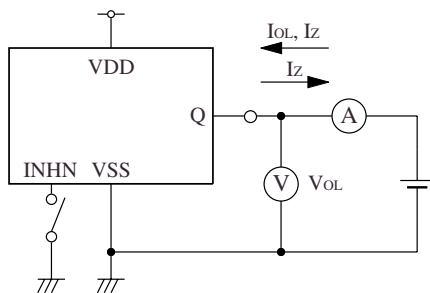
Measurement cct 1



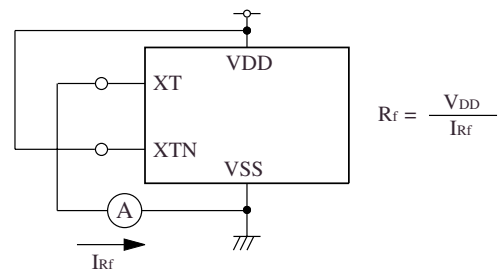
Measurement cct 4



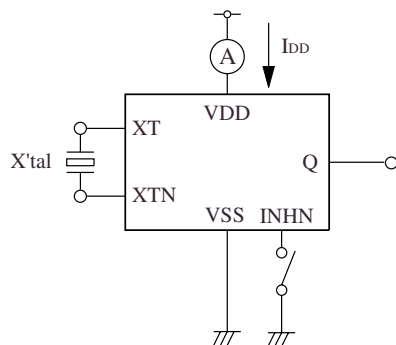
Measurement cct 2



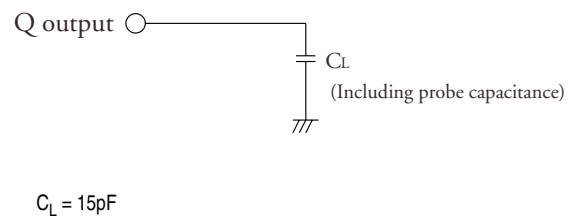
Measurement cct 5



Measurement cct 3

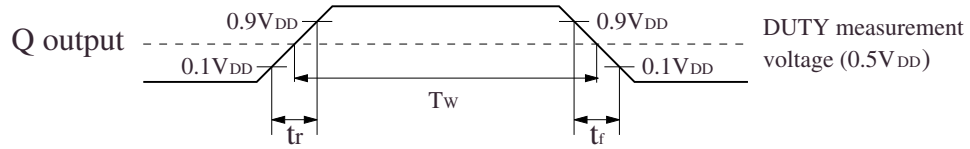


Load cct 1

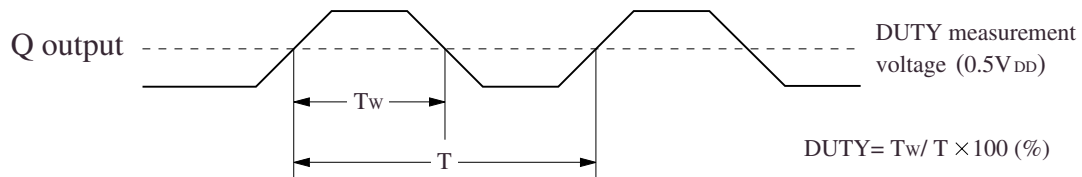


Switching Time Measurement Waveform

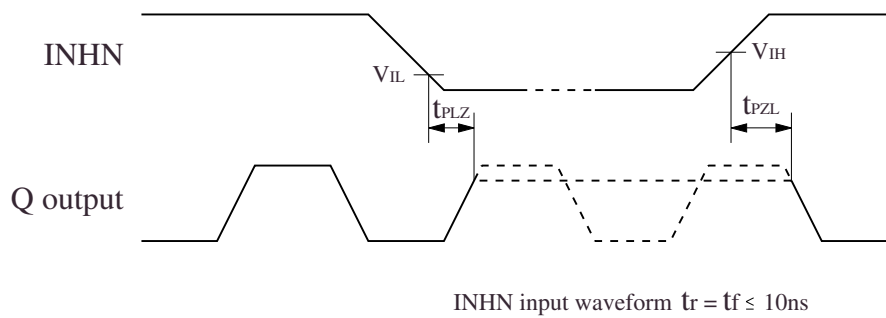
T_r , T_f , Duty



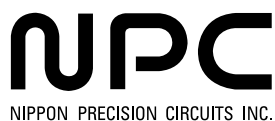
Output duty cycle



Output Enable/Disable Delay



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NC0111AE 2002.01