

## OVERVIEW

The SM5021 series are crystal oscillator module ICs fabricated in NPC's Molybdenum-gate CMOS, that incorporate high-frequency, low current consumption oscillator and output buffer circuits. Highly

accurate thin-film feedback resistors and high-frequency capacitors are built-in, eliminating the need for external components to make a stable 3rd-harmonic oscillator.

## FEATURES

- 3rd overtone oscillation
- Capacitors CG, CD built-in
- Inverter amplifier feedback resistor built-in (A×, B× series)
- TTL input level
- 4 mA ( $V_{DD} = 2.7$  V) drive capability  
8 mA ( $V_{DD} = 4.5$  V) drive capability
- Output three-state function
- 2.7 to 5.5 V supply voltage (A×, K× series)  
4.5 to 5.5 V supply voltage (B×, L× series)
- Oscillator frequency output
- 6-pin SOT (SM5021××H)
- Chip form (CF5021××)

## SERIES CONFIGURATION

Version <sup>1</sup>	Supply voltage		Recommended operating frequency range (MHz)		Built-in capacitance (pF)		gm ratio	Rf (kΩ)	Output frequency	Output level	Standby output state
	Chip	SOT	3V	5V	C <sub>G</sub>	C <sub>D</sub>					
SM5021AAH	4.5 to 5.5	4.5 to 5.5	×	22 to 30	8	15	1	6.0	f <sub>o</sub>	CMOS	High impedance
SM5021ABH	2.7 to 5.5	2.7 to 5.5	22 to 30	30 to 43	8	15	1	3.3	f <sub>o</sub>	CMOS	High impedance
SM5021ACH	2.7 to 5.5	2.7 to 5.5	30 to 40	43 to 55	8	15	2	3.9	f <sub>o</sub>	CMOS	High impedance
SM5021ADH	2.7 to 5.5	2.7 to 5.5	40 to 50	55 to 70	8	15	3	2.7	f <sub>o</sub>	CMOS	High impedance
SM5021AEH	2.7 to 3.6	×	50 to 70	×	8	12	4	2.7	f <sub>o</sub>	CMOS	High impedance
SM5021BAH	4.5 to 5.5	4.5 to 5.5	×	22 to 30	8	15	1	6.0	f <sub>o</sub>	TTL	High impedance
SM5021BBH	4.5 to 5.5	4.5 to 5.5	×	30 to 43	8	15	1	3.3	f <sub>o</sub>	TTL	High impedance
SM5021BCH	4.5 to 5.5	4.5 to 5.5	×	43 to 55	8	15	2	3.9	f <sub>o</sub>	TTL	High impedance
SM5021BDH	4.5 to 5.5	4.5 to 5.5	×	55 to 70	8	15	3	2.7	f <sub>o</sub>	TTL	High impedance
SM5021KDH	2.7 to 5.5	2.7 to 5.5	22 to 50	22 to 70	8	15	3	—	f <sub>o</sub>	CMOS	High impedance
SM5021KEH	2.7 to 3.6	2.7 to 3.6	50 to 70	×	8	12	4	—	f <sub>o</sub>	CMOS	High impedance
SM5021LDH	4.5 to 5.5	4.5 to 5.5	×	22 to 70	8	15	3	—	f <sub>o</sub>	TTL	High impedance

1. Chip form devices have designation CF5021××.

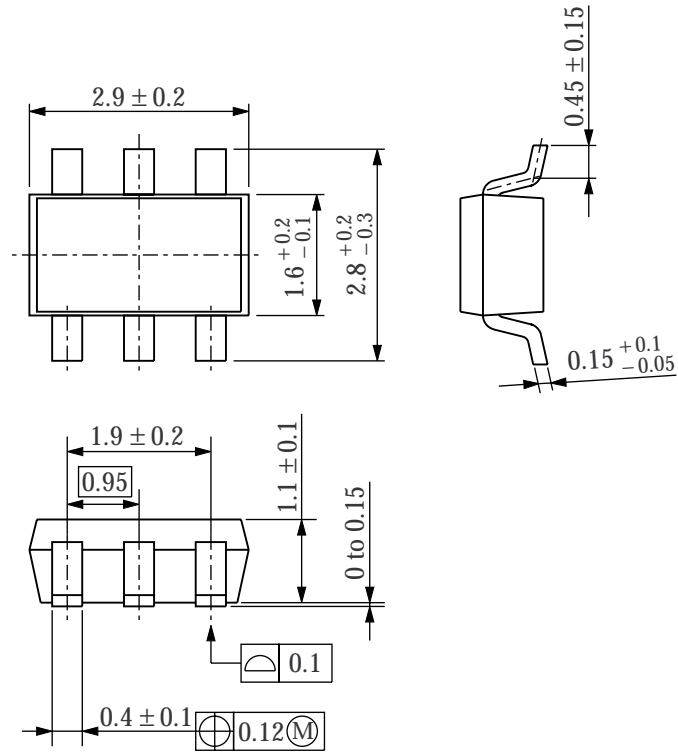
## ORDERING INFORMATION

Devicez	Package
SM5021××H	6-pin SOT
CF5021××-2	Chip form

## PACKAGE DIMENSIONS

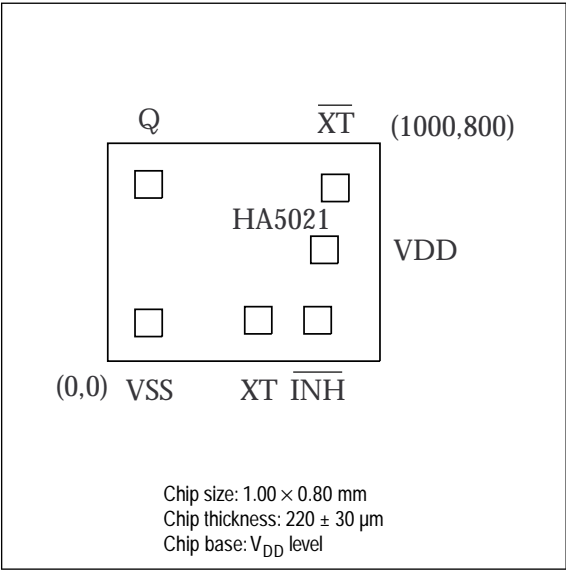
(UNIT : mm)

- 6-pin SOT



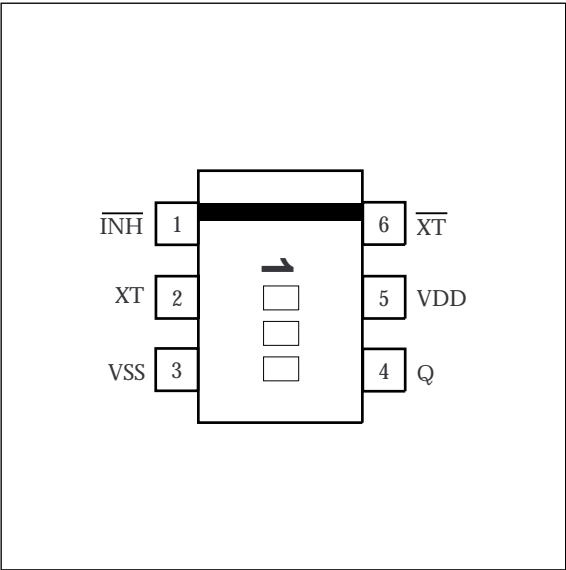
PAD LAYOUT

(Unit :  $\mu\text{m}$ )



PINOUT

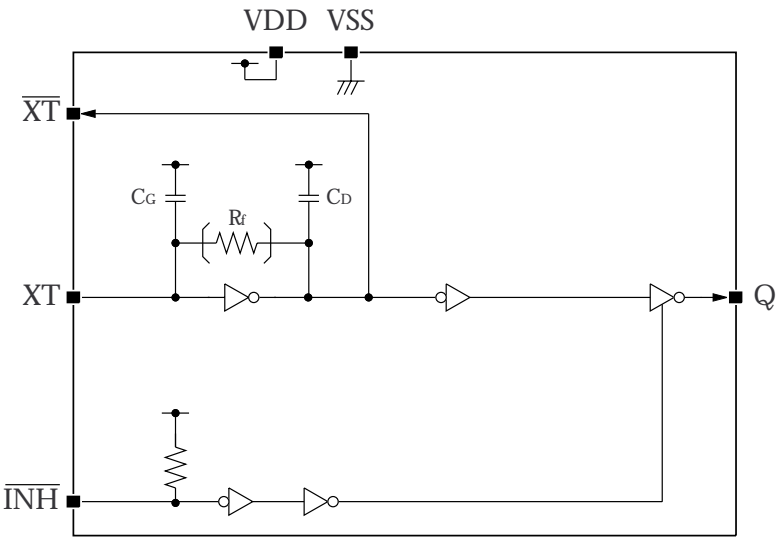
(Top View)



PIN DESCRIPTION and PAD DIMENSIONS

Number	Name	I/O	Description	Pad dimensions [ $\mu\text{m}$ ]	
				X	Y
1	INH	I	Output state control input. High impedance when LOW. Pull-up resistor built in	771	150
2	XT	I	Amplifier input. Crystal oscillator connection pins. Crystal oscillator connected between XT and XT	553	150
3	VSS	-	Ground	150	140
4	Q	O	Output. Output frequency ( $f_o$ )	150	649
5	VDD	-	Supply voltage	796	409
6	XT	O	Amplifier output. Crystal oscillator connection pins. Crystal oscillator connected between XT and XT	836	636

BLOCK DIAGRAM



## SPECIFICATIONS

### Absolute Maximum Ratings

$$V_{SS} = 0 \text{ V}$$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	$V_{DD}$		−0.5 to 7.0	V
Input voltage range	$V_{IN}$		−0.5 to $V_{DD} + 0.5$	V
Output voltage range	$V_{OUT}$		−0.5 to $V_{DD} + 0.5$	V
Operating temperature range	$T_{opr}$		−40 to 85	°C
Storage temperature range	$T_{stg}$	Chip form	−65 to 150	°C
		6-pin SOT	−55 to 125	
Output current	$I_{OUT}$		13	mA
Power dissipation	$P_D$	6-pin SOT	250	mW

### Recommended Operating Conditions

$$V_{SS} = 0 \text{ V}, f \leq 70\text{MHz}, C_L \leq 15\text{pF}$$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		2.7	–	5.5	V
Input voltage	$V_{IN}$		$V_{SS}$	–	$V_{DD}$	V
Operating temperature	$T_{OPR}$		−20	–	80	°C

Note: Recommended operating conditions will change in accordance with operating frequency, load capacitance, or power dissipation.

## Electrical Characteristics

3 V operation: AA, AB, AC, AD, AE series/ KD, KE series

$V_{DD} = 2.7$  to  $3.6$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	$V_{OH}$	Q: Measurement cct 1, $V_{DD} = 2.7$ V, $I_{OH} = 4$ mA	SM5021×AH, CF5021×A SM5021×BH, CF5021×B SM5021×CH, CF5021×C SM5021×DH, CF5021×D	2.1	2.4	–	V
		Q: Measurement cct 1, $V_{DD} = 2.7$ V, $I_{OH} = 8$ mA	SM5021×EH, CF5021×E				
LOW-level output voltage	$V_{OL}$	Q: Measurement cct 2, $V_{DD} = 2.7$ V, $I_{OL} = 4$ mA	SM5021×AH, CF5021×A SM5021×BH, CF5021×B SM5021×CH, CF5021×C SM5021×DH, CF5021×D	–	0.3	0.4	V
		Q: Measurement cct 2, $V_{DD} = 2.7$ V, $I_{OL} = 8$ mA	SM5021×EH, CF5021×E				
Output leakage current	$I_Z$	Q: Measurement cct 2, $V_{DD} = 3.3$ V, $\overline{INH} = \text{LOW}$ , $V_{OH} = V_{DD}$		–	–	10	$\mu\text{A}$
		Q: Measurement cct 2, $V_{DD} = 3.3$ V, $\overline{INH} = \text{LOW}$ , $V_{OL} = V_{SS}$		–	–	10	
HIGH-level input voltage	$V_{IH}$	$\overline{INH}$		2.0	–	–	V
LOW-level input voltage	$V_{IL}$	$\overline{INH}$		–	–	0.5	V
Current consumption	$I_{DD}$	$\overline{INH} = \text{open}$ , Measurement cct 3, load cct 1, $C_L = 15$ pF, 70 MHz crystal oscillator	SM5021A×H, CF5021A× SM5021K×H, CF5021K×	–	13	25	mA
$\overline{INH}$ pull-up resistance	$R_{UP}$	Measurement cct 4		25	100	250	k $\Omega$
Feedback resistance (A× series only)	$R_f$	Measurement cct 5	SM5021×AH, CF5021×A	5.1	6.0	6.9	k $\Omega$
			SM5021×BH, CF5021×B	2.8	3.3	3.8	
			SM5021×CH, CF5021×C	3.3	3.9	4.5	
			SM5021×DH, CF5021×D SM5021×EH, CF5021×E	2.3	2.7	3.1	
Built-in capacitance	$C_G$	Design value, determined by the internal wafer pattern		7.44	8	8.56	pF
	$C_D$	Design value, determined by the internal wafer pattern	SM5021×AH, CF5021×A SM5021×BH, CF5021×B SM5021×CH, CF5021×C SM5021×DH, CF5021×D	13.95	15	16.05	pF
			SM5021×EH, CF5021×E	11.16	12	12.84	

# SM5021 series

5 V operation: AA, AB, AC, AD series/ BA, BB, BC, BD series/ KD series/ LD series

$V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V <sub>OH</sub>	Q: Measurement cct 1, V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = 8 mA		3.9	4.2	–	V
LOW-level output voltage	V <sub>OL</sub>	Q: Measurement cct 2, V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 8 mA		–	0.3	0.4	V
Output leakage current	I <sub>Z</sub>	Q: Measurement cct 2, V <sub>DD</sub> = 5.5 V, $\overline{INH}$ = LOW, V <sub>OH</sub> = V <sub>DD</sub>		–	–	10	μA
		Q: Measurement cct 2, V <sub>DD</sub> = 5.5 V, $\overline{INH}$ = LOW, V <sub>OL</sub> = V <sub>SS</sub>		–	–	10	
HIGH-level input voltage	V <sub>IH</sub>	$\overline{INH}$		2.0	–	–	V
LOW-level input voltage	V <sub>IL</sub>	$\overline{INH}$		–	–	0.8	V
Current consumption	I <sub>DD</sub>	$\overline{INH}$ = open, Measurement cct 3, load cct 1, C <sub>L</sub> = 15 pF, 70 MHz crystal oscillator	SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	18	35	mA
		$\overline{INH}$ = open, Measurement cct 3, load cct 2, C <sub>L</sub> = 15 pF, 70 MHz crystal oscillator	SM5021B×H, CF5021B× SM5021L×H, CF5021L×	–	18	35	
$\overline{INH}$ pull-up resistance	R <sub>UP</sub>	Measurement cct 4		25	100	250	kΩ
Feedback resistance (A×, B× series only)	R <sub>f</sub>	Measurement cct 5	SM5021×AH, CF5021×A	5.1	6.0	6.9	kΩ
			SM5021×BH, CF5021×B	2.8	3.3	3.8	
			SM5021×CH, CF5021×C	3.3	3.9	4.5	
			SM5021×DH, CF5021×D	2.3	2.7	3.1	
Built-in capacitance	C <sub>G</sub>	Design value, determined by the internal wafer pattern	SM5021×AH, CF5021×A SM5021×BH, CF5021×B	7.44	8	8.56	pF
	C <sub>D</sub>		SM5021×CH, CF5021×C SM5021×DH, CF5021×D	13.95	15	16.05	pF

## Switching Characteristics

### CMOS

3 V operation: AA, AB, AC, AD, AE series/ KD, KE series

$V_{DD} = 2.7$  to  $3.6$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	$t_{r1}$	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$ , $C_L = 15$ pF	–	5	10	ns
		SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	3.5	7	
		Measurement cct 6, load cct 1, $0.2V_{DD}$ to $0.8V_{DD}$ , $C_L = 15$ pF	–	3.5	7	
Output fall time	$t_{f1}$	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$ , $C_L = 15$ pF	–	5	10	ns
		SM5021AAH, CF5021AA SM5021ABH, CF5021AB SM5021ACH, CF5021AC SM5021ADH, CF5021AD SM5021KDH, CF5021KD	–	3.5	7	
		Measurement cct 6, load cct 1, $0.8V_{DD}$ to $0.2V_{DD}$ , $C_L = 15$ pF	–	3.5	7	
Output duty cycle <sup>1</sup>	Duty	Measurement cct 6, load cct 1, $T_a = 25$ °C, $V_{DD} = 3$ V, $C_L = 15$ pF, $f \leq 70$ MHz	45	–	55	%
Output disable delay time	$t_{PLZ}$	Measurement cct 6, load cct 1, $T_a = 25$ °C, $V_{DD} = 3$ V, $C_L = 15$ pF	–	–	100	ns
Output enable delay time	$t_{PZL}$		–	–	100	ns

1. Determined by the lot monitor.

5 V operation: AA, AB, AC, AD series/ KD series

$V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	$t_{r1}$	Measurement cct 6, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$ , $C_L = 15$ pF	–	3.5	7	ns
Output fall time	$t_{f1}$	Measurement cct 6, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$ , $C_L = 15$ pF	–	3.5	7	ns
Output duty cycle <sup>1</sup>	Duty	Measurement cct 6, load cct 1, $T_a = 25$ °C, $V_{DD} = 5$ V, $C_L = 15$ pF, $f \leq 70$ MHz	45	–	55	%
Output disable delay time	$t_{PLZ}$	Measurement cct 6, load cct 1, $T_a = 25$ °C, $V_{DD} = 5$ V, $C_L = 15$ pF	–	–	100	ns
Output enable delay time	$t_{PZL}$		–	–	100	ns

1. Determined by the lot monitor.

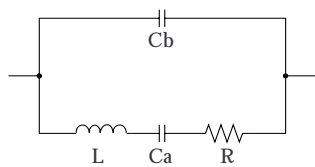
**TTL**

5 V operation: BA, BB, BC, BD series/ LD series

$V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $80$  °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	$t_{r2}$	Measurement cct 6, load cct 2, 0.4V to 2.4V, $C_L = 15$ pF	–	2.5	7	ns
Output fall time	$t_{f2}$	Measurement cct 6, load cct 2, 2.4V to 0.4V, $C_L = 15$ pF	–	2.5	7	ns
Output duty cycle <sup>1</sup>	Duty	Measurement cct 6, load cct 2, $T_a = 25$ °C, $V_{DD} = 5$ V, $C_L = 15$ pF, $f \leq 70$ MHz	45	–	55	%
Output disable delay time	$t_{PLZ}$	Measurement cct 6, load cct 2, $T_a = 25$ °C, $V_{DD} = 5$ V, $C_L = 15$ pF	–	–	100	ns
Output enable delay time	$t_{PZL}$		–	–	100	ns

1. Determined by the lot monitor.

**Current consumption and Output waveform with NPC's standard crystal**

f (MHz)	R (Ω)	L (mH)	Ca (fF)	Cb (pF)
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
60	22.20	5.05	1.388	4.226
70	25.42	4.18	1.254	5.170

**FUNCTIONAL DESCRIPTION****Standby Function**

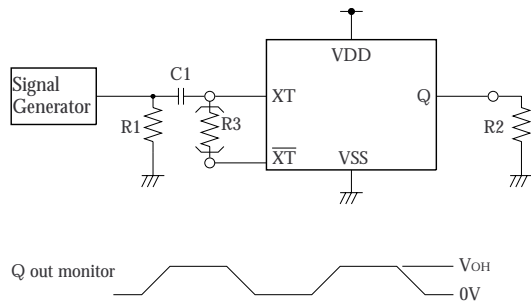
When  $\overline{INH}$  goes LOW, the oscillator output on Q goes high impedance.

$\overline{INH}$	Q	Oscillator
HIGH (or open)	$f_O$ output frequency	Normal operation
LOW	High impedance	Normal operation



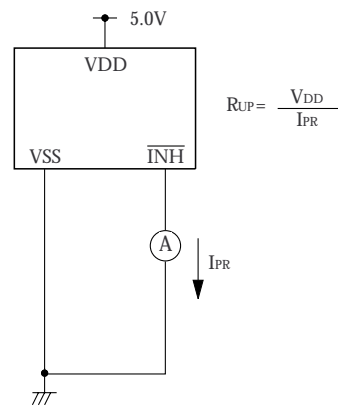
## MEASUREMENT CIRCUITS

### Measurement cct 1

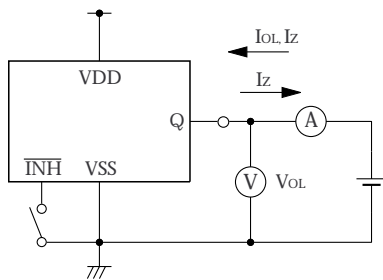


2.0V<sub>P-P</sub>, 10MHz sine wave input signal (3V operation)  
 3.5V<sub>P-P</sub>, 10MHz sine wave input signal (5V operation)  
 C1 : 0.001μF  
 R1 : 50Ω  
 R2 : 525Ω (3V operation/×A, ×B, ×C, ×D series)  
 263Ω (3V operation/×E series)  
 490Ω (5V operation)  
 R3 : 100kΩ (K×, L× series)

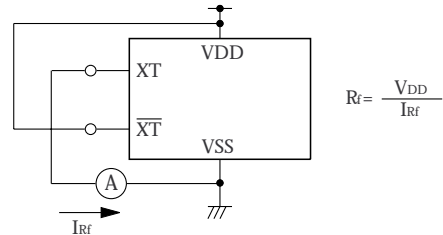
### Measurement cct 4



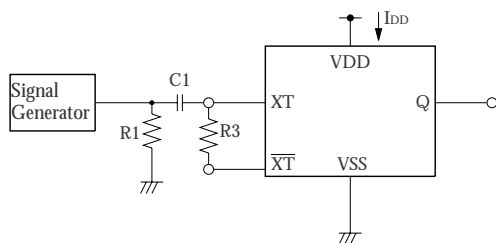
### Measurement cct 2



### Measurement cct 5

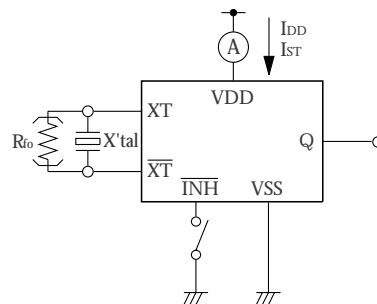


### Measurement cct 3



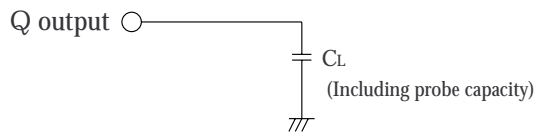
2.0V<sub>P-P</sub>, 70MHz sine wave input signal (3V operation)  
 3.5V<sub>P-P</sub>, 70MHz sine wave input signal (5V operation)  
 C1 : 0.001μF  
 R1 : 50Ω  
 R3 : 100kΩ (K×, L× series)

### Measurement cct 6



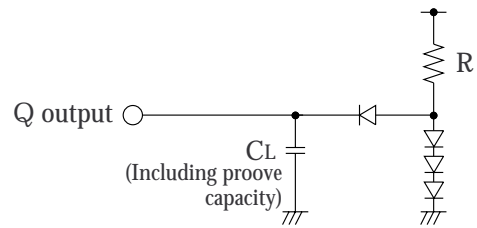
$R_{f0} : 2.7k\Omega$  (K×, L× series)

### Load cct 1



$$C_L = 15\text{pF}; t_{r1}, t_{f1}$$

### Load cct 2

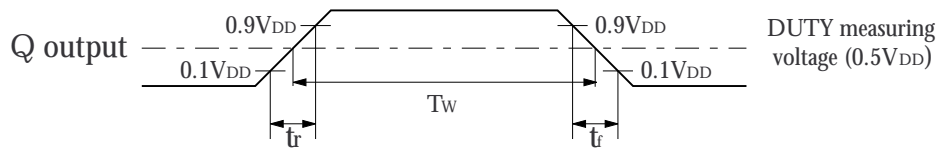


$$C_L = 15\text{pF}; t_{r2}, t_{f2}$$

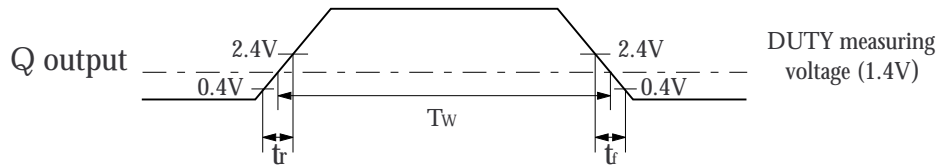
$$R = 800\Omega$$

## Switching Time Measurement Waveform

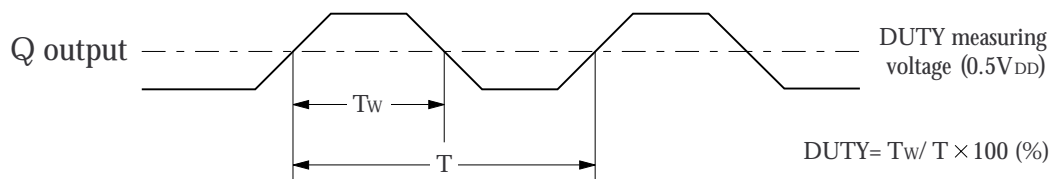
### Output duty level (CMOS)



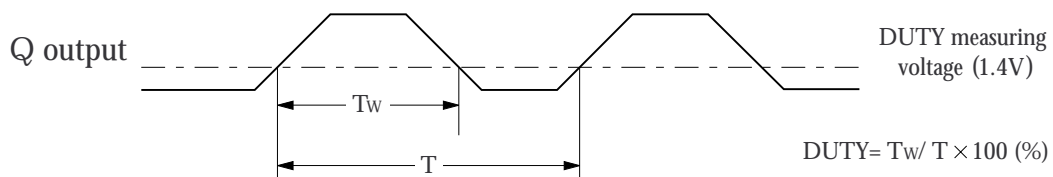
### Output duty level (TTL)



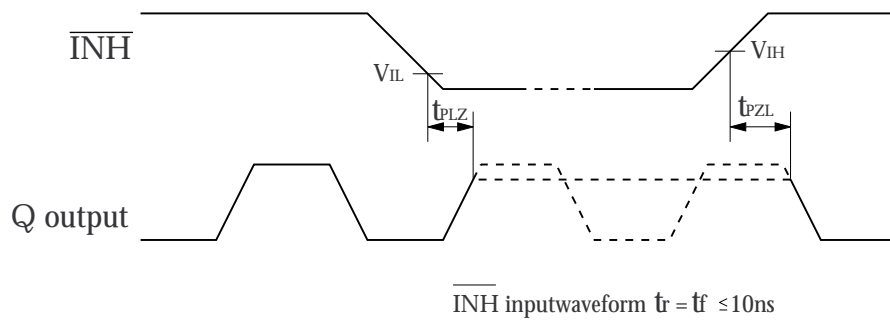
### Output duty cycle (CMOS)



### Output duty cycle (TTL)



## Output Enable/Disable Delay



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