

100304 Low Power Quint AND/NAND Gate

General Description

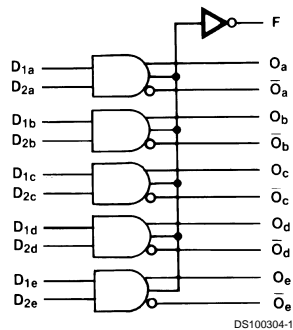
The 100304 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

- 2000V ESD protection
- Pin/function compatible with 100104
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to Standard Microcircuit Drawing (SMD) 5962-9153701

Features

- Low Power Operation

Logic Symbol



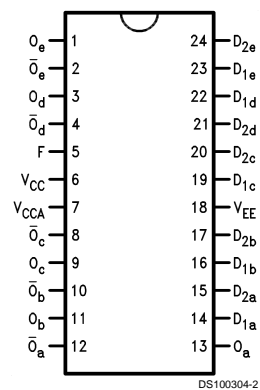
Logic Equation

$$F = (\overline{D_{1a}} \cdot \overline{D_{2a}}) + (\overline{D_{1b}} \cdot \overline{D_{2b}}) + (\overline{D_{1c}} \cdot \overline{D_{2c}}) + (\overline{D_{1d}} \cdot \overline{D_{2d}}) + (\overline{D_{1e}} \cdot \overline{D_{2e}}).$$

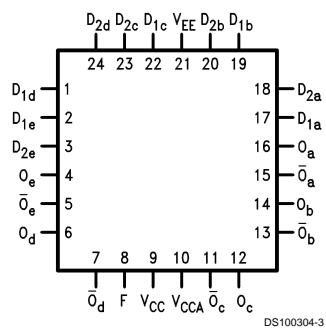
Pin Names	Description
D_{1a} – D_{2e}	Data Inputs
F	Function Output
O_a – O_e	Data Outputs
$\overline{O_a}$ – $\overline{O_e}$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



24-Pin Quad Cerpak



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T_{STG}) -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J)

Ceramic $+175^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

ESD (Note 2)

$\geq 2000\text{V}$

Recommended Operating Conditions

Case Temperature (T_C)

Military -55°C to $+125^{\circ}\text{C}$

Supply Voltage (V_{EE}) -5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -5.7V , $V_{CC} = V_{CCA} = \text{GND}$, $T_C = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

Symbol	Parameter	Min	Max	Units	T _C	Conditions		Notes
V _{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085	-870	mV	-55°C			
V _{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1830	-1555	mV	-55°C			
V _{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085		mV	-55°C			
V _{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
			-1555	mV	-55°C			
V _{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C +125°C	Guaranteed HIGH Signal for All Inputs		(Notes 3, 4, 5, 6)
V _{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs		(Notes 3, 4, 5, 6)
I _{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	V _{EE} = -4.2V V _{IN} = V _{IL} (Min)		(Notes 3, 4, 5)
I _{IH}	Input High Current D _{2a} -D _{2e} D _{1a} -D _{1e}		250 350	μA	0°C to +125°C	V _{EE} = -5.7V V _{IN} = V _{IH} (Max)		(Notes 3, 4, 5)
	D _{2a} -D _{2e} D _{1a} -D _{1e}		350 500	μA	-55°C			
I _{EE}	Power Supply Current	-75	-25	mA	-55°C to +125°C	Inputs Open		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C , $+25^{\circ}\text{C}$, and $+125^{\circ}\text{C}$, Subgroups, 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C , $+25^{\circ}\text{C}$, and $+125^{\circ}\text{C}$, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $+25^{\circ}\text{C}$ temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each mfg. lot at $+25^{\circ}\text{C}$, Subgroup A9, and at $+125^{\circ}\text{C}$ and -55°C temperatures, Subgroups A10 and A11.

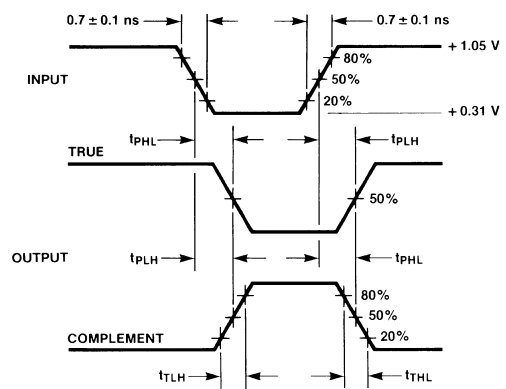
Note 10: Not tested at $+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, and -55°C temperature (design characterization data).

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$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1\ \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_1 = Fixture and stray capacitance $\leq 3\ pF$

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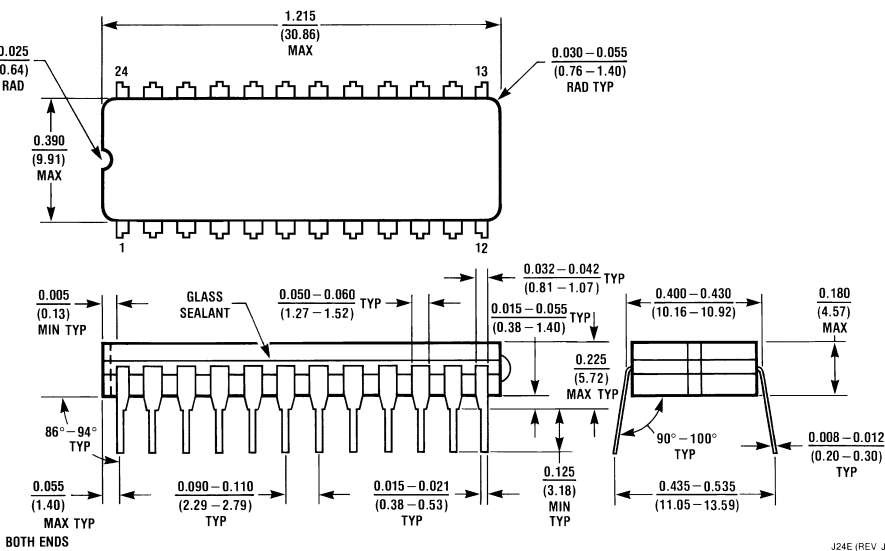
Switching Waveforms



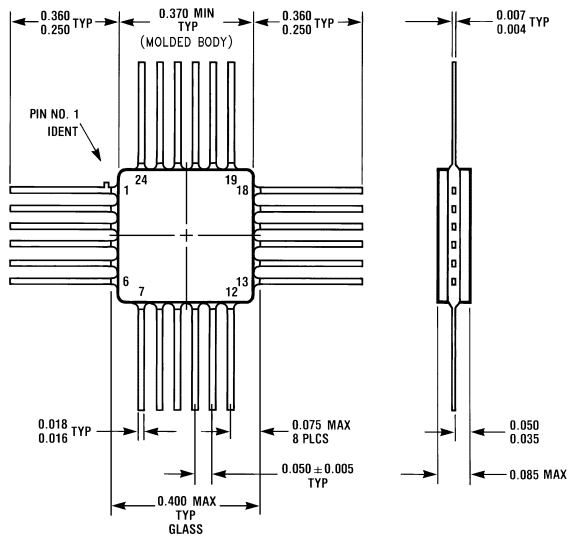
DS100304-6

FIGURE 2. Propagation Delay and Transition Times



Physical Dimensions inches (millimeters) unless otherwise noted

24-Pin Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Pin Quad Cerpak (F)
NS Package Number W24B

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