National Semiconductor

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100323
Low Power Hex Bus Driver

General Description

The 100323 is a monolithic device containing six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its own respective ground connection. Transition times were designed to be longer than on other F100K devices. The driver itself performs the positive logic AND of a data input (D_1–D_6) and the OR of two select inputs (E and either DE_1, DE_2, or DE_3).

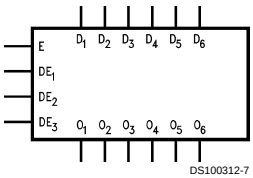
Enabling of data is possible in multiples of two, i.e., 2, 4 or all 6 paths. All inputs have 50 kΩ pull-down resistors.

The output voltage LOW level is designed to be more negative than normal ECL outputs (cut off state). This allows an emitter-follower output transistor to turn off when the termination supply is −2.0V and thus present a high impedance to the data bus.

Features

- 50% power reduction of the 100123
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Drives 25Ω load

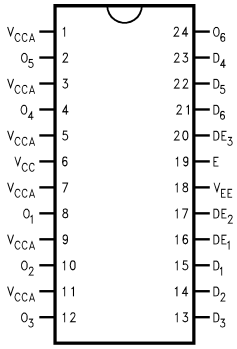
Logic Symbol



Pin Names	Description
D_1–D_6	Data Inputs
DE_1–DE_3	Dual Enable Inputs
E	Common Enable Input
O_1–O_6	Data Outputs

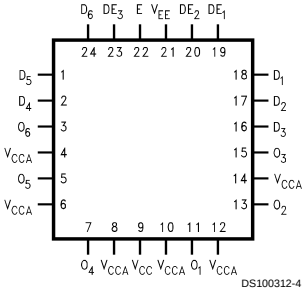
Connection Diagrams

24-Pin DIP



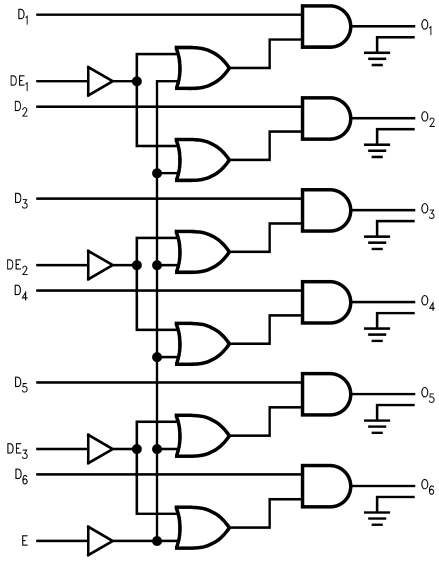
DS100312-3

24-Pin Quad Cerpak



DS100312-4

Logic Diagram



DS100312-1

Truth Table

E	DE_n	D_n	D_{n+1}	O_n	O_{n+1}
L	L	X	X	Cutoff	Cutoff
X	H	L	L	Cutoff	Cutoff
X	H	L	H	Cutoff	H
X	H	H	L	H	Cutoff
X	H	H	H	H	H
H	X	L	L	Cutoff	Cutoff
H	X	L	H	Cutoff	H
H	X	H	L	H	Cutoff
H	X	H	H	H	H

H = High
Cutoff = Lower-than-LOW state
L = Low
X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Maximum Junction Temperature	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−50 mA
ESD	≥2000V

Recommended Operating Conditions

Case Temperature	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH	−1025	−870	mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (max)}$	Loading with	(Notes 3, 4, 5)
	Voltage	−1085	−870	mV	−55˚C	or $V_{IL\ (min)}$	25Ω to −2.0V	
V_{OHC}	Output HIGH	−1035		mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (min)}$	Loading with	(Notes 3, 4, 5)
	Voltage	−1085		mV	−55˚C	or $V_{IL\ (max)}$	25Ω to −2.0V	
V_{OLC}	Output LOW		−1610	mV	0˚C to +125˚C			
	Voltage		−1555	MV	−55˚C			
V_{OLZ}	Cut-Off LOW		−1950	mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (min)}$	Loading with	(Notes 3, 4, 5)
	Voltage		−1850		−55˚C	or $V_{IL\ (max)}$	25Ω to −2.0V	
V_{IH}	Input HIGH	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal		(Notes 3, 4, 5, 6)
	Voltage					for All Inputs		
V_{IL}	Input LOW	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal		(Notes 3, 4, 5, 6)
	Voltage					for All Inputs		
I_{IL}	Input LOW	0.50		µA	−55˚C to +125˚C	V_{EE} = 4.2V, V_{IN} = $V_{IL\ (min)}$		(Notes 3, 4, 5)
	Current							
I_{IH}	Input HIGH		240	µA	0˚C to +125˚C	V_{EE} = −5.7V, V_{IN} = $V_{IH\ (max)}$		(Notes 3, 4, 5)
	Current		340	µA	−55˚C			
I_{EE}	Power Supply					Inputs Open		
	Current	−155	−53	mA	−55˚C to +125˚C	V_{EE} = −4.2V to −5.7V		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

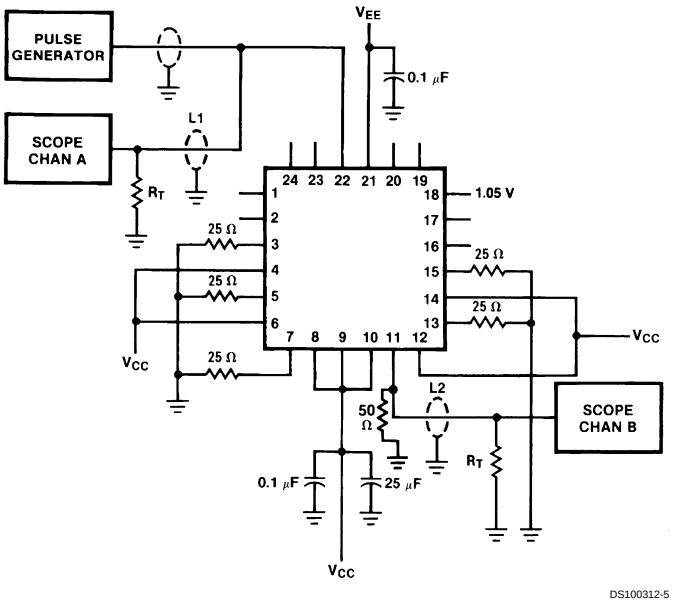
V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PZH}	Propagation Delay	0.70	3.70	1.10	3.60	1.20	3.60	ns	*Figures 1, 2*
t_{PHZ}	Data to Output	0.50	3.60	1.10	3.10	1.20	3.50		
t_{PZH}	Propagation Delay	0.60	3.60	1.10	3.60	1.30	3.80	ns	
t_{PHZ}	Data Enable to Output	1.00	4.20	1.50	3.60	1.60	4.00		
t_{PZH}	Propagation Delay	0.70	3.60	1.00	3.50	1.20	3.60	ns	
t_{PHZ}	Common Enable to Output	0.90	4.00	1.40	3.40	1.40	3.80		
t_{TZH}	Transition Time	0.20	2.00	0.20	2.00	0.20	2.00	ns	
t_{THZ}	20% to 80%, 80% to 20%	0.20	1.80	0.20	1.60	0.20	1.60		

Note 7: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 8: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Timing Waveform

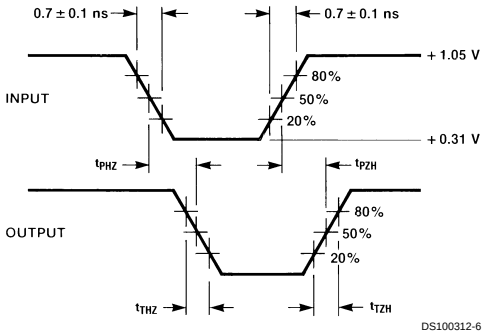
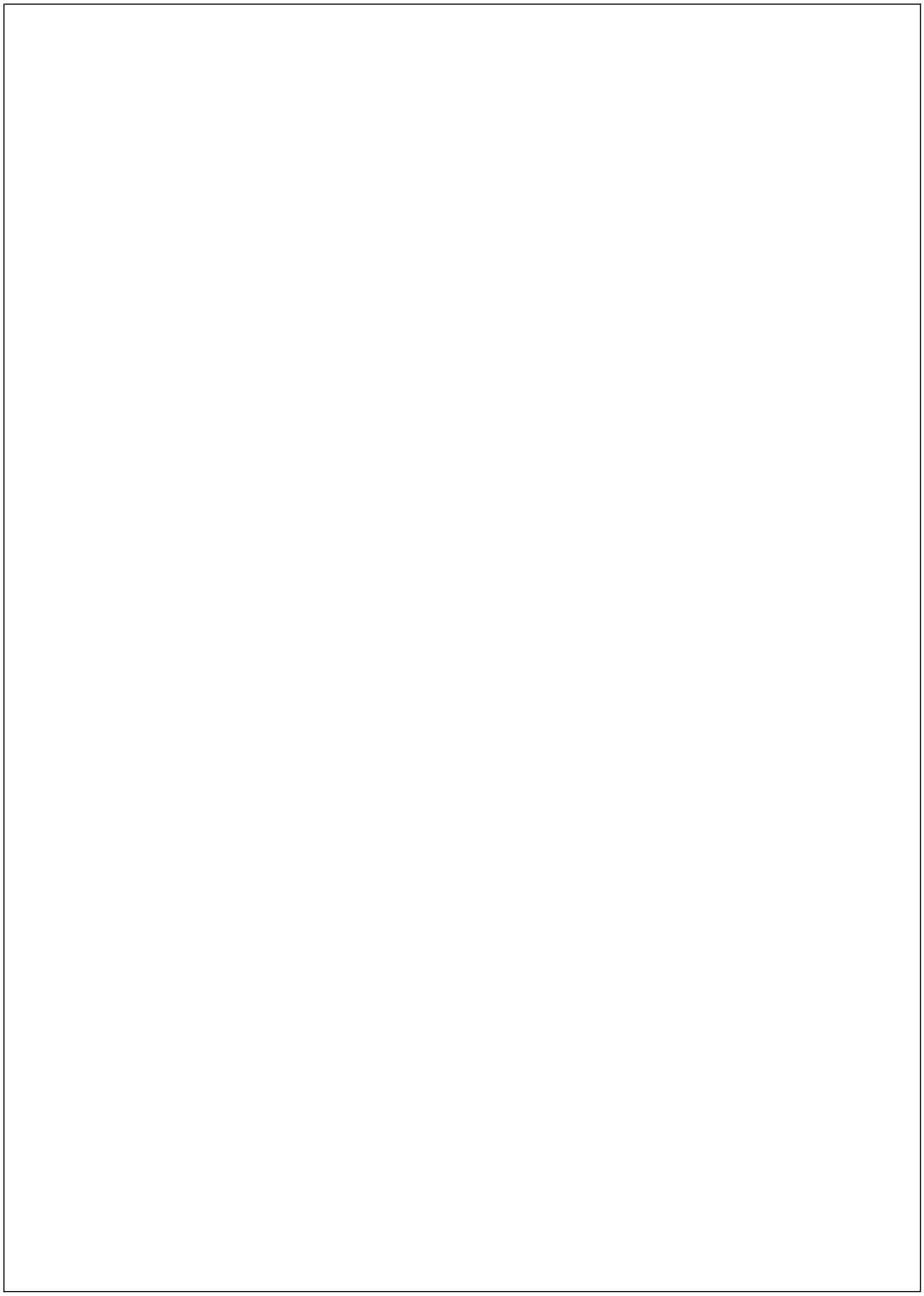
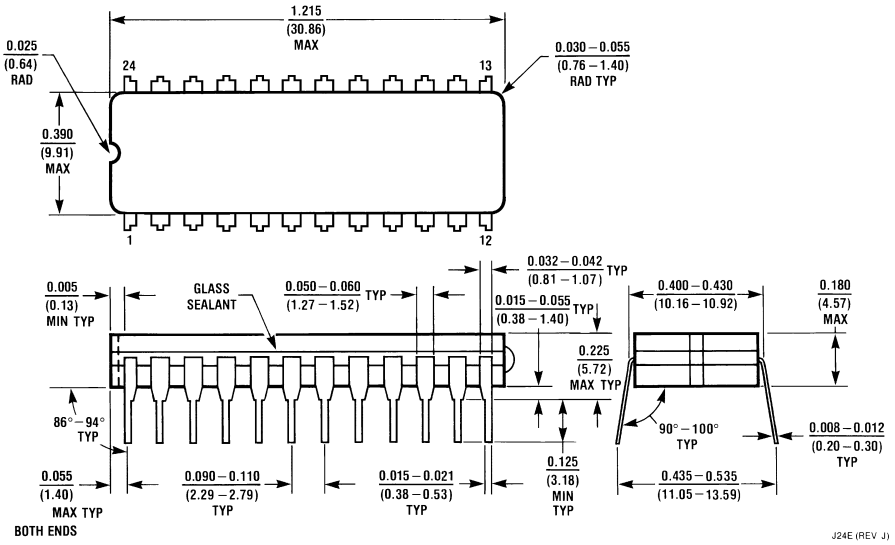


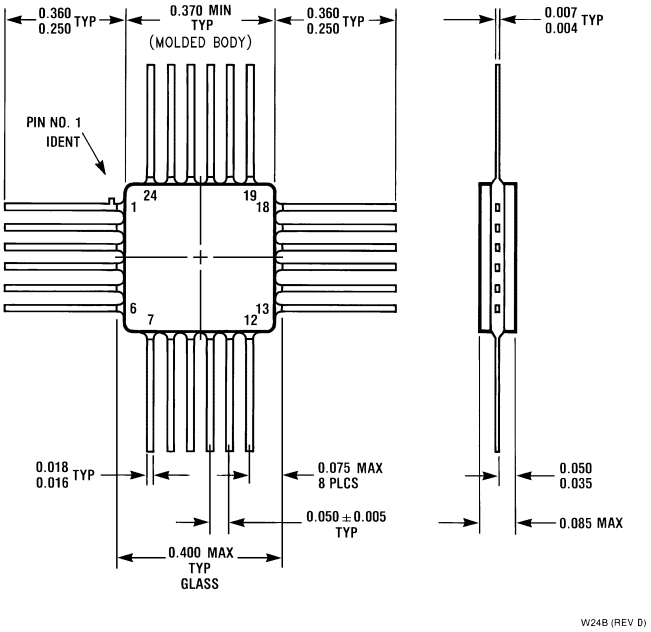
FIGURE 2. Propagation Delay and Transition Times



Physical Dimensions inches (millimeters) unless otherwise noted



24 Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24 Lead Quad Cerpak (F)
NS Package Number W24B

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