

# 54ACTQ827

## Quiet Series 10-Bit Buffer/Line Driver with TRI-STATE® Outputs

### General Description

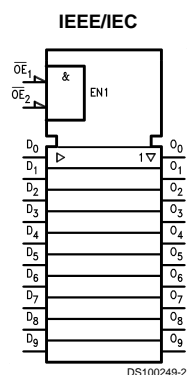
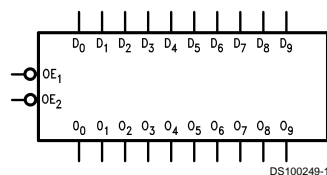
The 'ACTQ827 10-bit bus buffer provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility. The 'ACTQ827 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ feature GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- Functionally and pin-compatible to AMD's AM29827
- 'ACTQ827 has TTL-compatible inputs
- 4 kV minimum ESD immunity
- Standard Microcircuit Drawing (SMD) 5962-92199

### Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance

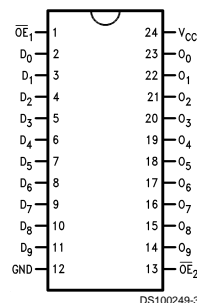
### Logic Symbols



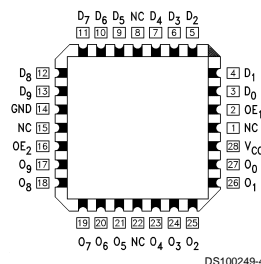
Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable
$D_0$ – $D_9$	Data Inputs
$O_0$ – $O_9$	Data Outputs

### Connection Diagrams

Pin Assignment for DIP and Flatpak



Pin Assignment for LCC



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 FACT® is a registered trademark of Fairchild Semiconductor Corporation.  
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## Functional Description

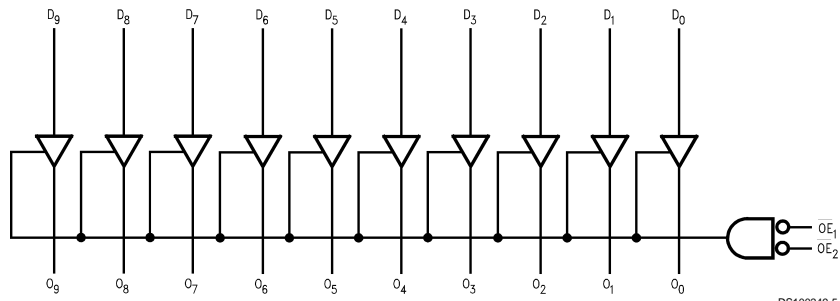
The 'ACTQ827 line driver is designed to be employed as memory address driver, clock driver and bus-oriented transmitter/receiver. The devices have TRI-STATE outputs controlled by the Output Enable ( $\overline{OE}$ ) pins. When the  $\overline{OE}$  is LOW, the device is transparent. When  $\overline{OE}$  is HIGH, the device is in TRI-STATE mode.

## Function Table

Inputs		Outputs	Function
$\overline{OE}$	$D_n$	$O_n$	
L	H	H	Transparent
L	L	L	Transparent
H	X	Z	High Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 Z = HIGH Impedance  
 X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	–0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	–0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	–0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	–65°C to +150°C

DC Latch-Up Source	
or Sink Current	±300 mA
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACTQ	–55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

**Note 2:** All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from –40°C to +125°C.

## DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54ACTQ	Units	Conditions
			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
$V_{OH}$	Minimum High Level Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		5.5	4.70		
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, \text{ GND}$
$I_{OZ}$	Maximum TRI-STATE Current	5.5	±10.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{ GND}$
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
$I_{OLD}$	(Note 4) Minimum Dynamic	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$
$I_{OHD}$	Output Current	5.5	–50	mA	$V_{OHD} = 3.85V \text{ Min}$
$I_{CC}$	Maximum Quiescent Supply Current	5.5	160.0	μA	$V_{IN} = V_{CC}$ or GND (Note 5)

## DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54ACTQ	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.5	V	(Notes 6, 7)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-1.2	V	(Notes 6, 7)

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 6:** Plastic DIP package.

**Note 7:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

**Note 8:** Max number of data inputs (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold. (V<sub>HD</sub>), f = 1 MHz.

## AC Electrical Characteristics

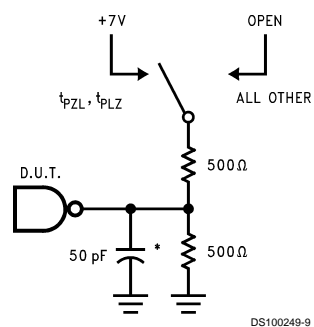
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54ACTQ		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	5.0	2.0	9.0	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	5.0	2.0	12.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	5.0	1.0	9.0	ns

**Note 9:** Voltage Range 5.0 is 5.0V ±0.5V.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	82	pF	V <sub>CC</sub> = 5.0V

## AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

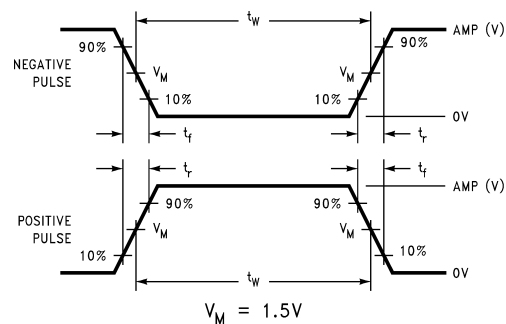


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

## AC Waveforms

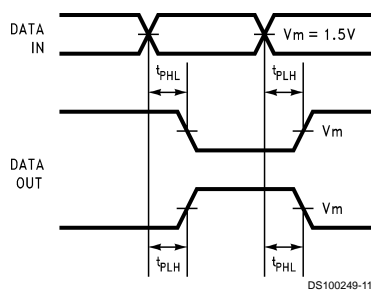


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

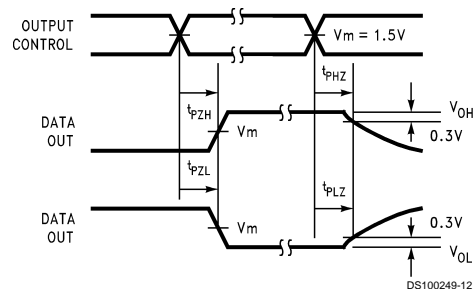
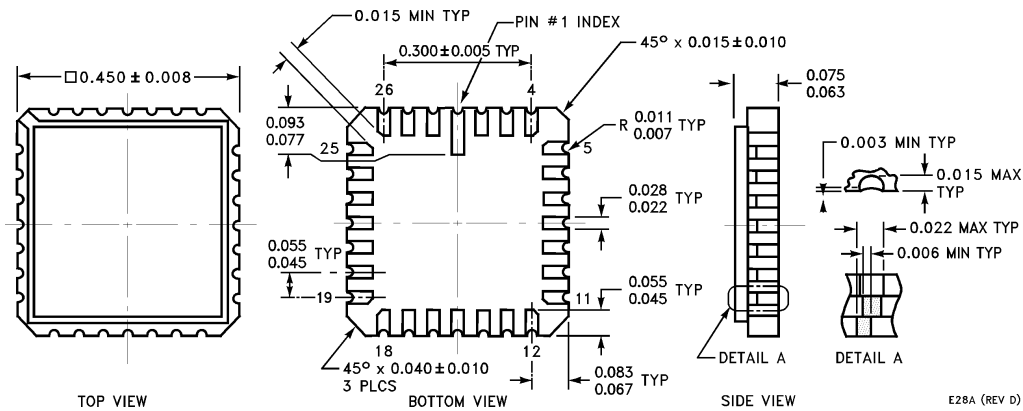


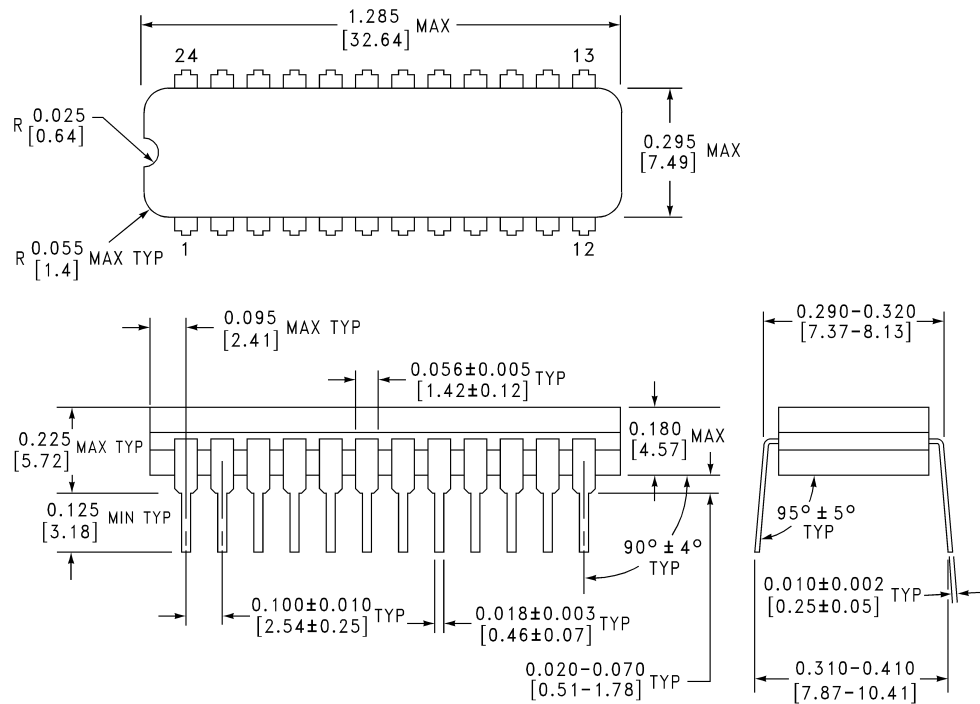
FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Time



# Physical Dimensions inches (millimeters) unless otherwise noted

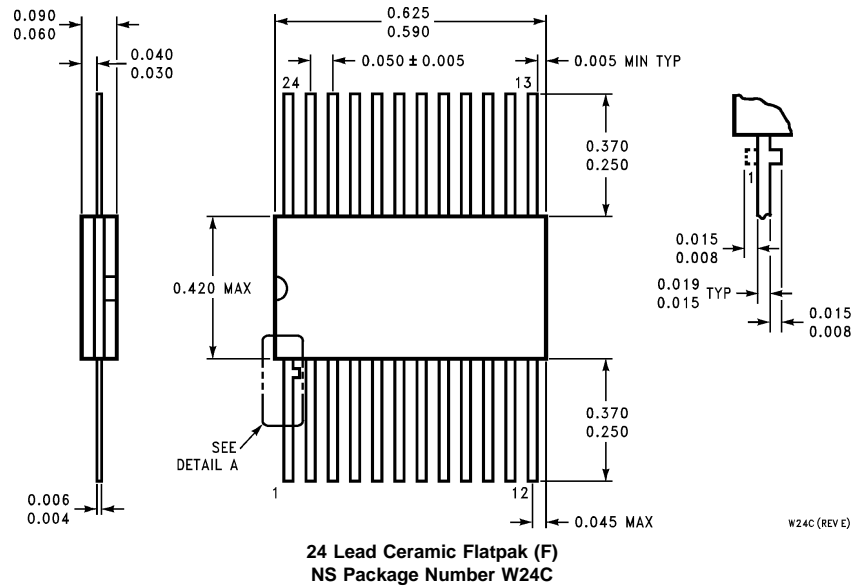


**28-Terminal Ceramic Leadless Chip Carrier (L)**  
NS Package Number E28A



**24-Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD)**  
NS Package Number J24F

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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