

54F/74F299 Octal Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The 'F299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs, Q₀–Q₇, are provided to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

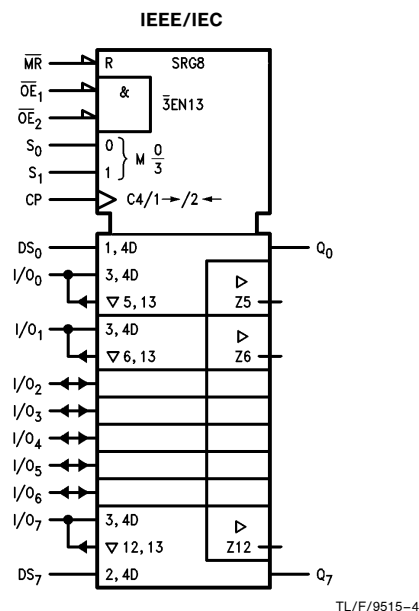
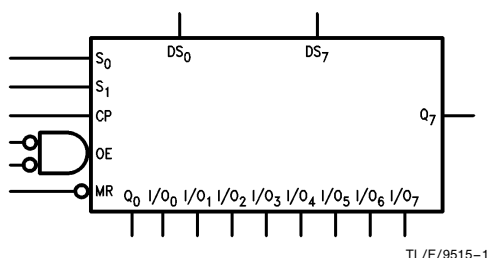
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F299PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F299DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F299SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F299SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F299FM (Note 2)	W20A	20-Lead Cerpack
	54F299LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMOB, FMQB and LMOB.

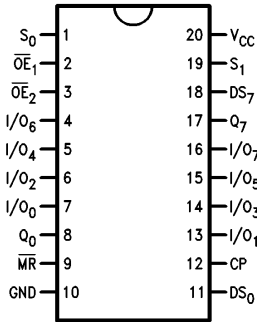
Logic Symbols



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

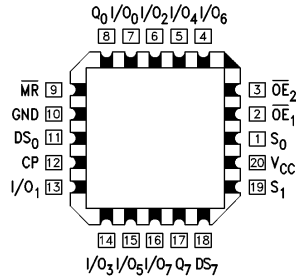
Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak



TL/F/9515-2

Pin Assignment
for LCC



TL/F/9515-3

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
DS ₀	Serial Data Input for Right Shift	1.0/1.0	20 μ A/ -0.6 mA
DS ₇	Serial Data Input for Left Shift	1.0/1.0	20 μ A/ -0.6 mA
S ₀ , S ₁	Mode Select Inputs	1.0/2.0	20 μ A/ -1.2 mA
\overline{MR}	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}_1 , \overline{OE}_2	TRI-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
I/O ₀ -I/O ₇	Parallel Data Inputs or TRI-STATE Parallel Outputs	3.5/1.083 150/40(33.3)	70 μ A/ -0.65 mA -3 mA/24 mA (20 mA)
Q ₀ , Q ₇	Serial Outputs	50/33.3	-1 mA/20 mA

Functional Description

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{MR} overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE outputs are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
\overline{MR}	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset; Q ₀ -Q ₇ = LOW
H	H	H	↗	Parallel Load; I/O _n → Q _n
H	L	H	↗	Shift Right; DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L	↗	Shift Left; DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold

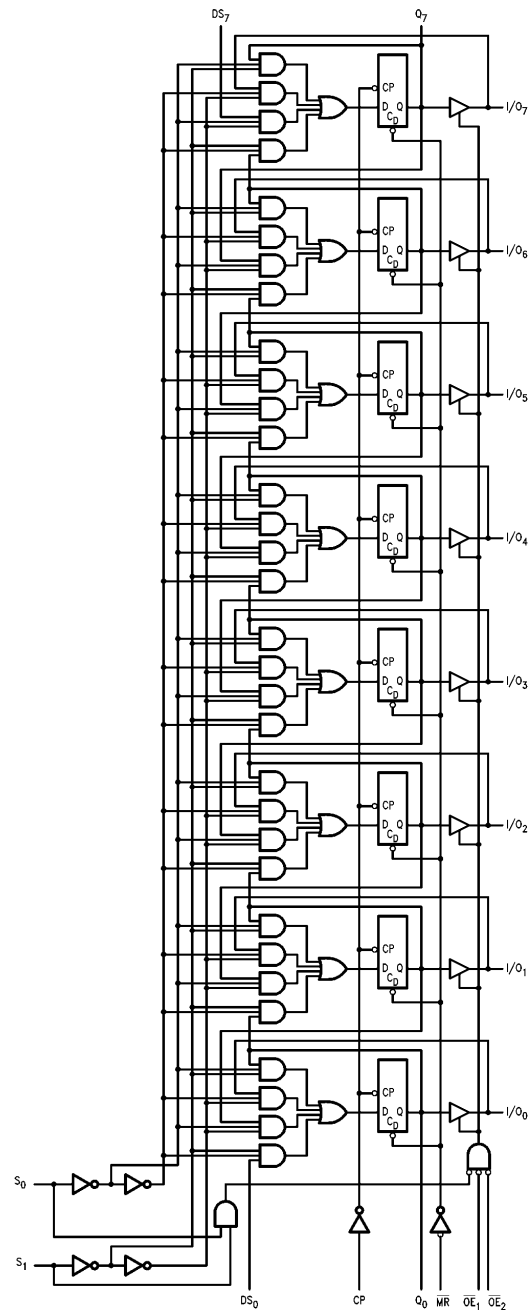
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9515-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C

V_{CC} Pin Potential to Ground Pin −0.5V to +7.0V

Input Voltage (Note 2) −0.5V to +7.0V

Input Current (Note 2) −30 mA to +5.0 mA

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output
in HIGH State (with V_{CC} = 0V)
Standard Output −0.5V to V_{CC}
TRI-STATE Output −0.5V to +5.5V

Current Applied to Output
in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature
Military −55°C to +125°C
Commercial 0°C to +70°C

Supply Voltage
Military +4.5V to +5.5V
Commercial +4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = −1 mA (Q ₀ , Q ₇ , I/O _n) I _{OH} = −3 mA (I/O _n) I _{OH} = −1 mA (Q ₀ , Q ₇ , I/O _n) I _{OH} = −3 mA (I/O _n) I _{OH} = −1 mA (Q ₀ , Q ₇ , I/O _n) I _{OH} = −3 mA (I/O _n)
V _{OL}	Output LOW Voltage	54 10% V _{CC} 74 10% V _{CC} 74 10% V _{CC}		0.5 0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA (Q ₀ , Q ₇) I _{OL} = 24 mA (I/O _n)
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V (CP, DS ₀ , DS ₇ , S ₀ , S ₁ , MR, OE ₁ , OE ₂)
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V (CP, DS ₀ , DS ₇ , S ₀ , S ₁ , MR, OE ₁ , OE ₂)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	54F 74F		1.0 0.5	mA	Max	V _{IN} = 5.5V (I/O _n)
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6 −1.2	mA	Max	V _{IN} = 0.5V (CP, DS ₀ , DS ₇ , MR, OE ₁ , OE ₂) V _{IN} = 0.5V (S ₀ , S ₁)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{I/O} = 2.7V (I/O _n)
I _{IL} + I _{OZL}	Output Leakage Current			−650	μA	Max	V _{I/O} = 0.5V (I/O _n)
I _{OS}	Output Short-Circuit Current		−60	−150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current		68	95	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		68	95	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		68	95	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

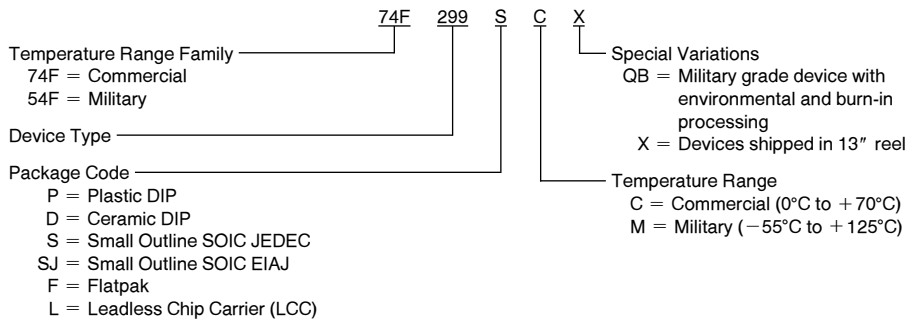
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Input Frequency	70	100		85		70		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	4.0 4.5	7.0 6.5	8.0 8.0	4.0 4.5	9.0 9.5	4.0 4.5	8.5 8.5	ns
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	3.5 4.0	7.0 8.5	9.0 9.0	3.5 4.0	10.0 11.0	3.5 4.0	10.0 10.0	
t _{PHL}	Propagation Delay MR to Q ₀ or Q ₇	5.5	7.5	9.5	5.5	12.5	5.5	10.5	ns
t _{PHL}	Propagation Delay MR to I/O _n	5.5	11.0	10.0	5.5	12.0	5.5	10.5	
t _{PZH} t _{PZL}	Output Enable Time OE to I/O _n	3.5 4.0	6.0 7.0	8.0 10.0	3.0 4.0	9.5 13.0	3.5 4.0	9.0 11.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE to I/O _n	2.0 1.0	4.5 4.0	6.0 5.5	1.5 1.0	7.0 6.5	2.0 1.0	7.0 6.5	
t _{PZH} t _{PZL}	Output Enable Time S _n to I/O _n	3.5 4.0		9.0 10.0	3.0 4.0	10.5 13.0	3.5 4.0	10.0 11.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time S _n to I/O _n	2.5 1.5		6.0 5.5	1.5 1.0	7.0 6.5	2.5 1.5	7.0 6.5	ns

AC Operating Requirements

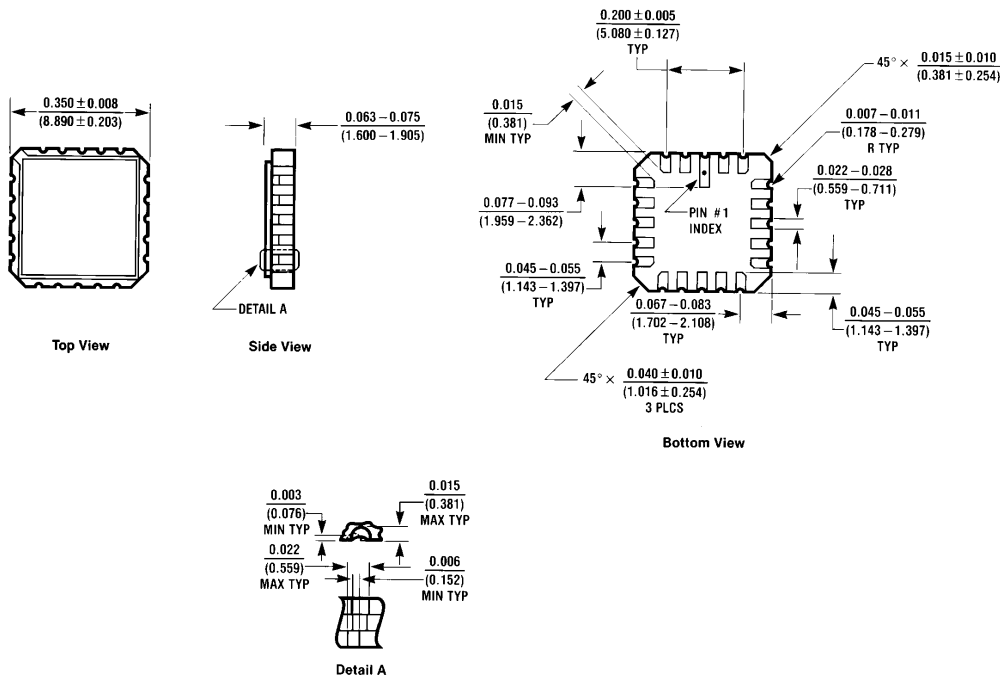
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW S_0 or S_1 to CP	8.5 8.5		10.0 7.5		8.5 8.5		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0		0 0		0 0		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $I/O_n, DS_0$ or DS_7 to CP	5.0 5.0		5.0 5.0		5.0 5.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $I/O_n, DS_0$ or DS_7 to CP	2.0 2.0		2.0 2.0		2.0 2.0		
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.0		6.0		5.0		ns
t_{rec}	Recovery Time, $\overline{\text{MR}}$ to CP	7.0		12.0		7.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



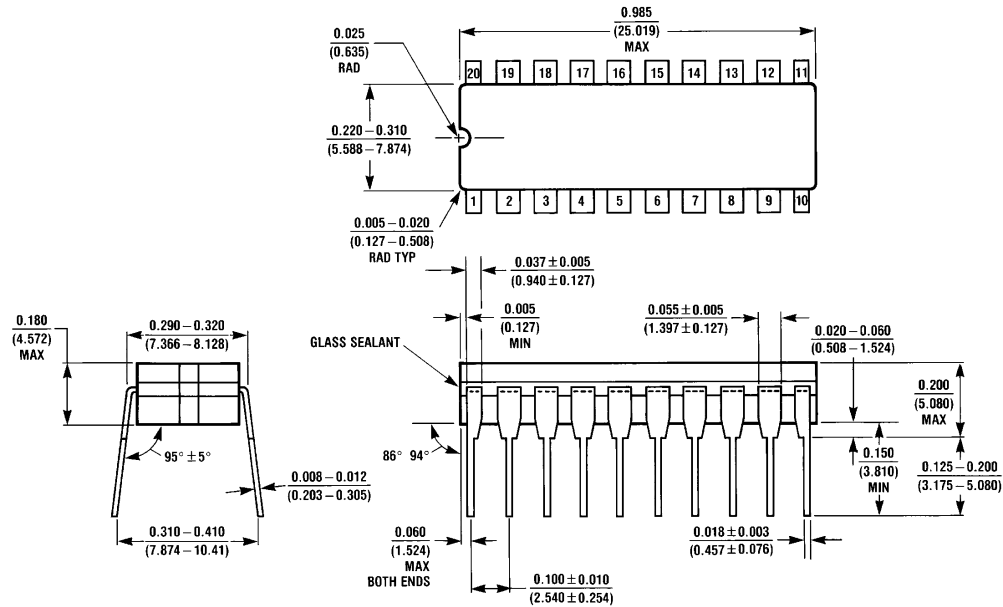
Physical Dimensions inches (millimeters)



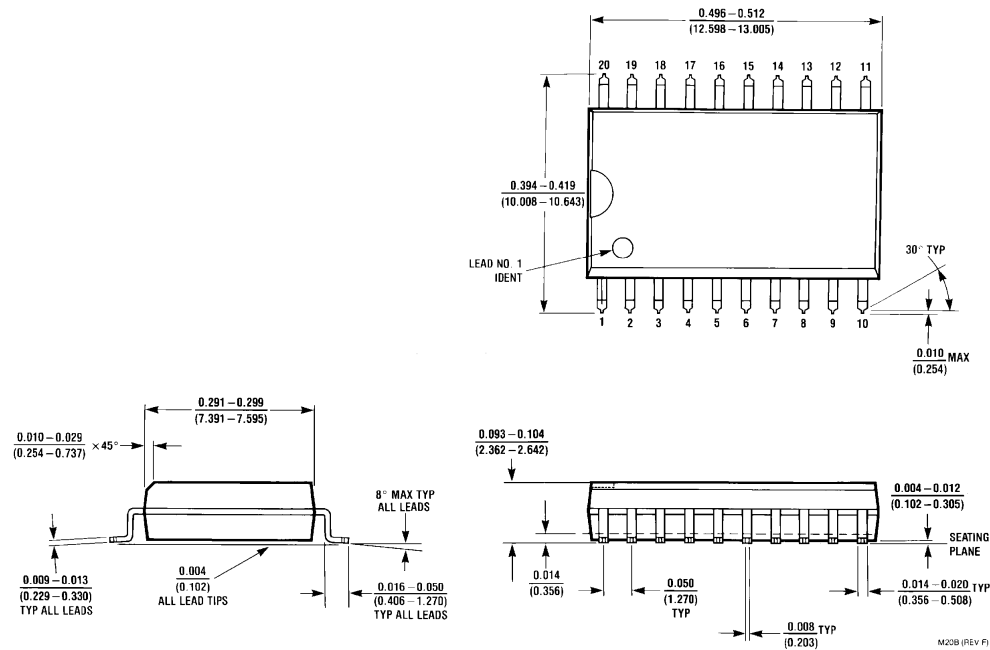
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

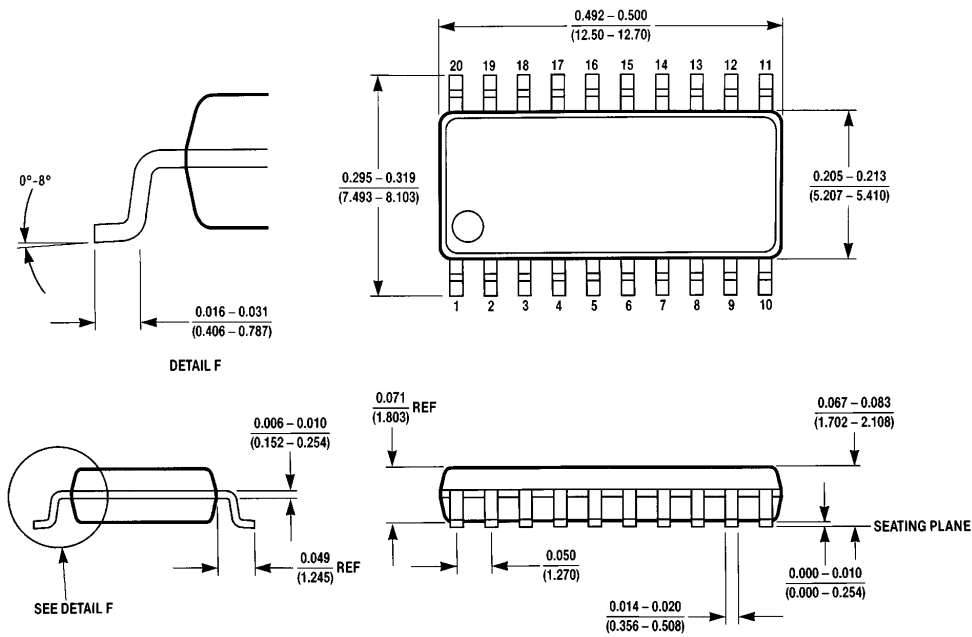


**20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A**



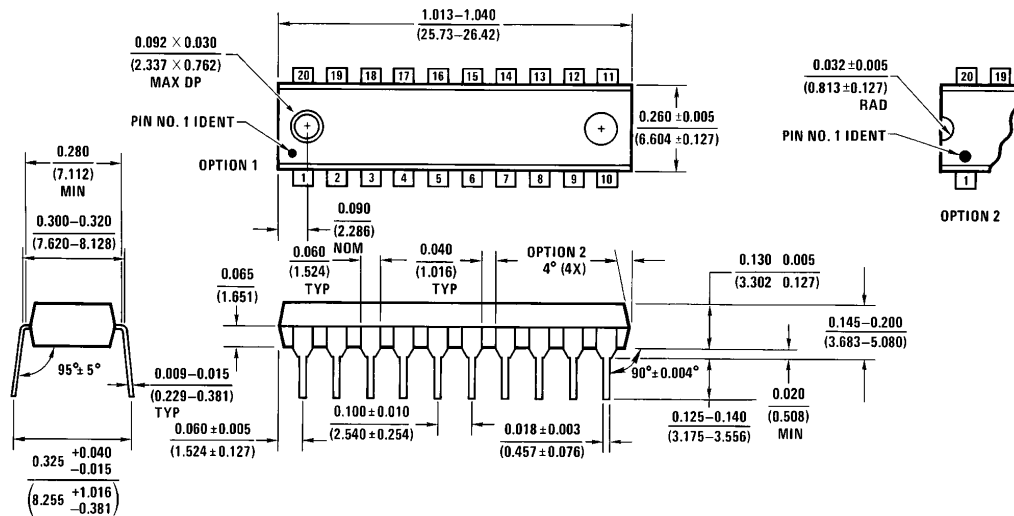
**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B**

Physical Dimensions inches (millimeters) (Continued)



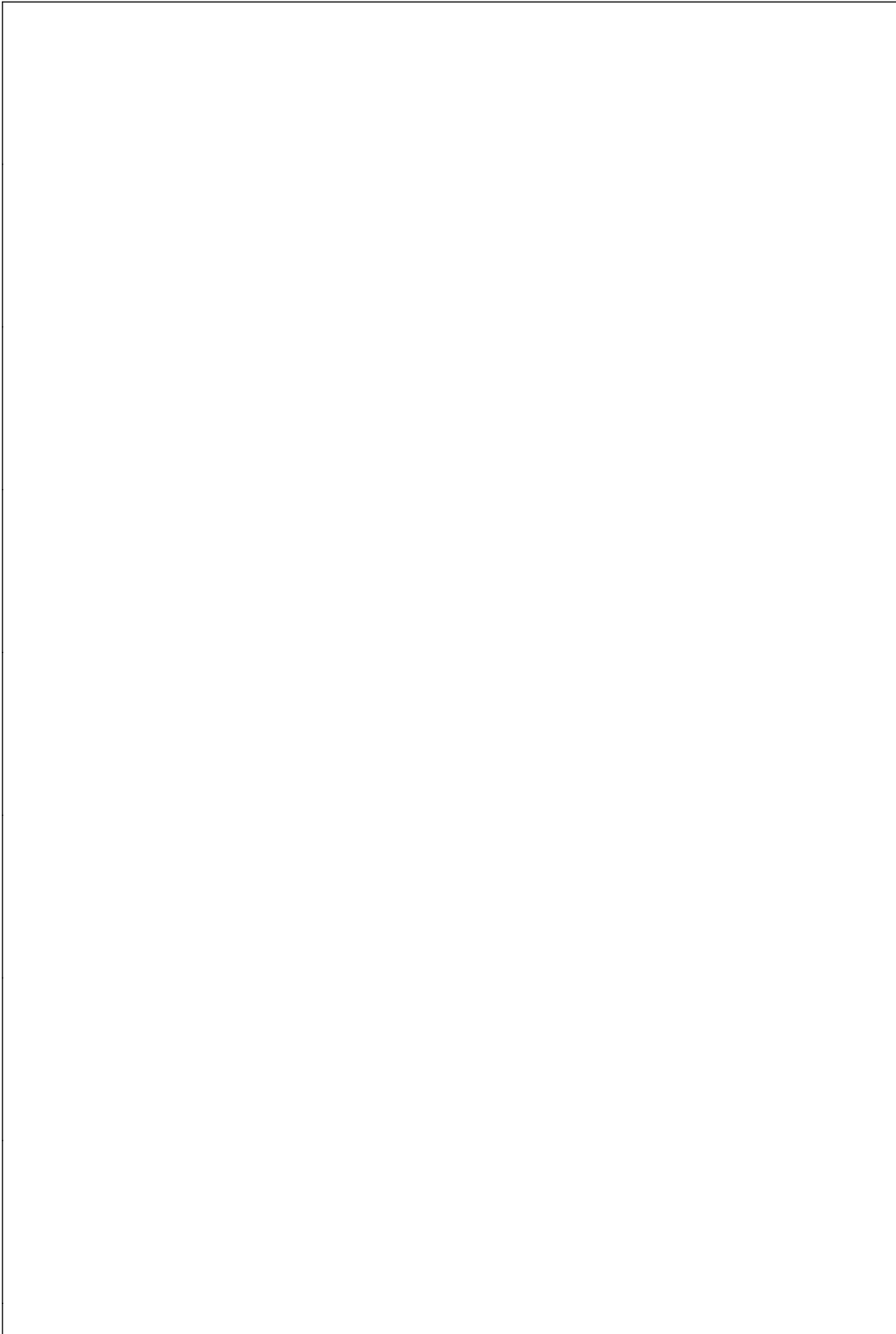
M20D (REV A)

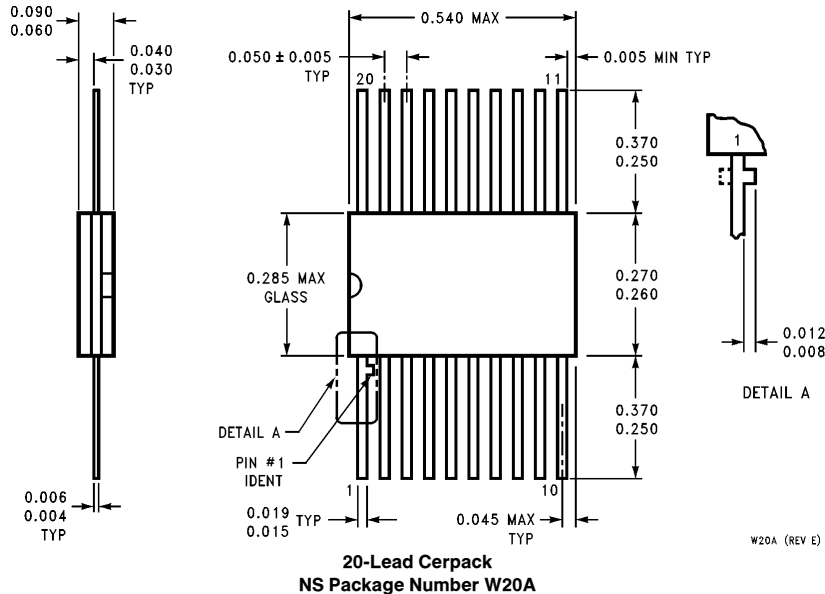
20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number MD20D



N20A (REV G)

20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A



Physical Dimensions inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livny-Gargan-Str. 10
D-82256 Fürstentfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527849
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihamu-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brasil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.