

## 54FCT377

### Octal D-Type Flip-Flop with Clock Enable

#### General Description

The 'FCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ( $\overline{CE}$ ) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The  $\overline{CE}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

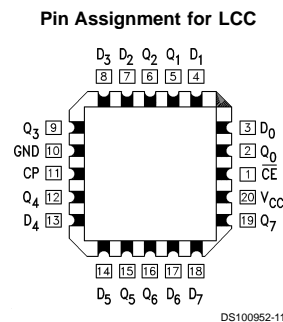
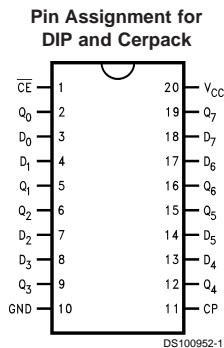
#### Features

- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'FCT273 for master reset version
- See 'FCT373 for transparent latch version
- See 'FCT374 for TRI-STATE® version
- TTL input and output level compatible
- CMOS power consumption
- Output sink capability of 32 mA, source capability of 12 mA
- Standard Microcircuit Drawing (SMD) 5962-8762701

#### Ordering Code

Military	Package Number	Package Description
54FCT377DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT377FMQB	W20A	20-Lead Cerpack
54FCT377LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

#### Connection Diagram



Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse Input
Q <sub>0</sub> –Q <sub>7</sub>	Data Outputs

## Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	$\overline{CE}$	$D_n$	$Q_n$
Load "1"		L	h	H
Load "0"		L	L	L
Hold		h	X	No Change
(Do Nothing)	X	H	X	No Change

H = HIGH Voltage Level

h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition

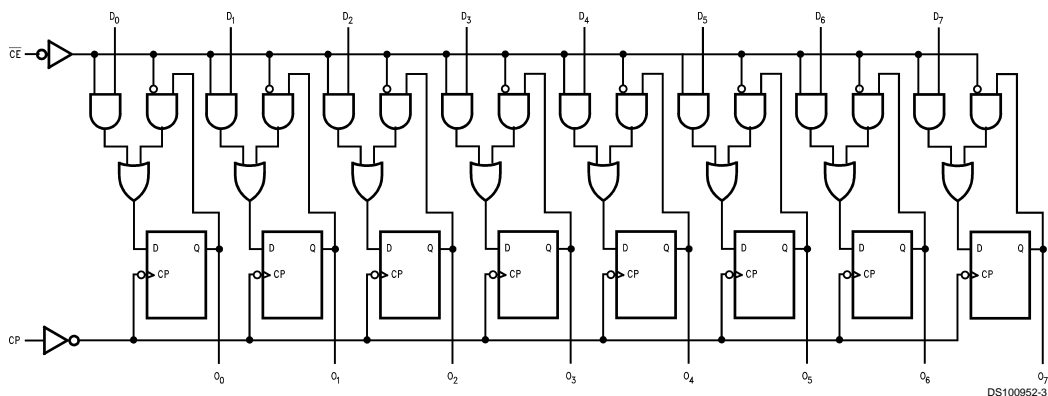
L = LOW Voltage Level

L = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition

X = Immaterial

= LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	
Ceramic	–55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	–0.5V to +4.75V
in the HIGH State	–0.5V to V <sub>CC</sub>

Current Applied to Output in LOW State (Max)	Twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current (Across Comm Operating Range)	–500 mA

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	–55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

**DC Electrical Characteristics**

Symbol	Parameter	FCT377			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54FCT	4.3		V	Min	I <sub>OH</sub> = –300 uA
		54FCT	2.4				I <sub>OH</sub> = –12 mA
V <sub>OL</sub>	Output LOW Voltage	54FCT		0.2	V	Min	I <sub>OL</sub> = 300 uA
		54FCT		0.5			I <sub>OL</sub> = 32mA
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>IL</sub>	Input LOW Current			–5	μA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	–60			mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CCQ</sub>	Quiescent Power Supply Current			1.5	mA	Max	V <sub>I</sub> = 0.2V or V <sub>I</sub> = 5.3V, V <sub>CC</sub> = 5.5V
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> /Input			2.0	mA	Max	V <sub>I</sub> = V <sub>CC</sub> – 2.1V Data Input V <sub>I</sub> = V <sub>CC</sub> – 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub>			0.4	mA/ MHz	Max	Outputs Open One bit Toggling, 50% Duty Cycle
I <sub>CC</sub>	Total Power Supply Current			6.0	mA	Max	V <sub>CC</sub> = 5.5V, Outputs Open, f <sub>CP</sub> = 10MHz, 50% Duty Cycle, One bit Toggling at f <sub>I</sub> = 5 MHz, 50% Duty Cycle

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## AC Electrical Characteristics

Symbol	Parameter	54FCT		Units	Fig. No.
		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.0	15.0	ns	Figure 4
t <sub>PHL</sub>	CP to O <sub>n</sub>	2.0	8.3		

## AC Operating Requirements

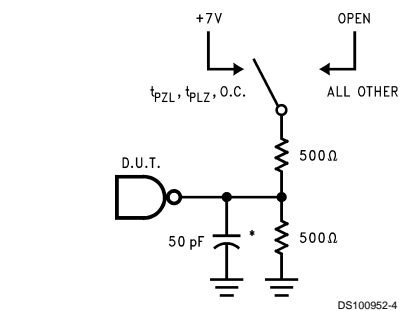
Symbol	Parameter	54FCT		Units	Fig. No.
		$T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max		
$t_s(\text{H})$	Setup Time, HIGH	4.0		ns	Figure 6
$t_s(\text{L})$	or LOW $D_n$ to CP	4.0			
$t_h(\text{H})$	Hold Time, HIGH	2.5		ns	Figure 6
$t_h(\text{L})$	or LOW $D_n$ to CP	2.5			
$t_s(\text{H})$	Setup Time, HIGH	4.5		ns	Figure 6
$t_s(\text{L})$	or LOW $\overline{CE}$ to CP	4.5			
$t_h(\text{H})$	Hold Time, HIGH	2.0		ns	Figure 6
$t_h(\text{L})$	or LOW $\overline{CE}$ to CP	2.0			
$t_w(\text{H})$	Pulse Width, CP,	7.0		ns	Figure 5
$t_w(\text{L})$	HIGH or LOW	7.0			

## Capacitance

Symbol	Parameter	Max	Units	Conditions
$C_{IN}$	Input Capacitance	10	pF	$V_{CC} = 0\text{V}$ , $T_A = 25^{\circ}\text{C}$
$C_{OUT}$ (Note 3)	Output Capacitance	12	pF	$V_{CC} = 5.0\text{V}$

**Note 3:**  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883B, Method 3012.

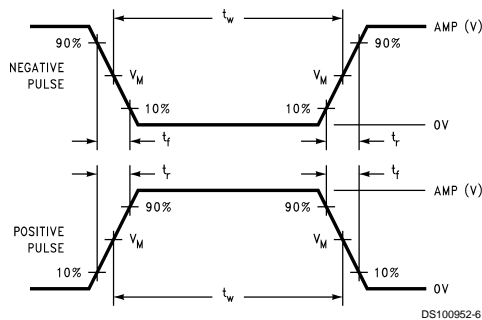
## AC Loading



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\*Includes jig and probe capacitance

**FIGURE 1. Standard AC Test Load**



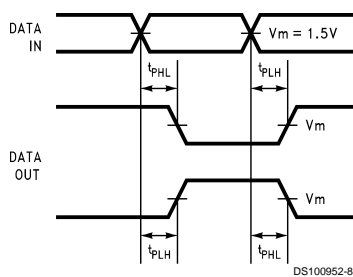
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**FIGURE 2.  $V_M = 1.5V$**

### Input Pulse Requirements

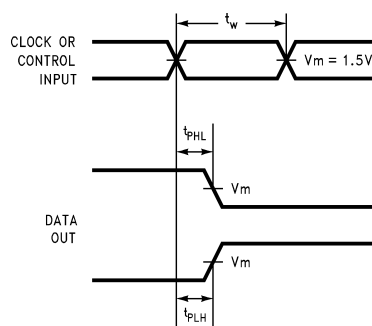
Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

**FIGURE 3. Test Input Signal Requirements**



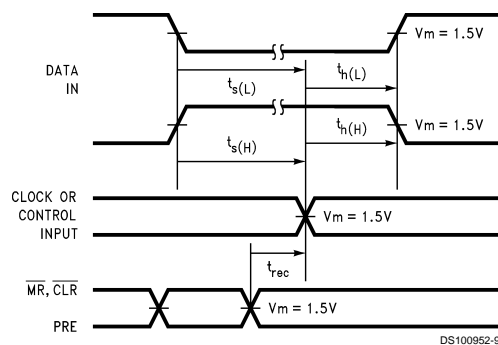
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**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



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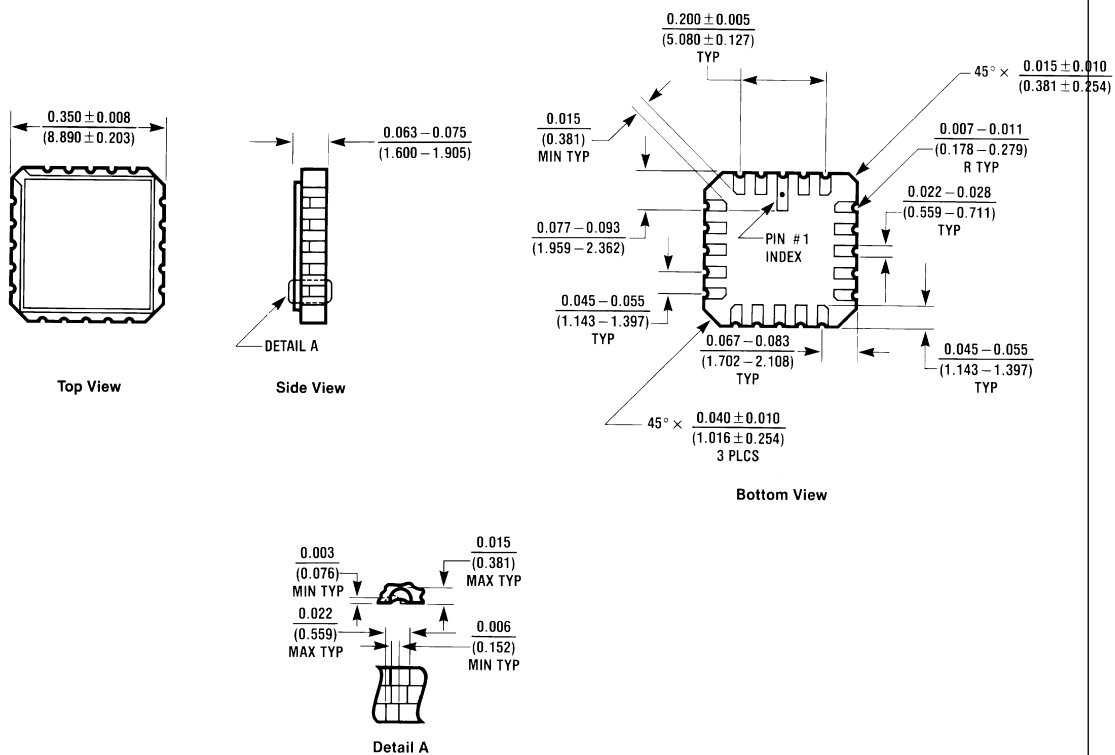
**FIGURE 5. Propagation Delay, Pulse Width Waveforms**



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**FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms**

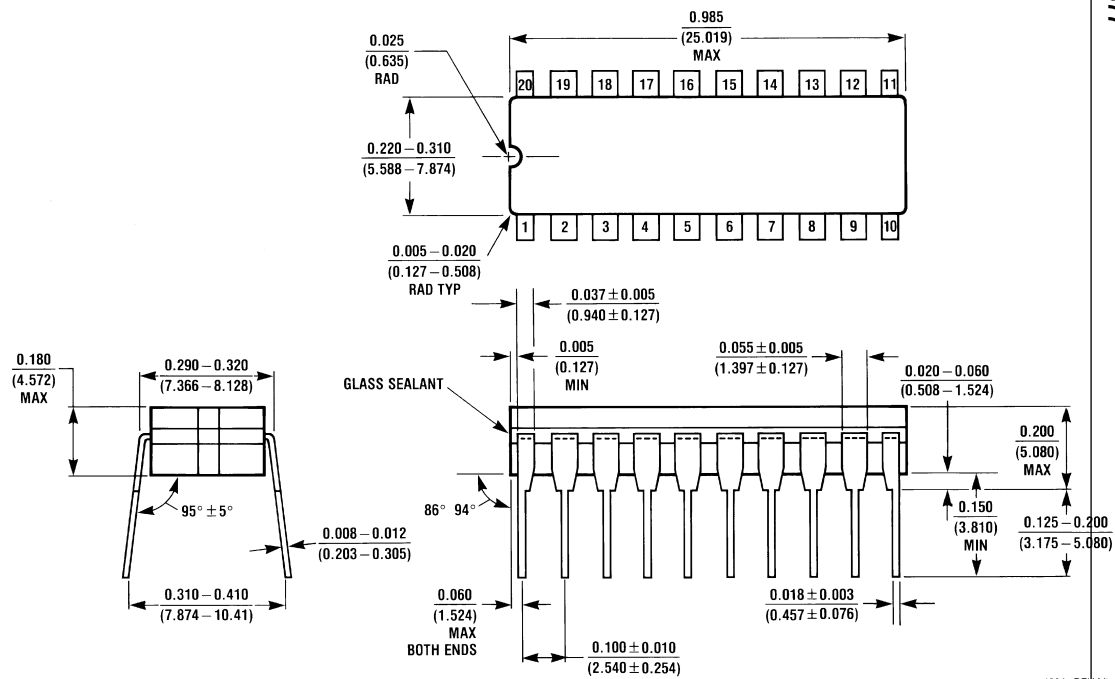
# Physical Dimensions inches (millimeters) unless otherwise noted



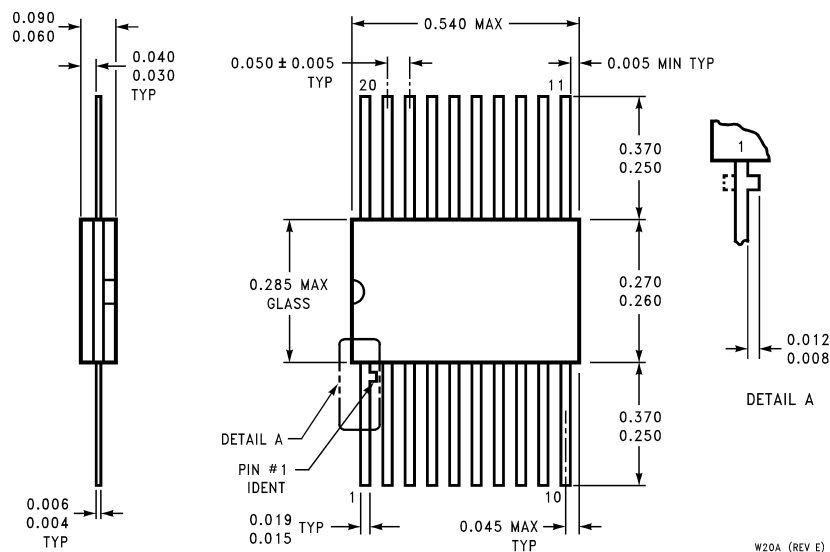
**20-Lead Ceramic Chip Carrier  
NS Package Number E20A**

E20A (REV D)

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Dual-In-Line Package**  
**NS Package Number J20A**



**20-Lead Ceramic Flatpack**  
**NS Package Number W20A**

## Notes

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