

54ABT373

Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 54ABT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Features

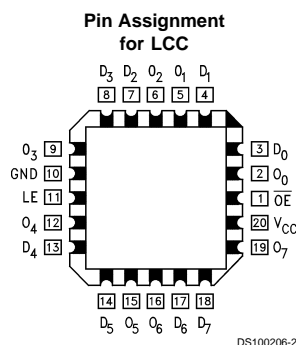
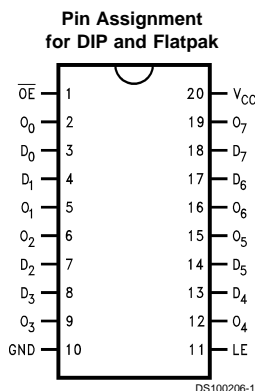
- TRI-STATE outputs for bus interfacing
- Output sink capability of 48 mA, source capability of 24 mA

- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9321801

Ordering Code

Military	Package Number	Package Description
54ABT373J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT373W-QML	W20A	20-Lead Cerpack
54ABT373E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams



Pin Names	Description
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
O ₀ –O ₇	TRI-STATE Latch Outputs

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54ABT373 Octal Transparent Latch with TRI-STATE Outputs

Functional Description

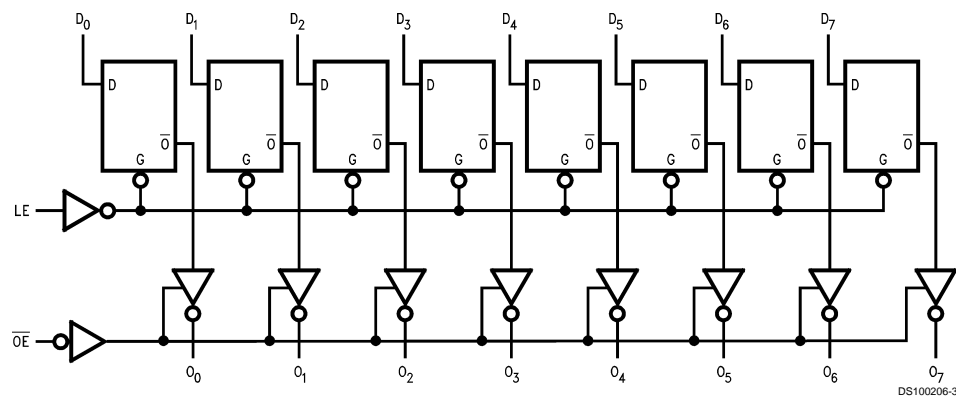
The 'ABT373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	\overline{OE}	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance State

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	
Ceramic	–55°C to +175°C
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	–0.5V to +5.5V
in the HIGH State	–0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Over Voltage Latchup (I/O)

10V

Recommended Operating Conditions

Free Air Ambient Temperature	–55°C to +125°C
Military	
Supply Voltage	+4.5V to +5.5V
Military	
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT373			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA
V _{OH}	Output HIGH Voltage	54ABT 2.5			V	Min	I _{OH} = –3 mA I _{OH} = –24 mA
V _{OL}	Output LOW Voltage	54ABT 2.0			V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V (Note 4) V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current		–5		μA	Max	V _{IN} = 0.5V (Note 4) V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current		50		μA	0 – 5.5V	V _{OUT} = 2.7V; \overline{OE} = 2.0V
I _{OZL}	Output Leakage Current		–50		μA	0 – 5.5V	V _{OUT} = 0.5V; \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current	–100	–275		mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current		50		μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		30		mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		50		μA	Max	\overline{OE} = V _{CC} All Others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input		2.5		mA		V _I = V _{CC} – 2.1V
	Outputs Enabled		2.5		mA	Max	Enable Input V _I = V _{CC} – 2.1V
	Outputs TRI-STATE		2.5		mA		Data Input V _I = V _{CC} – 2.1V
	Outputs TRI-STATE		2.5		mA		All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 4)		0.12		mA/ MHz	Max	Outputs Open, LE = V _{CC} \overline{OE} = GND, (Note 3) One Bit Toggling, 50% Duty Cycle

Note 3: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		$T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	
t_{PLH}	Propagation Delay	1.0	6.8	ns
t_{PHL}	D_n to O_n	1.0	7.0	
t_{PLH}	Propagation Delay	1.0	7.7	ns
t_{PHL}	LE to O_n	1.5	7.7	
t_{PZH}	Output Enable Time	1.0	6.7	ns
t_{PZL}		1.5	7.2	
t_{PHZ}	Output Disable Time	1.7	8.0	ns
t_{PLZ}		1.0	7.0	

AC Operating Requirements

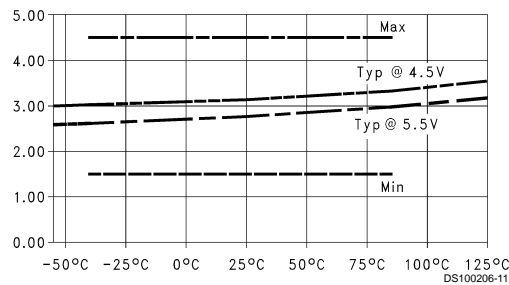
Symbol	Parameter	54ABT		Units
		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		
		Min	Max	
t _s (H)	Setup Time, HIGH	2.5		ns
t _s (L)	or LOW D _n to LE	2.5		
t _h (H)	Hold Time, HIGH	2.5		ns
t _h (L)	or LOW D _n to LE	2.5		
t _w (H)	Pulse Width, LE HIGH	3.3		ns

Capacitance

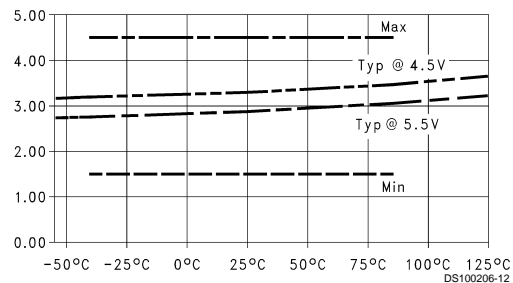
Symbol	Parameter	Typ	Units	Conditions ($T_A = 25^{\circ}\text{C}$)
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 5)	Output Capacitance	9	pF	$V_{CC} = 5.0\text{V}$

Note 5: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 Data to Output



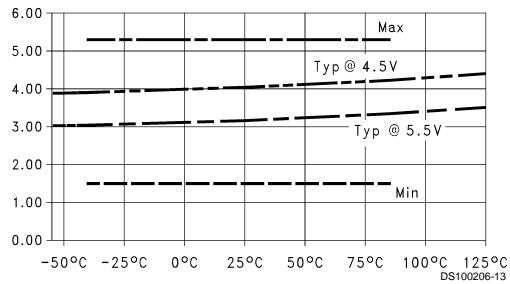
t_{PHL} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 Data to Output



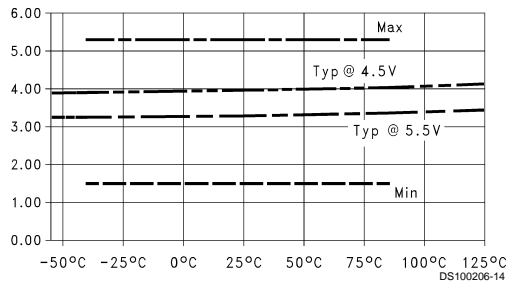
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

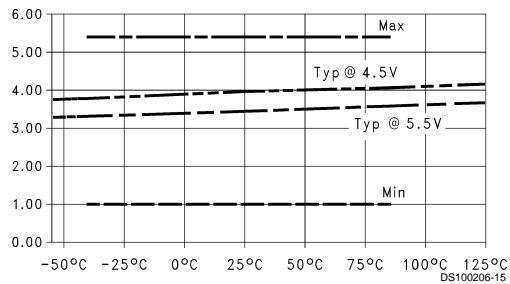
t_{PZH} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
OE to Output



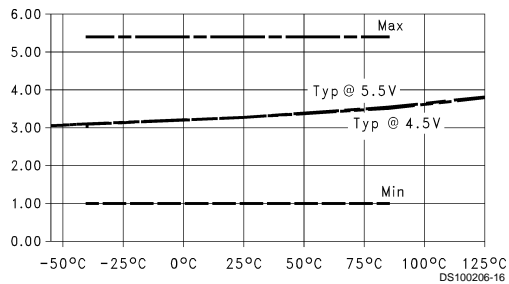
t_{PZL} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
OE to Output



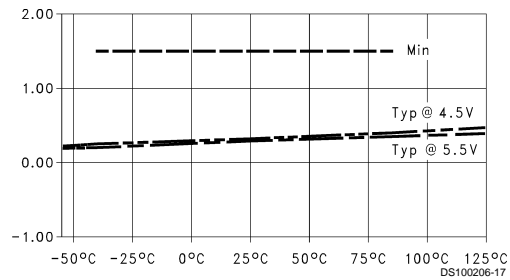
t_{PHZ} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
OE to Output



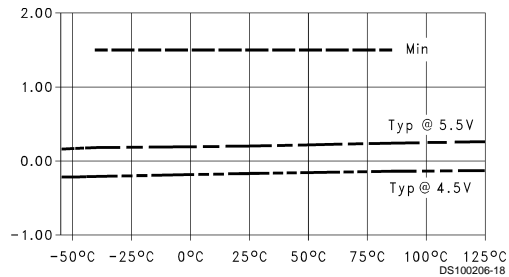
t_{PLZ} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
OE to Output



$t_{SET \text{ LOW}}$ vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
Data to LE



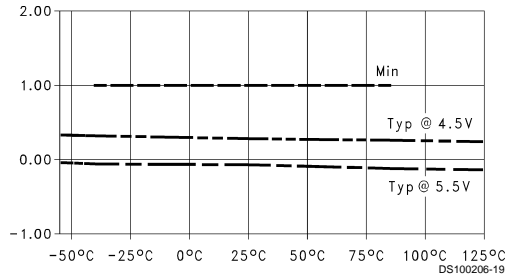
$t_{SET \text{ HIGH}}$ vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
Data to LE



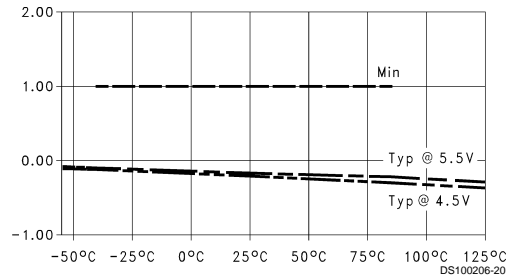
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

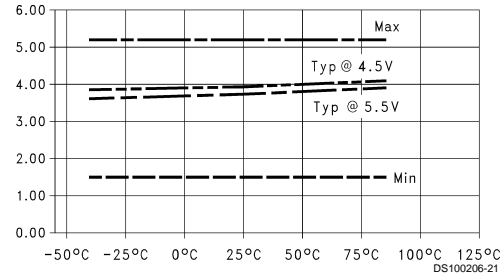
$t_{\text{HOLD HIGH}}$ vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
Data to LE



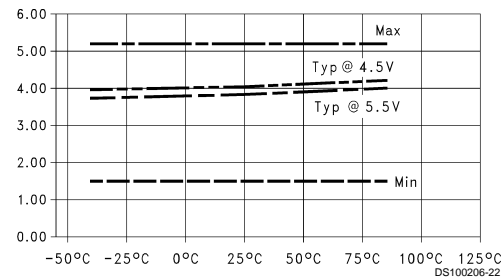
$t_{\text{HOLD LOW}}$ vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 1 Output Switching
Data to LE



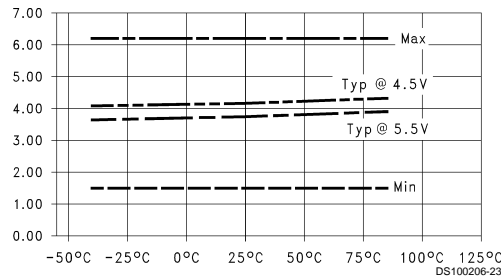
t_{PLH} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 8 Outputs Switching
Data to Output



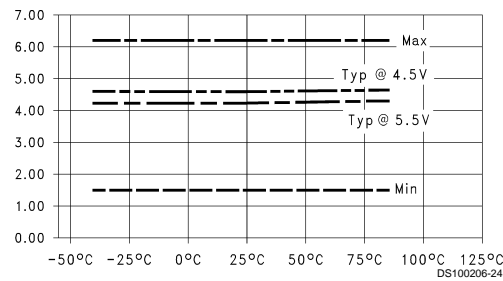
t_{PHL} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 8 Outputs Switching
Data to Output



t_{PZH} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 8 Outputs Switching
OE to Output



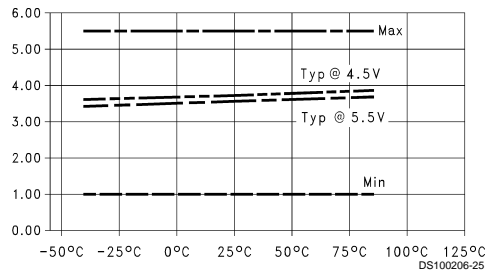
t_{PZL} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 8 Outputs Switching
OE to Output



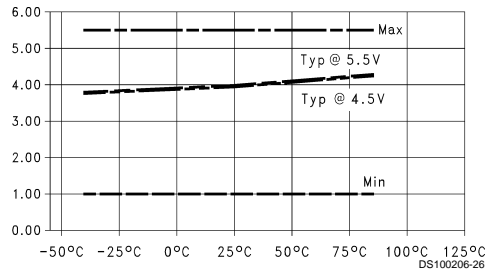
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

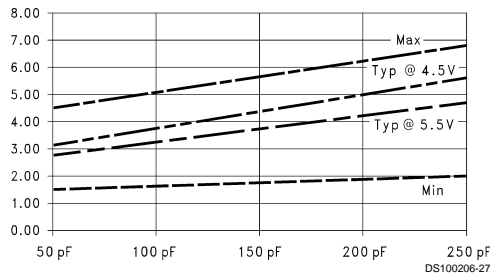
t_{PHZ} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 8 Outputs Switching
 OE to Output



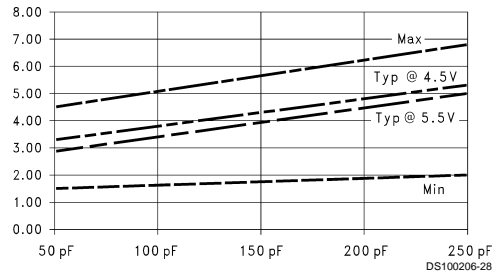
t_{PLZ} vs Temperature (T_A)
 $C_L = 50 \text{ pF}$, 8 Outputs Switching
 OE to Output



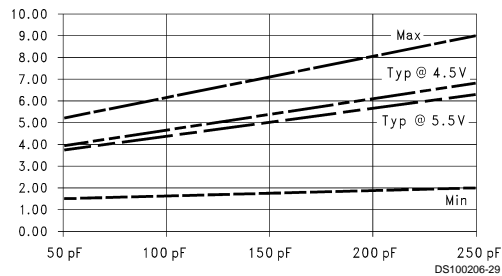
t_{PLH} vs Load Capacitance
 $T_A = 25^\circ\text{C}$, 1 Output Switching
 Data to Output



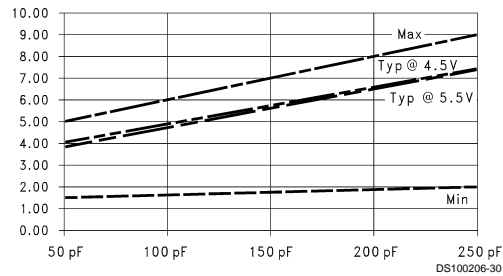
t_{PLH} vs Load Capacitance
 $T_A = 25^\circ\text{C}$, 1 Output Switching
 Data to Output



t_{PLH} vs Load Capacitance
 $T_A = 25^\circ\text{C}$, 8 Outputs Switching
 Data to Output



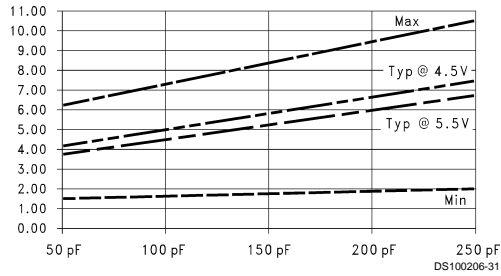
t_{PLH} vs Load Capacitance
 $T_A = 25^\circ\text{C}$, 8 Outputs Switching
 Data to Output



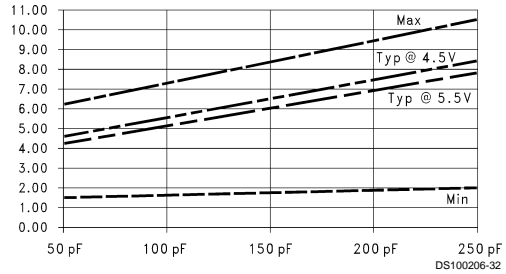
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

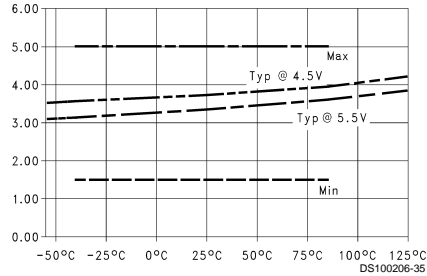
t_{PZH} vs Load Capacitance
 $T_A = 25^\circ\text{C}$, 8 Outputs Switching
 OE to Output



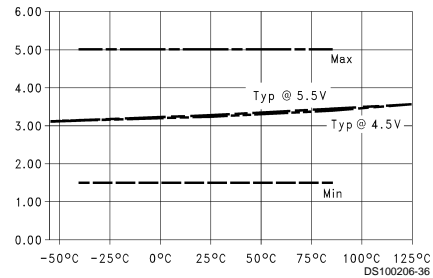
t_{PZL} vs Load Capacitance
 $T_A = 25^\circ\text{C}$, 8 Outputs Switching
 OE to Output



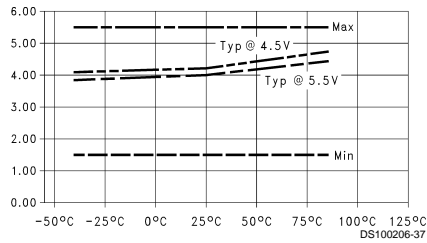
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 LE to Output



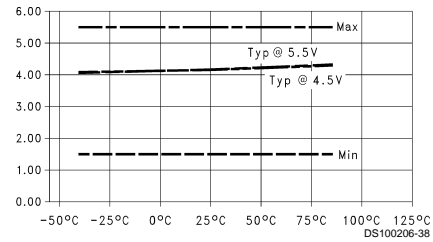
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 LE to Output



t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 LE to Output



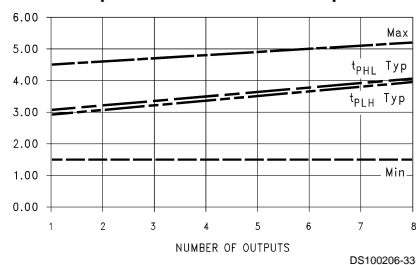
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 LE to Output



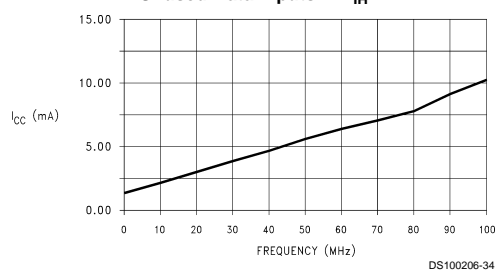
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

t_{PLH} and t_{PHL} vs Number Outputs Switching
 $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$,
 Outputs In Phase Data to Output

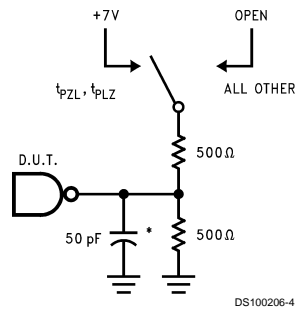


Typical I_{CC} vs Output Switching Frequency
 $C_L = 0 \text{ pF}$, $V_{CC} = V_{IH} = 5.5\text{V}$, $LE = \text{GND}$,
 1 Output Switching at 50% Duty Cycle
 Data to Output, Transparent Mode with
 Unused Data Inputs = V_{IH}



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

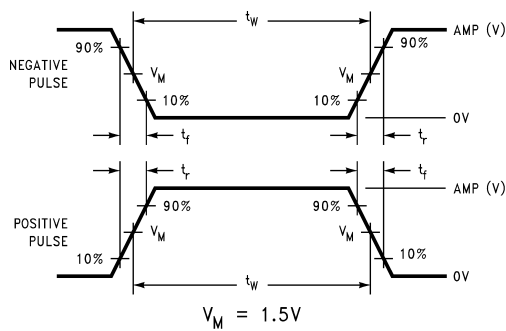


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

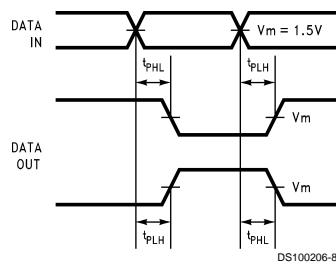


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

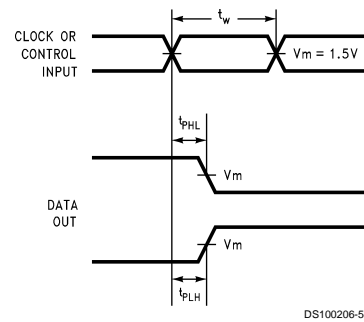


FIGURE 5. Propagation Delay, Pulse Width Waveforms

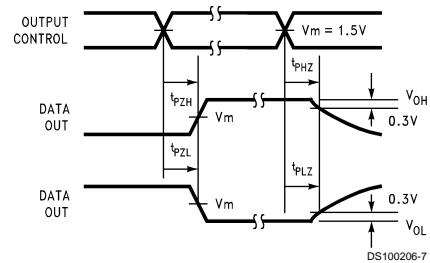


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

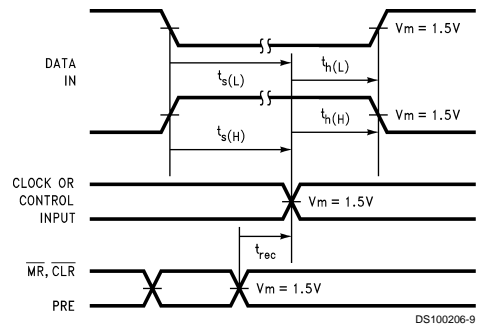
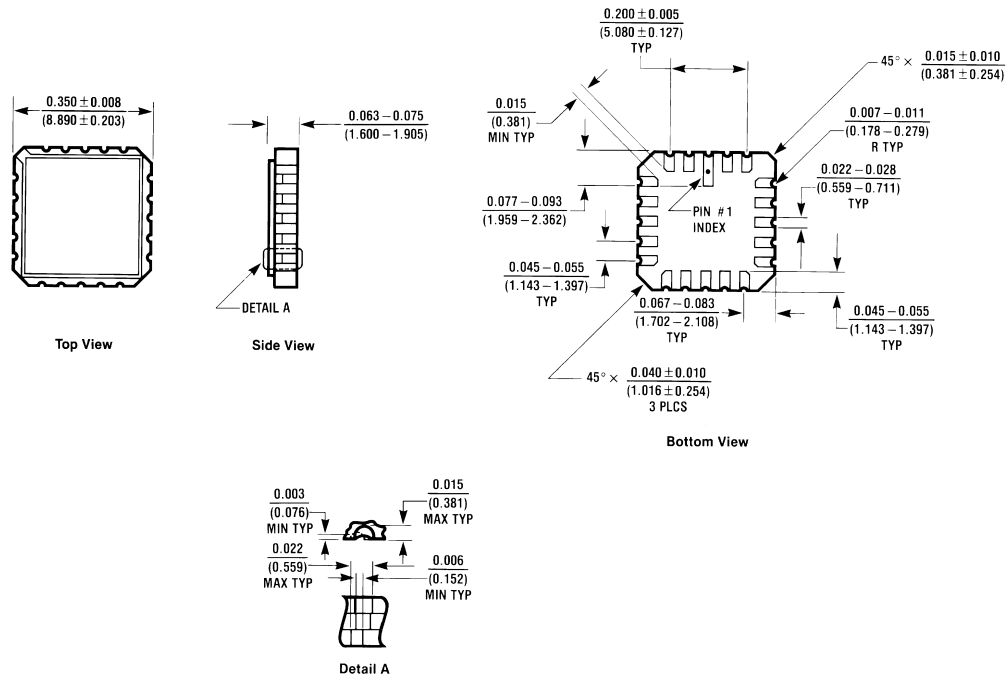


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms



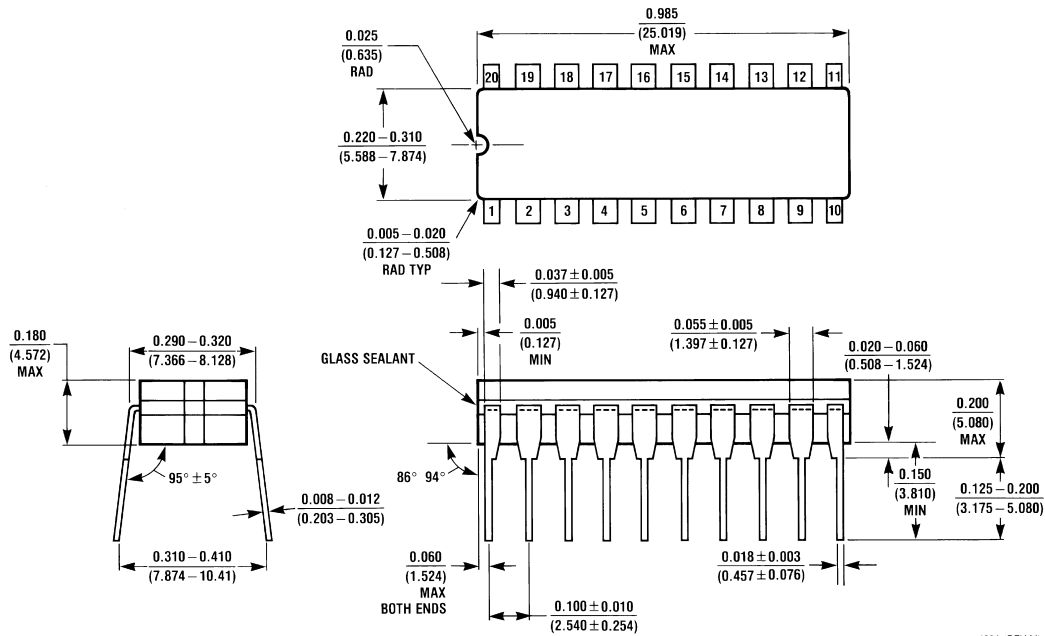
Physical Dimensions inches (millimeters) unless otherwise noted



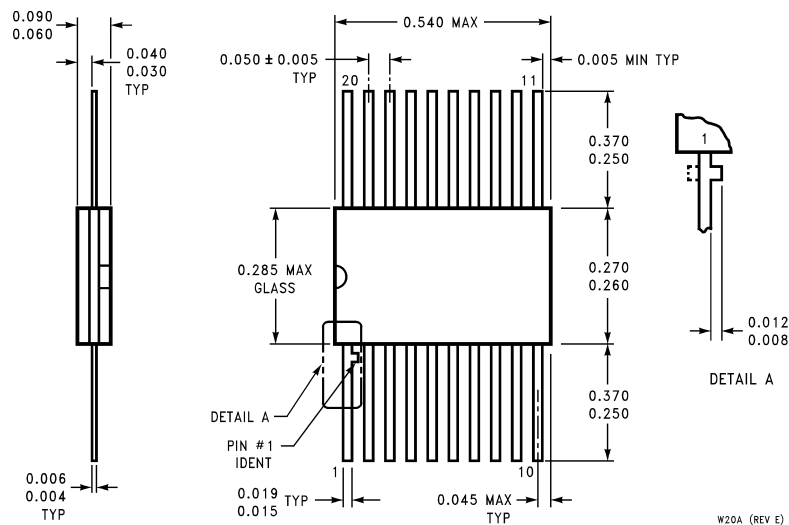
E20A (REV D)

20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Dual-In-Line (D)
NS Package Number J20A



20-Lead Ceramic Flatpak (F)
NS Package Number W20A



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