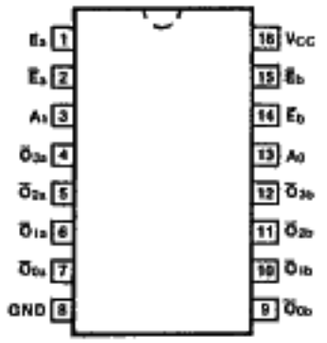
T-66-21-53

54/74156
54LS/74LS156

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

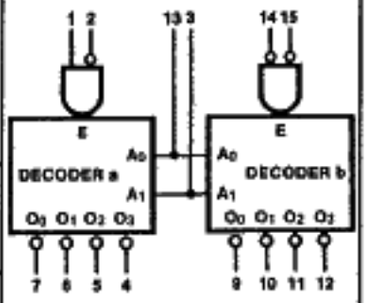
(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '156 contains two decoders with common Address (A_0, A_1) inputs and separate enable gates. Decoder "a" has an enable gate with one active HIGH and one active LOW input, while decoder "b" has two active LOW inputs. If the enable functions are satistied, one output of each decoder will be LOW, as selected by the Address inputs. For functional description, truth table and logic diagram, please refer to the '155 data sheet.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74156PC, 74LS156PC		9B
Ceramic DIP (D)	A	74156DC, 74LS156DC	54156DM, 54LS156DM	6B
Flatpak (F)	A	74156FC, 74LS156FC	54156FM, 54LS156FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Address Inputs	1.0/1.0	0.5/0.25
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
E_a	Enable Input (Active HIGH)	1.0/1.0	0.5/0.25
$\overline{O}_0$ — $\overline{O}_3$	Outputs (Active LOW)	OC*/10	OC*/5.0 (2.5)

*OC— Open Collector

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OH}	Output HIGH Current, OFF State			250		100	μA	V_{CC}=Min, V_{OH} = 5.5 V
I_{CC}	Power Supply Current	XM		35		10	mA	V_{CC}=Max; $\overline{E}_a$, E_b = GND
		XC		40		10		A_0, A_1, E_a=4.5 V

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	54/74LS C_L = 15 pF, R_L = 2 kΩ Min	54/74LS C_L = 15 pF, R_L = 2 kΩ Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		34 34		28 33	ns	Figs. 3-2, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$ or $\overline{E}_b$ to $\overline{O}_n$		23 30		25 30	ns	Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay E_a to $\overline{O}_n$		27 33		34 34	ns	Figs. 3-2, 3-4

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