

CLC952

12-bit, 41MSPS Monolithic A/D Converter

General Description

The CLC952 is a complete monolithic 12-bit 41MSPS analog-to-digital converter system. Fabricated from a 0.8 μ m BiCMOS process, the CLC952's on-chip features include a very linear wideband track-and-hold, bandgap voltage reference and a proprietary 12-bit multi-stage quantizer. The CLC952 has been designed for wideband digital communications receivers and features a 72dBc spurious-free dynamic range (SFDR) and 64dB signal-to-noise ratio (SNR).

The CLC952 operates from a standard ± 5 V power supply and features excellent noise isolation with its >60dB power-supply rejection ratio (PSRR). All digital control functions and output registers are TTL compatible. The CLC952AC operates over the commercial temperature range (0°C to 70°C), and the CLC952AJ operates over the industrial temperature range (-40°C to 85°C) version. The CLC952 is available in a 28-pin SSOP that provides an extremely small footprint for reduced board space. National Semiconductor thoroughly tests each part to verify full compliance with guaranteed specifications.

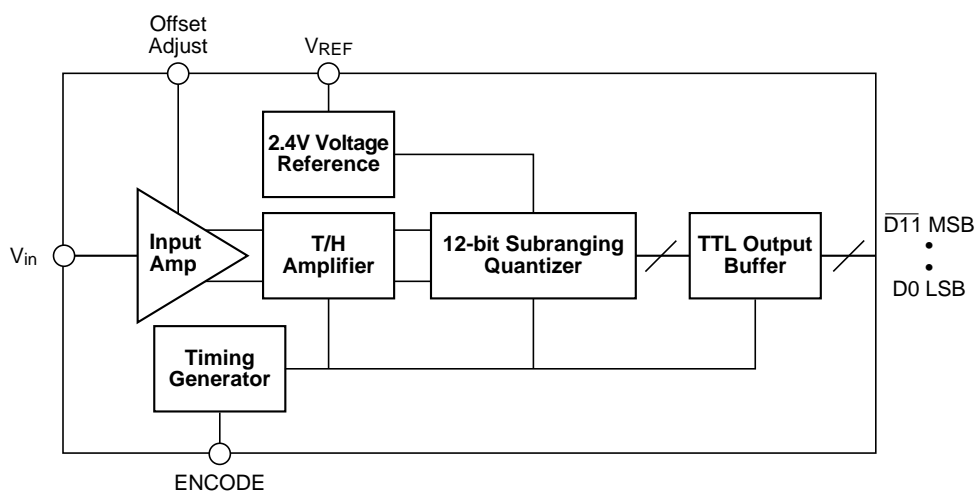
Features

- 41MSPS
- Wide dynamic range
SFDR: 72dBc
SNR: 64dB
- Low power dissipation: 660mW
- Ground centered,
DC-coupled analog input
- Excellent PSRR: >60dB
- Very small package: 28-pin SSOP
- Low cost

Applications

- Cellular base-stations
- Digital communications
- Infrared/CCD imaging
- IF sampling
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

CLC952
Block Diagram



CLC952 Electrical Characteristics (V_{CC} = +5V, V_{EE} = -5V, 40.96MSPS; unless specified)

| PARAMETERS | CONDITIONS | TEMP | RATINGS | | | UNITS | NOTES |
|---|---------------------------------|--------|---------|------|-------|-----------|-------|
| | | Note 4 | MIN | TYP | MAX | | |
| DYNAMIC PERFORMANCE | | | | | | | |
| small-signal bandwidth | V _{in} = 1/4FS | +25°C | | 185 | | MHz | |
| large-signal bandwidth | V _{in} = FS | +25°C | | 180 | | MHz | |
| slew rate | | +25°C | | 357 | | V/μs | |
| overvoltage recovery time | V _{in} = 1.5FS (0.01%) | +25°C | | 5 | | ns | |
| effective aperture delay | | +25°C | | 1.6 | | ns | |
| aperture jitter | | +25°C | | 4 | | ps(rms) | |
| NOISE AND DISTORTION (40.96MSPS) | | | | | | | |
| signal-to-noise ratio (w/o harmonics) | | | | | | | |
| 2.0MHz | FS | +25°C | 60 | 64 | | dB | 1 |
| | FS | Full | | 61 | | dB | |
| 9.67MHz | FS | +25°C | 60 | 64 | | dB | 1 |
| | FS | Full | | 61 | | dB | |
| 19.5MHz | FS | +25°C | 60 | 62 | | dB | 1 |
| | FS | Full | | 60 | | dB | |
| spurious-free dynamic range | | | | | | | |
| 2.0MHz | FS-1dB | +25°C | 64 | 72 | | dBc | 1 |
| | FS-1dB | Full | | 71 | | dBc | |
| 9.67MHz | FS-1dB | +25°C | 61 | 69 | | dBc | 1 |
| | FS-1dB | Full | | 68 | | dBc | |
| 19.5MHz | FS-1dB | +25°C | 60 | 67 | | dBc | 1 |
| | FS-1dB | Full | | 66 | | dBc | |
| intermodulation distortion | | | | | | | |
| 19.49MHz (f ₁), 19.9MHz (f ₂) | FS-7dB | +25°C | | 75 | | dBFS | |
| DC ACCURACY AND PERFORMANCE | | | | | | | |
| differential non-linearity | DC; FS | +25°C | | 1.4 | | LSB | |
| integral non-linearity | DC; FS | +25°C | | 3.0 | | LSB | |
| bipolar offset error | | +25°C | | 5.1 | | mV | |
| bipolar offset error | | Full | | | 25.0 | mV | 3 |
| bipolar gain error | | +25°C | | -4.5 | | %FS | |
| bipolar gain error | | Full | | | 15.0 | %FS | 3 |
| ANALOG INPUT AND PERFORMANCE | | | | | | | |
| analog input resistance | | +25°C | | 500 | | Ω | |
| analog input capacitance | | +25°C | | 2 | | pF | |
| DIGITAL INPUTS | | | | | | | |
| input voltage | logic LOW | Full | | | 0.8 | V | 1,3 |
| | logic HIGH | Full | 2.0 | | | V | 1,3 |
| input current | logic LOW | Full | | 0 | 5 | μA | 1,3 |
| | logic HIGH | Full | | 4.0 | 25 | μA | 1,3 |
| output voltage | logic LOW | Full | | | 0.8 | V | 1,3 |
| | logic HIGH | Full | 2.4 | | | V | 1,3 |
| TIMING | | | | | | | |
| maximum conversion rate | | Full | | | 40.96 | MSPS | 1,3 |
| minimum conversion rate | | Full | | 3.0 | | MSPS | 3 |
| pulse width high | | Full | | 12.2 | 15 | ns | 3 |
| pulse width low | | Full | 10.5 | 12.2 | | ns | 3 |
| pipeline delay | | Full | | | 1.0 | clk cycle | 3 |
| output propagation delay | | +25°C | | 15 | | ns | |
| POWER REQUIREMENTS | | | | | | | |
| +5V supply current | 41MSPS | +25°C | | 54 | 70 | mA | 1 |
| +5V supply current | 41MSPS | Full | | | 70 | mA | 3 |
| -5V supply current | 41MSPS | +25°C | | 78 | 100 | mA | 1 |
| -5V supply current | 41MSPS | Full | | | 100 | mA | 3 |
| nominal power dissipation | 41MSPS | +25°C | | 660 | | mW | |
| V _{EE} power supply rejection ratio | | +25°C | | 72 | | dB | |
| V _{CC} power supply rejection ratio | | +25°C | | 60 | | dB | |

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

- 1) These parameters are 100% tested at 25°C.
- 2) Typical specifications are the mean values of the distributions of deliverable converters tested to date.
- 3) Min/max data over temperature is based on the 5 sigma limit for deliverable converters tested to date.
- 4) Full temperature range is 0°C to +70°C for AC, -40°C to +85°C for AJ.

Absolute Maximum Ratings

| | |
|---|----------------------|
| positive supply voltage (V_{CC}) | -0.5V to +6V |
| negative supply voltage (V_{EE}) | +0.5V to -6V |
| differential voltage between any two grounds | <200mV |
| analog input voltage range | V_{EE} to V_{CC} |
| digital input voltage range | -0.5V to + V_{CC} |
| output short circuit duration (one-pin to ground) | infinite |
| junction temperature | 175°C |
| storage temperature range | -65°C to 150°C |
| lead solder duration (+300°C) | 10sec |

Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

| | |
|--|----------------|
| positive supply voltage (V_{CC}) | +5V \pm 5% |
| negative supply voltage (V_{EE}) | -5V \pm 5% |
| differential voltage between any two grounds | <10mV |
| analog input voltage range | \pm 0.5V |
| operating temperature range (AC) | 0°C to +70°C |
| operating temperature range (AJ) | -40°C to +85°C |

Package Thermal Resistance

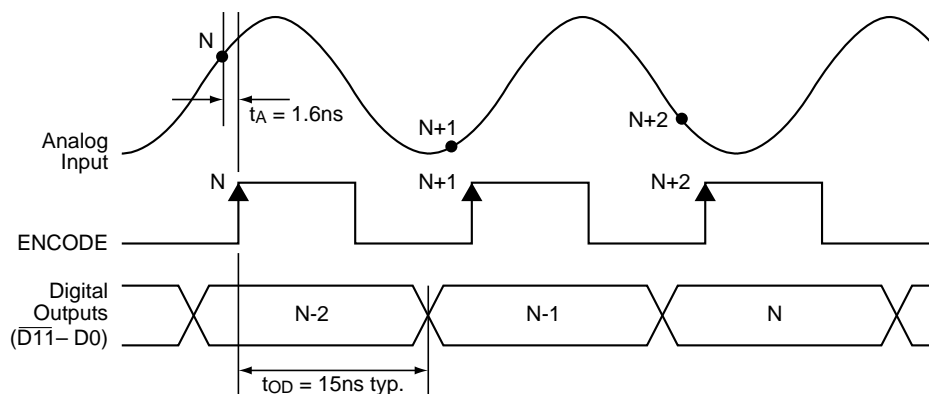
| Package | θ_{JA} | θ_{JC} |
|-------------|---------------|---------------|
| 28-pin SSOP | 80°C/W | 32°C/W |

Reliability Information

| | |
|------------------|------|
| Transistor count | 3000 |
|------------------|------|

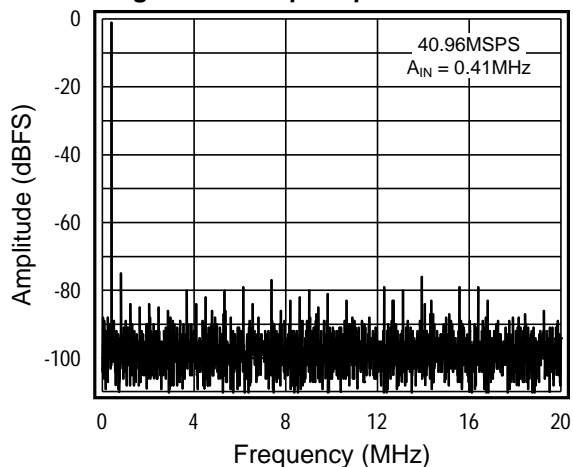
Ordering Information

| Model | Temperature Range | Description |
|-------------|-------------------|---|
| CLC952ACMSA | 0°C to +70°C | 28-pin SSOP (commercial part) |
| CLC952AJMSA | -40°C to +85°C | 28-pin SSOP (industrial part) |
| CLC952PCASM | | Fully loaded evaluation board with CLC952 ... ready for test. |

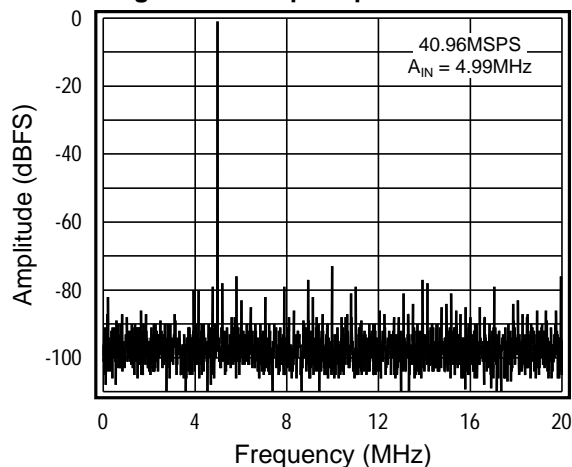


CLC952 Timing Diagram

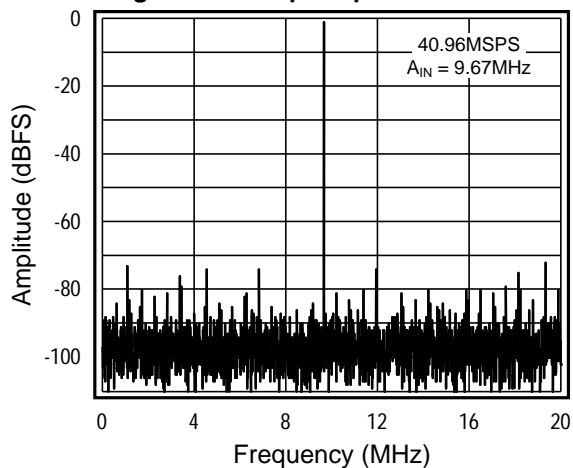
Single Tone Output Spectrum



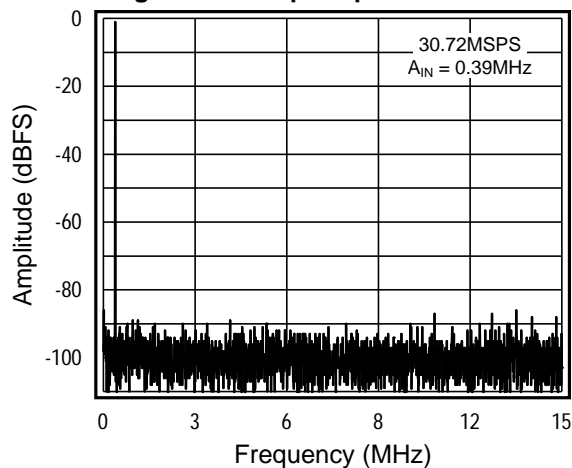
Single Tone Output Spectrum



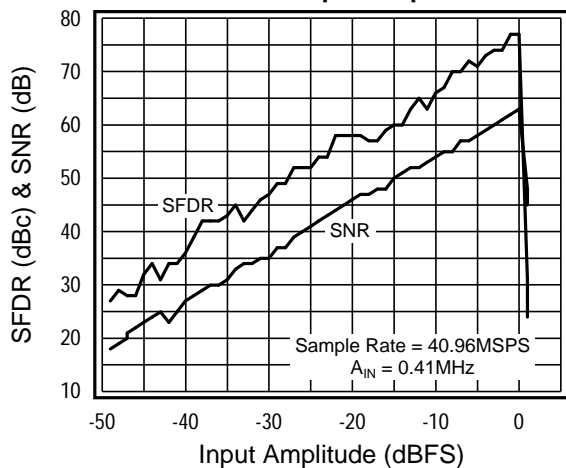
Single Tone Output Spectrum



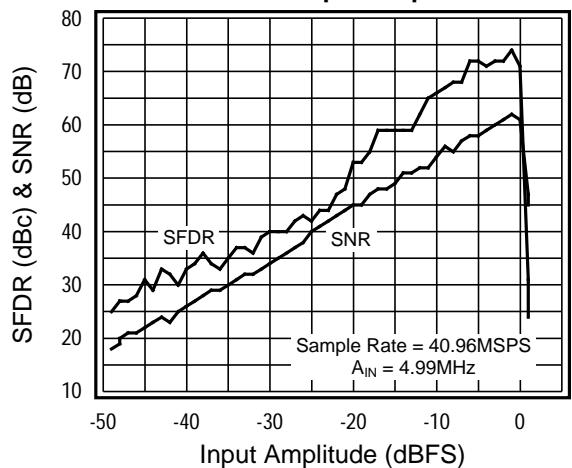
Single Tone Output Spectrum

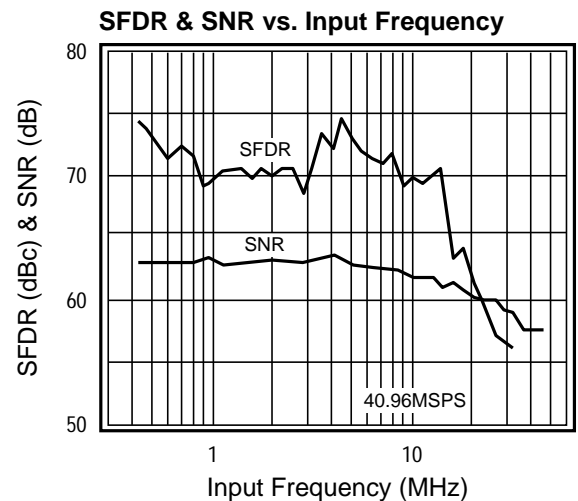
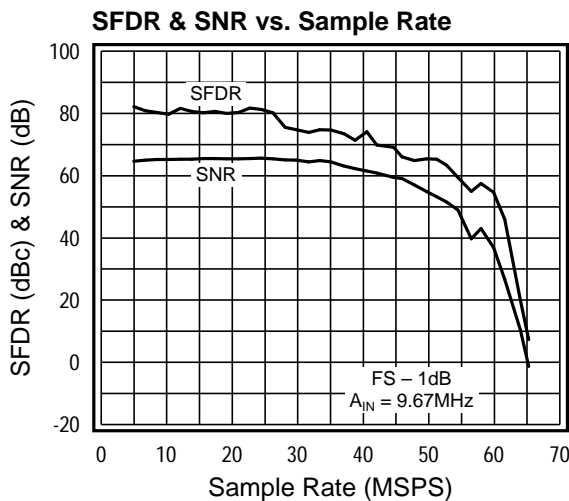
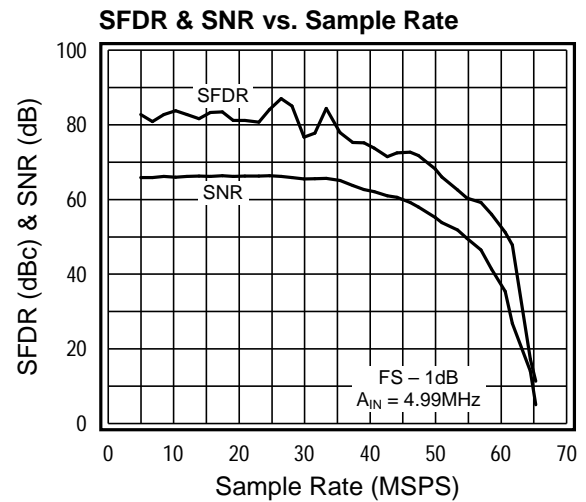
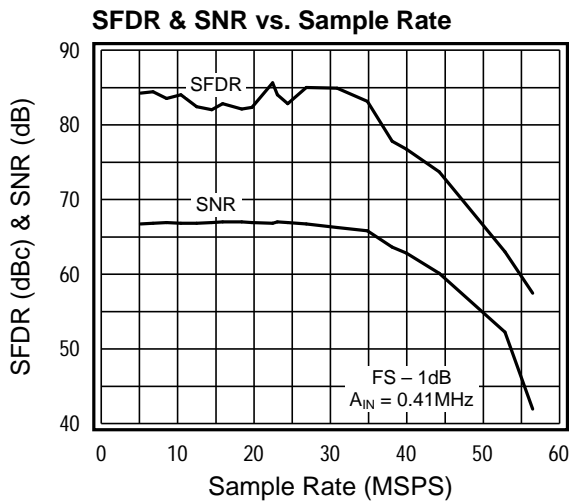
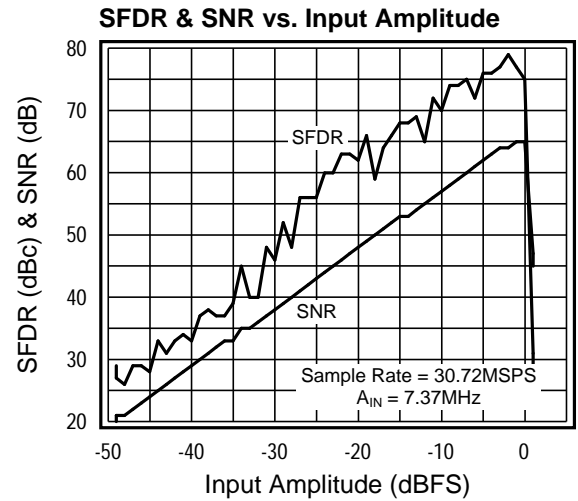
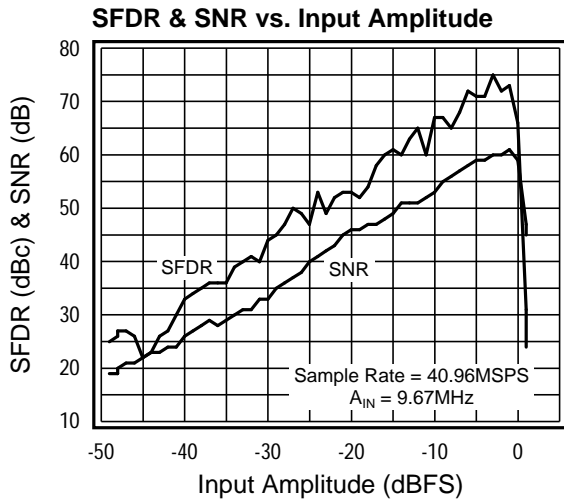


SFDR & SNR vs. Input Amplitude

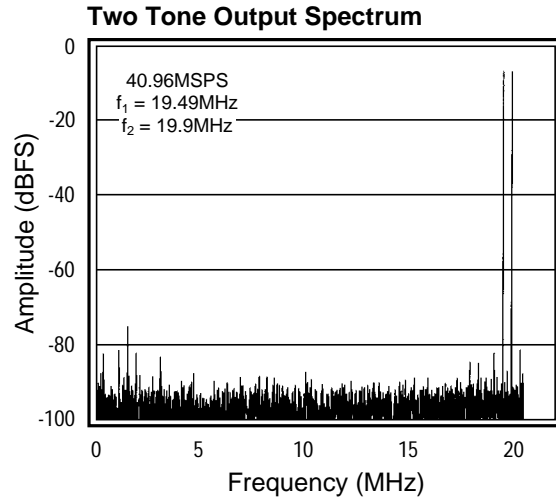
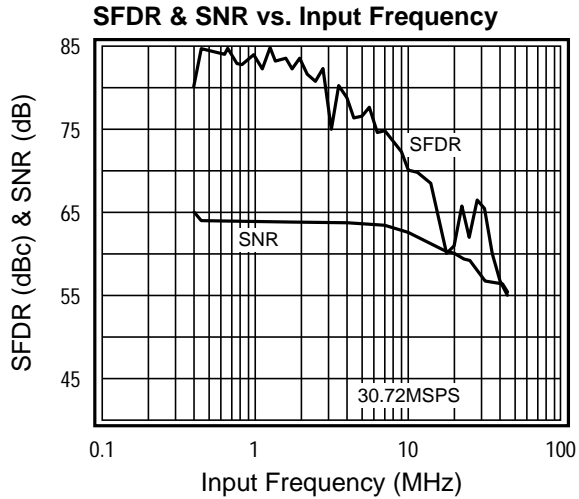


SFDR & SNR vs. Input Amplitude

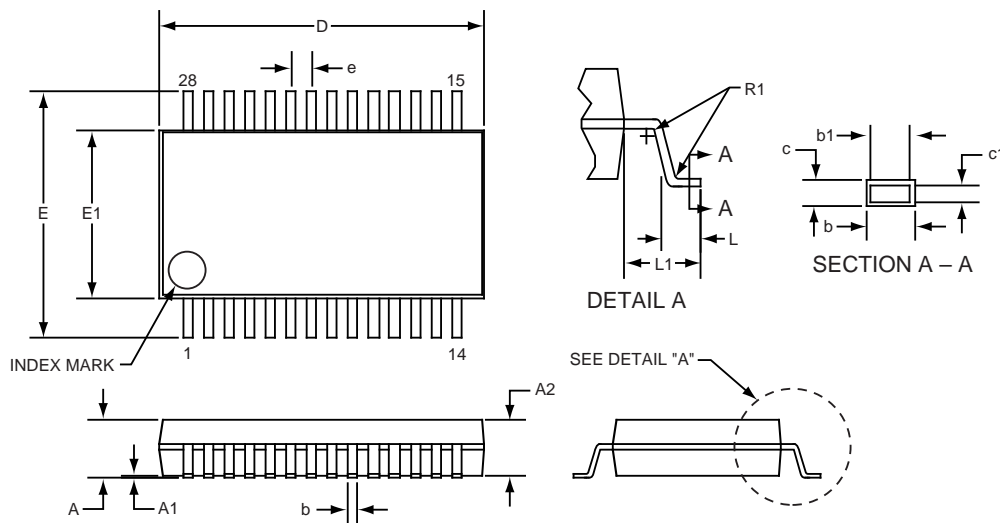




CLC952 Typical Performance Characteristics ($V_{CC} = +5V$, $V_{EE} = -5V$)



Physical Dimensions

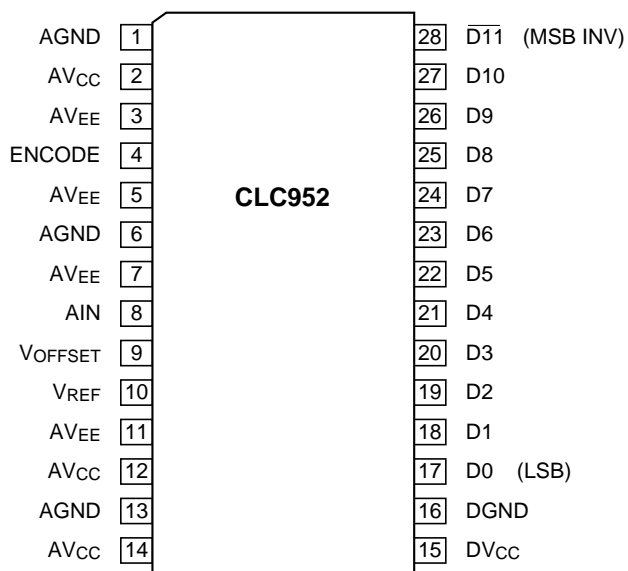


| Symbol | Min | Max | Notes |
|--------|----------|-------|-------|
| A | 1.73 | 2.00 | |
| A1 | 0.00 | 0.21 | |
| A2 | 1.65 | 1.85 | |
| b | 0.20 | 0.40 | |
| b1 | 0.20 | 0.33 | |
| c | 0.10 | 0.22 | |
| c1 | 0.10 | 0.18 | |
| D | 10.07 | 10.33 | 2 |
| E | 7.50 | 7.90 | |
| E1 | 5.20 | 5.38 | 2 |
| e | 0.65 BSC | | |
| L | 0.52 | 0.95 | |
| L1 | 1.25 REF | | |
| R1 | 0.09 | | |

Notes:

1. All dimensions are in millimeters
2. Dimensions D and E1 do not include mold protrusion. Allowable protrusion is 0.20mm per side.

CLC952 Pin Definitions



AGND (Pins 1, 6, 13) Analog circuit ground.

AV_{CC} (Pins 2, 12, 14) +5V power supply for the analog section. Bypass to analog ground with a 0.1μF capacitor.

AV_{EE} (Pins 3, 5, 7, 11) -5V power supply for the analog section. Bypass to analog ground with a 0.1μF capacitor.

ENCODE (Pin 4) ENCODE initiates a new data conversion cycle on each rising edge. Logic for this input is standard TTL. 50% duty cycle is recommended for full compliance with the guaranteed specifications.

AIN (Pin 8) Ground-centered, DC-coupled analog input with a 1V_{pp} maximum input range from -0.5V to +0.5V. Analog input impedance is approximately 500Ω.

V_{OFFSET} (Pin 9) Voltage offset control. Sets the midpoint of the analog input range. Normally left floating. Ratio of applied voltage to effective offset is 200:1. (1V applied to V_{OFFSET} produces 5mV midpoint offset.)

V_{REF} (Pin 10) Internal voltage reference. Nominally +2.4V. V_{REF} can be pulled up or down with a voltage source to program gain and input range. Bypass V_{REF} to ground with a 0.1μF capacitor.

DV_{CC} (Pin 15) +5V power supply for the digital section. Bypass to digital ground with a 0.1μF capacitor.

DGND (Pin 16) Digital ground.

D0-D11 (Pins 17-28) Digital data outputs are CMOS and TTL compatible. D0 is the LSB and D11 is the MSB. MSB is inverted. Output coding is two's complement.

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