

## F100325

### Low Power Hex ECL-to-TTL Translator

#### General Description

The F100325 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides  $V_{BB}$  for single-ended operation, or for use in Schmitt trigger applications. All inputs have 50k $\Omega$  pull-down resistors. When the inputs are either unconnected or at the same potential the outputs will go low.

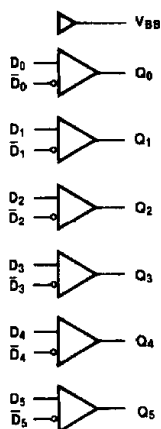
When used in single-ended operation the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The  $V_{EE}$  and  $V_{TTL}$  power may be applied in either order.

#### Features

- Pin/function compatible with F100125
- Meets F100125 AC specifications
- 50% power reduction of the F100125
- Differential inputs with built in offset
- Standard FAST® outputs
- 2000V ESD protection
- -4.2V to -5.7V operating range

**Ordering Code:** See Section 8

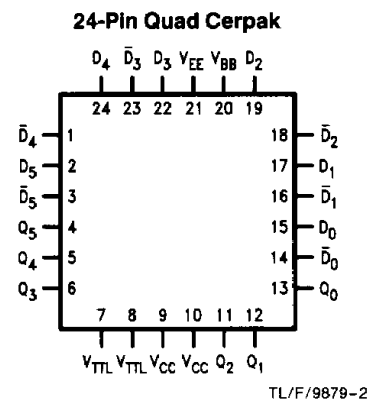
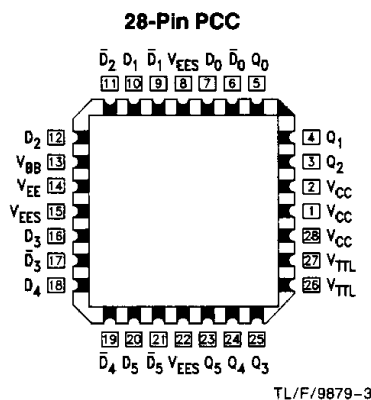
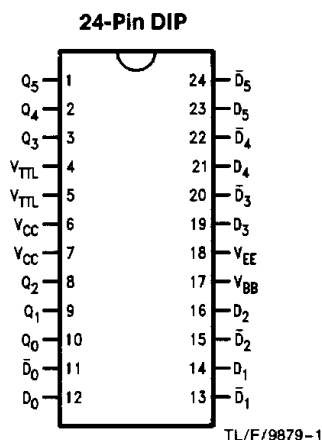
#### Logic Diagram



TL/F/9879-4

Pin Names	Description
$D_0$ – $D_5$	Data Inputs
$\bar{D}_0$ – $\bar{D}_5$	Inverting Data Inputs
$Q_0$ – $Q_5$	Data Outputs

#### Connection Diagrams



## Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Maximum Junction Temperature ( $T_J$ )

Ceramic  $+175^{\circ}\text{C}$

Plastic  $+150^{\circ}\text{C}$

$V_{EE}$  Pin Potential to Ground Pin  $-7.0\text{V}$  to  $+0.5\text{V}$

$V_{TTL}$  Pin Potential to Ground Pin  $+6.0\text{V}$  to  $-0.5\text{V}$

Input Voltage (DC)  $V_{EE}$  to  $+0.5\text{V}$

Output Current (DC Output HIGH)  $-50\text{ mA}$

ESD (Note 2)  $\geq 2000\text{V}$

## Recommended Operating Conditions

Case Temperature ( $T_C$ )

Commercial

$0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Military

$-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply Voltage ( $V_{EE}$ )

Commercial

$-5.7\text{V}$  to  $-4.2\text{V}$

Military

$-5.7\text{V}$  to  $-4.2\text{V}$

## DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$  to  $-5.7\text{V}$ ,  $V_{CC} = \text{GND}$ ,  $T_C = 0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{BB}$	Output Reference Voltage	$-1380$	$-1320$	$-1260$	mV	$I_{VBB} = -2.1\text{ mA}$
$V_{IH}$	Single-Ended Input HIGH Voltage	$-1165$		$-870$	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to $V_{BB}$ )
$V_{IL}$	Single-Ended Input LOW Voltage	$-1830$		$-1475$	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to $V_{BB}$ )
$V_{OH}$	Output HIGH Voltage	2.5			V	$I_{OH} = -2.0\text{ mA}$
$V_{OL}$	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{ mA}$
$V_{DIFF}$	Input Voltage Differential	150			mV	Required for Full Output Swing
$V_{CM}$	Common Mode Voltage	$V_{CC} - 2.0$		$V_{CC} - 0.5$	V	
$I_{IH}$	Input HIGH Current			350	$\mu\text{A}$	$V_{IN} = V_{IH}(\text{Max})$ , $D_0-D_5 = V_{BB}$ , $\bar{D}_0-\bar{D}_5 = V_{IL}(\text{Min})$
$I_{IL}$	Input LOW Current	0.5			$\mu\text{A}$	$V_{IN} = V_{IL}(\text{Min})$ , $D_0-D_5 = V_{BB}$
$I_{OS}$	Output Short-Circuit Current	$-150$		$-60$	mA	$V_{OUT} = \text{GND}^*$
$I_{EE}$	$V_{EE}$ Power Supply Current	$-37$	$-27$	$-17$	mA	$D_0-D_5 = V_{BB}$
$I_{TTL}$	$V_{TTL}$ Power Supply Current		45	65	mA	$D_0-D_5 = V_{BB}$

\*Test one output at a time.

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.80	3.50	0.90	3.70	1.00	4.00	ns	$C_L = 15\text{ pF}$ <i>Figures 1 and 2</i>
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	1.60	4.30	1.70	4.50	1.80	4.80	ns	$C_L = 50\text{ pF}$ <i>Figures 1 and 3</i>

## PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	$C_L = 15\text{ pF}$ <i>Figures 1 and 2</i>
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	1.60	4.10	1.70	4.30	1.80	4.60	ns	$C_L = 50\text{ pF}$ <i>Figures 1 and 3</i>
$t_{S\text{ G-G}}$	Skew Gate to Gate	TBD		TBD		TBD		ps	PCC only (Note 1)

**Note 1:** Gate to gate skew is defined as the difference in the propagation delays between each of the outputs.

## Truth Table

Inputs		Outputs
$D_n$	$\bar{D}_n$	$Q_n$
L	H	L
H	L	H
L	L	L
H	H	L
Open	Open	L
$V_{EE}$	$V_{EE}$	L
L	$V_{BB}$	L
H	$V_{BB}$	H
$V_{BB}$	L	H
$V_{BB}$	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

**Military Version—Preliminary****DC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^{\circ}C$  to  $+125^{\circ}C$ ,  $C_L = 50$  pF,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$V_{BB}$	Output Reference Voltage	-1380	-1260	mV	$-55^{\circ}C$ to $+125^{\circ}C$	$I_{VBB} = -3 \mu A$ , $V_{EE} = -4.2V$ $I_{VBB} = -2.1$ mA, $V_{EE} = -5.7V$	1, 2, 3
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Guaranteed HIGH Signal for All Inputs (with One Input Tied to $V_{BB}$ )	1, 2, 3, 4
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Guaranteed LOW Signal for All Inputs (with One Input Tied to $V_{BB}$ )	1, 2, 3, 4
$V_{OH}$	Output HIGH Voltage	2.5 2.4		mV	$0^{\circ}C$ to $+125^{\circ}C$ $-55^{\circ}C$	$I_{OH} = -2.0$ mA $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	1, 2, 3
$V_{OL}$	Output LOW Voltage		0.5	mV	$-55^{\circ}C$ to $+125^{\circ}C$	$I_{OL} = 20$ mA	
$V_{DIFF}$	Input Voltage Differential	150		mV	$-55^{\circ}C$ to $+125^{\circ}C$	Required for Full Output Swing	1, 2, 3
$V_{CM}$	Common Mode Voltage	-2000	-500	mV	$-55^{\circ}C$ to $+125^{\circ}C$		1, 2, 3, 4
$I_{IH}$	Input HIGH Current		350 500	$\mu A$	$0^{\circ}C$ to $+125^{\circ}C$ $-55^{\circ}C$	$V_{IN} = V_{IH} (Max)$ , $D_0-D_5 = V_{BB}$ , $\bar{D}_0-\bar{D}_5 = V_{IL} (Min)$	1, 2, 3
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^{\circ}C$ to $+125^{\circ}C$	$V_{IN} = V_{IL} (Min)$ , $D_0-D_5 = V_{BB}$	1, 2, 3
$I_{OS}$	Output Short Circuit Current	-150	-60	mA	$-55^{\circ}C$ to $+125^{\circ}C$	$V_{OUT} = GND$ Test One Output at a Time	1, 2, 3
$I_{CEX}$	Output HIGH Leakage Current		250	$\mu A$	$-55^{\circ}C$ to $+125^{\circ}C$	$V_{OUT} = 5.5V$	1, 2, 3
$I_{EE}$	$V_{EE}$ Power Supply Current	-35	-12	mA	$-55^{\circ}C$ to $+125^{\circ}C$	$D_0-D_5 = V_{BB}$	1, 2, 3
$I_{TTL}$	$V_{TTL}$ Power Supply Current		65	mA	$-55^{\circ}C$ to $+125^{\circ}C$	$D_0-D_5 = V_{BB}$	1, 2, 3

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^{\circ}C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at  $-55^{\circ}C$ ,  $+25^{\circ}C$ , and  $+125^{\circ}C$ , Subgroups 1, 2, 3, 7, and 8.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^{\circ}C$ ,  $+25^{\circ}C$ , and  $+125^{\circ}C$ , Subgroups A1, 2, 3, 7, and 8.

**Note 4:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

**Ceramic Dual-In-Line Package AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	$T_C = -55^{\circ}C$		$T_C = +25^{\circ}C$		$T_C = +125^{\circ}C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	1.50	5.00	1.60	4.70	1.70	5.70	ns	$C_L = 50$ pF Figures 1 and 3	1, 2, 3

## Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	1.50	5.00	1.60	4.70	1.70	5.70	ns	$C_L = 50\text{ pF}$ Figures 1 and 3	1, 2, 3

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at  $+25^\circ C$ , temperature only, Subgroup A9.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$  temperatures, Subgroups A10 and A11.

**Note 4:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

## Switching Waveform

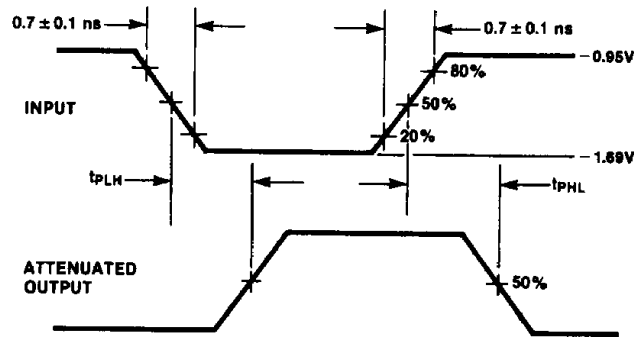
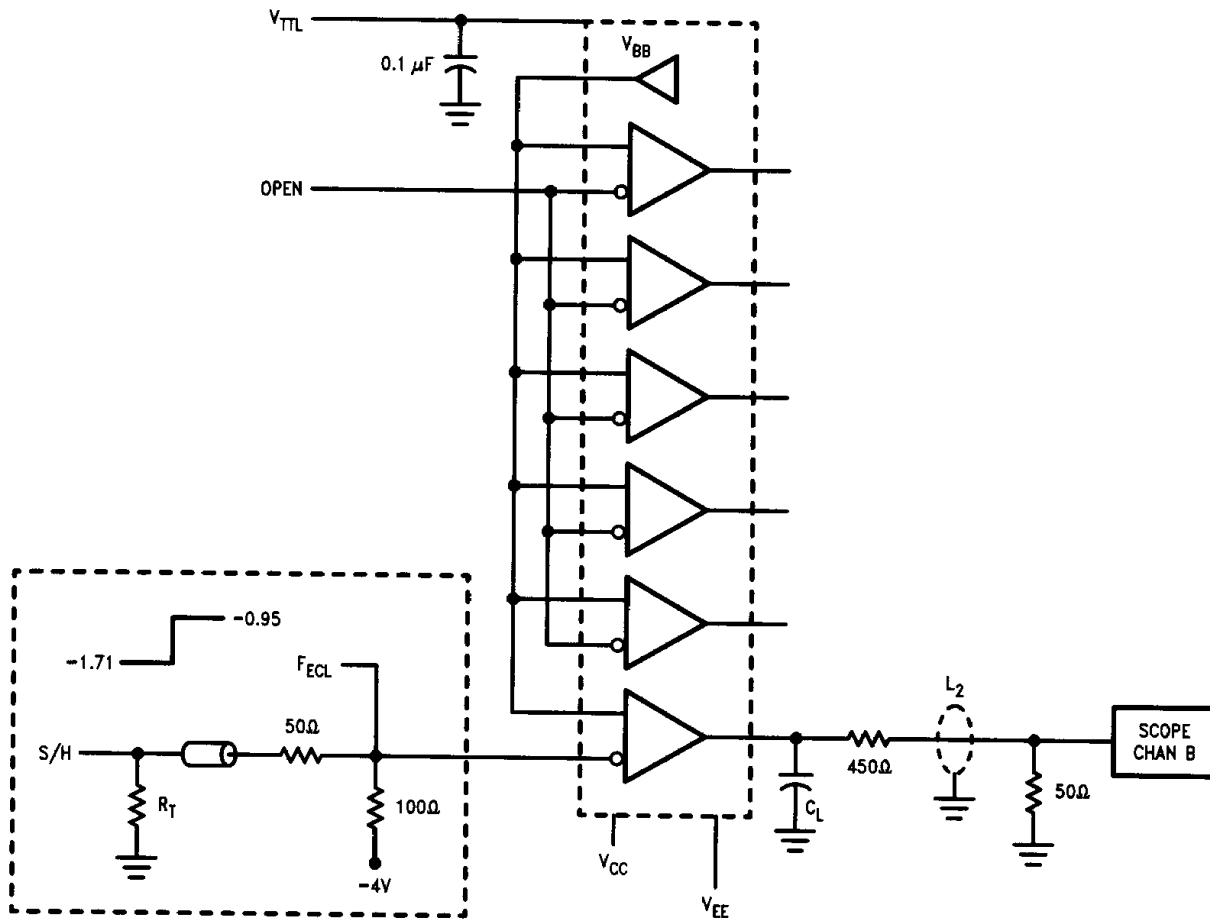


FIGURE 1. Propagation Delay

TL/F/9879-6



## Test Circuits (Continued)



**FIGURE 3. AC Test Circuit for 50 pF Loading**

TL/F/9879-8

**Notes:**

$$V_{CC} = 0V, V_{EE} = -4.5V, V_{TTL} = +5V$$

L1 and L2 = equal length  $50\Omega$  impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling 0.1  $\mu\text{F}$  from GND to  $V_{CC}$ ,  $V_{EE}$  and  $V_{TTL}$

All unused outputs are loaded with 500Ω to GND

$C_L$  = Fixture and stray capacitance = 50 pF