

LH4117/LH4117C Precision RF Amplifier

General Description

The LH4117 is a FET-input wideband amplifier optimized for high speed, low gain applications. It is an ideal alternative to low precision open loop buffers and conventional operational amplifiers. It features a closed loop -3 dB unity gain bandwidth in excess of 150 MHz. Unlike conventional op-amps, the bandwidth is relatively independent of closed loop gain between 1 and 20. A high current output stage is also incorporated, allowing the LH4117 to drive 50Ω terminated lines directly. It is an ideal choice for video distribution, flash converter input buffering and ATE pin drivers.

Features

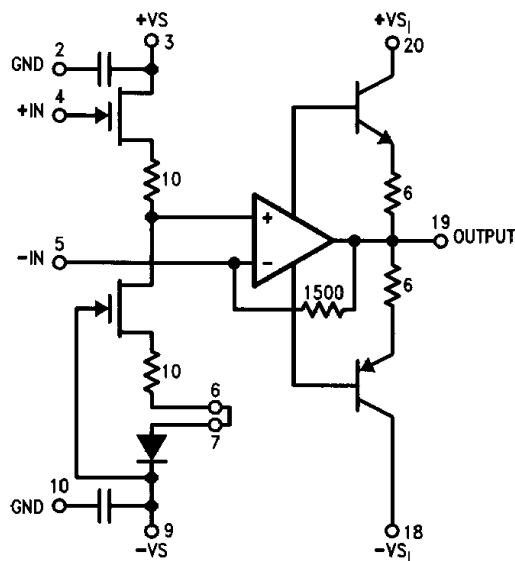
- 150 MHz bandwidth
- 9 ns settling time to 0.2%

- 3.3 ns rise and fall times
- Output current to 200 mA
- FET-input, low bias current
- 2500 V/ μ S slew rate (100 Ω load)
- ± 0.3 dB gain flatness ($A_V = 20$)

Applications

- Unity gain buffers
- Low gain op amp
- High speed peak detectors
- Video amplifier

LH4117 Simplified Schematic



TL/K/9348-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_S) $\pm 18V$
Power Dissipation, (P_D) See Graph 2.0W

Input Voltage Range, (V_{CM}) $\pm V_S$
Operating Temperature Range, (T_A)
LH4117CD -25°C to $+85^\circ\text{C}$
LH4117D -25°C to $+125^\circ\text{C}$
Storage Temperature Range, (T_{STG}) -65°C to $+150^\circ\text{C}$
Maximum Junction Temperature, (T_j) 175°C
Lead Temperature (Soldering, <10 sec.) 300°C

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4117D			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	$V_{IN} = 0V$, $T_A = T_j = 25^\circ\text{C}$ (Note 4)	15	20 25		mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift	$V_{IN} = 0V$	100			$\mu\text{V}/^\circ\text{C}$
I_B	Non-Inverting Input Bias Current	$T_A = T_j = 25^\circ\text{C}$ Pin 4 (Note 4)	0.2	2 5		nA
V_O	Output Voltage Swing	$R_L = 100\Omega$		± 11		V (Min)
PSRR	Power Supply Rejection Ratio	$\Delta V_S = \pm 10V$ to $\pm 15V$	70	60 50		dB (Min)
I_O	Peak Output Current	$T_A = T_j = 25^\circ\text{C}$ (Note 5)	200			mA
I_S	Supply Current	$T_A = T_j = 25^\circ\text{C}$		45		mA
P_D	Quiescent Power Dissipation	(Note 5)		1.35		W

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4117CD			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	$V_{IN} = 0V$, $T_A = T_j = 25^\circ\text{C}$ (Note 4)	15	20	25	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift		100			$\mu\text{V}/^\circ\text{C}$
I_B	Non-Inverting Input Bias Current	$T_A = T_j = 25^\circ\text{C}$ Pin 4 (Note 4)	0.2	2	5	nA
V_O	Output Voltage Swing	$R_L = 100\Omega$		± 11	± 11	V (Min)
PSRR	Power Supply Rejection Ratio	$\Delta V_S = \pm 10V$ to $\pm 15V$	70	50		dB (Min)
I_O	Peak Output Current	$T_A = T_j = 25^\circ\text{C}$ (Note 5)	200			mA
I_S	Supply Current			45		mA
P_D	Quiescent Power Dissipation	(Note 5)		1.35		W

AC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $T_A = 25^\circ C$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4117D/LH4117CD			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
t_r	Small Signal Rise Time	$V_O = 5V$, $A_V = +20$ 10%–90%	3			ns
t_s	Settling Time to 0.2%	$V_O = 10V$	9			ns
f _{-3 dB}	Small Signal Bandwidth	$V_O = 4 V_{PP}$, $A_V = 20$	150	100		MHz (Min)
f _{-3 dB}	Large Signal Bandwidth	$V_O = 20 V_{PP}$, $A_V = 20$	70	40		MHz
	–1 dB Gain Compression	V_O , $f = 50$ MHz, $A_V = +20$	20			V_{PP}
SR	Slew Rate	$V_{IN} = \pm 1V$, $A_V = +20$ $V_O = 10\%–90\%$, $V_O = \pm 4V$	2500 6000			V/ μ S V/ μ S
	Harmonic Distortion	Second Order, $V_O = 4 V_{PP}$, 20 MHz	–50			dB
	Gain Flatness	$V_{IN} = 100$ mV _{PP} , $A_V = +20$ $f = DC$ to 50 MHz $f = DC$ to 70 MHz	± 0.3 ± 0.9			dB
	Differential Gain	(Note 6)	0.01			dB
	Differential Phase	(Note 6)	0.01			deg

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4117C is $-25^\circ C$ to $+85^\circ C$, and LH4117 is $-55^\circ C$ to $+125^\circ C$.

Note 2: Tested limits are guaranteed and 100% production tested.

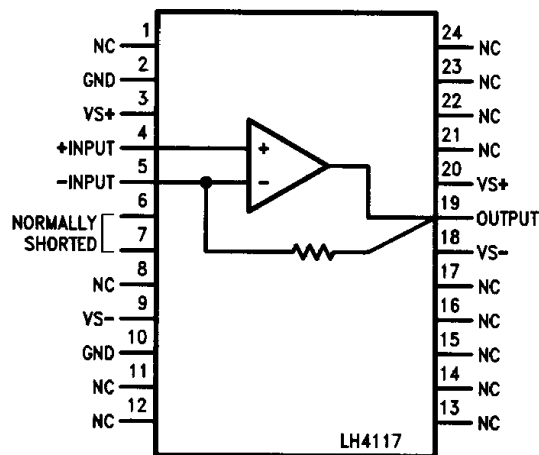
Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specifications is at $25^\circ C$ junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_j = 25^\circ C$.

Note 5: When the LH4117 is operated at elevated temperature (such as $125^\circ C$), some form of heat sinking or forced air cooling is required. The quiescent power with $V_S = \pm 15V$ is 1.2W, whereas the package can only handle 660 mW without a heatsink at $125^\circ C$.

Note 6: Differential gain and phase were measured at video levels (0 mV–750 mV) between 15.7 kHz and 3.58 MHz. The actual values are smaller than 0.01 dB and 0.01 deg, but could not be accurately measured with existing equipment.

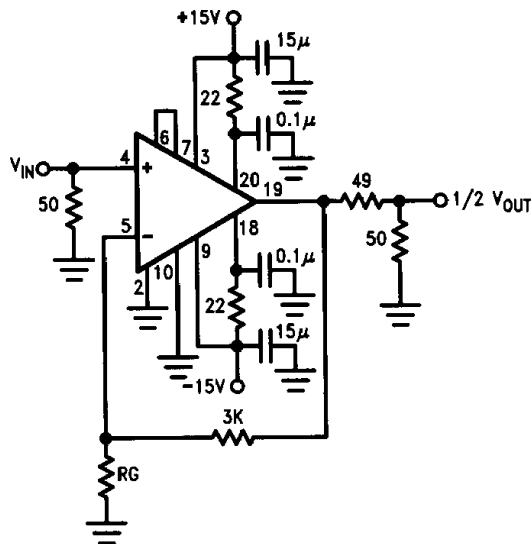
Connection Diagram



Order Number LH4117D or LH4117CD
See NS Package Number D24J

TL/K/9348–2

AC Test Circuit



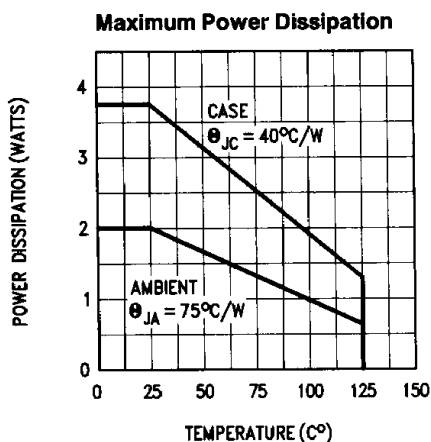
TL/K/9348-3

The 22 ohm resistors in the supply line are for limiting the short circuit current.

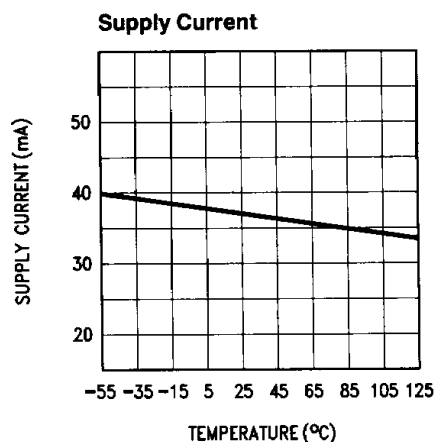
For a gain of 20 select $R_G = 52 \Omega$.

Slew rate measurement is done with $R_G = 56 \Omega$, $\Delta V_{IN} = \pm 1V$ Step with 1 ns rise time.

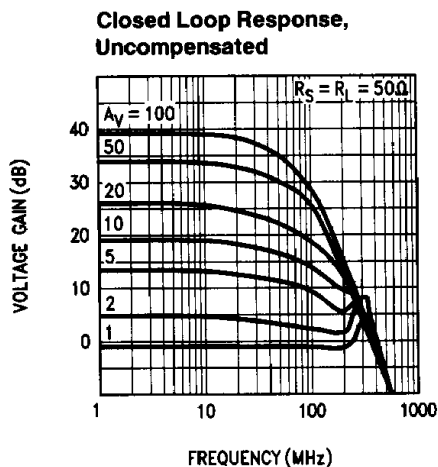
Typical Performance Characteristics



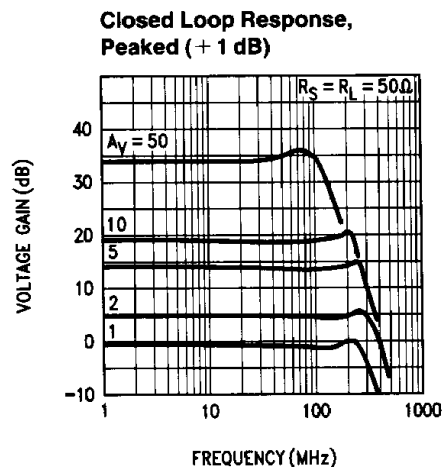
TL/K/9348-4



TL/K/9348-5



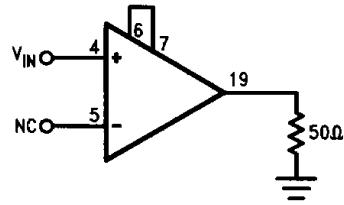
TL/K/9348-6



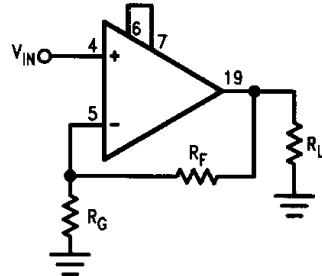
TL/K/9348-7

*For details see application section.

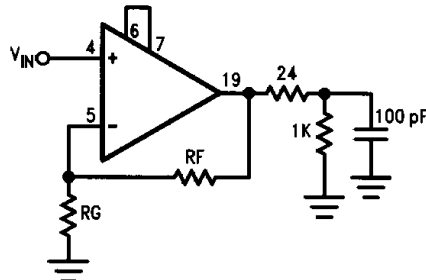
Typical Applications



TL/K/9348-8

FIGURE 1. Unity Gain Buffer

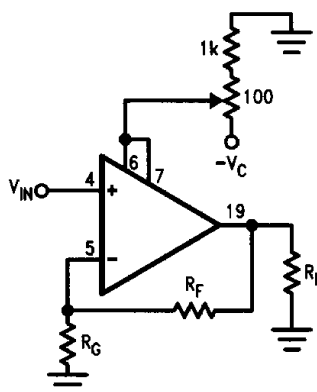
TL/K/9348-9

FIGURE 2. Amplifier

TL/K/9348-10

FIGURE 3. Driving Capacitive Loads

Typical Applications (Continued)



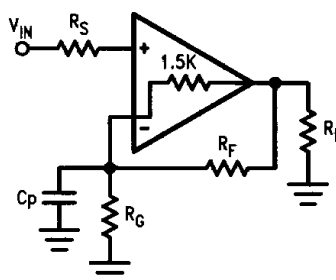
TL/K/9348-11

FIGURE 4. Offset Adjust

Application Hints

The two inputs of the LH4117 are radically different. While the non-inverting input is the gate of a FET, the inverting input is low impedance.

The graph "Closed Loop Response, Uncompensated" shows gain vs. frequency using only the internal feedback resistor. This performance can be considerably improved by choice of R_F and peaking (See graph "Closed Loop Response, Peaked")



$$A_V = 1 + \frac{R_F^*}{R_G}$$

$$R_F^* = \frac{1500 \times R_F}{1500 + R_F}$$

TL/K/9348-12

FIGURE 5. LH4117 as Amplifier with Compensation Elements

Guidelines for Compensation

A_V (Nom. Gain)	R_F Ω	R_F^* Ω	R_G Ω	C_p pF	R_S Ω
1	—	1.5k	—	—	140
2	3k	1k	1k	—	—
5	3k	1k	165	1.2	—
10	3k	1k	110	3.9	—
50	3k	1k	20	25	—
100	750	500	5	100	—

The maximum peaking for the above values was +1 dB. For $A_V = 1$, the input resistor R_S corrects for excessive peaking.