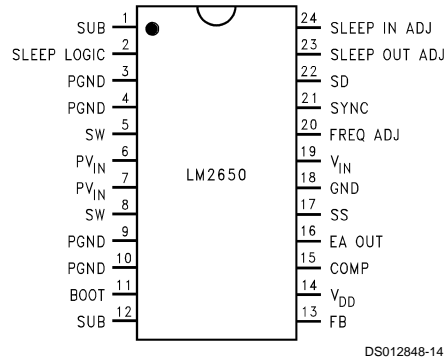




## Connection Diagram



**Top View**  
**24-Lead Small Outline Package (M)**  
**Order Number LM2650M-ADJ**  
**See Package Number M24B**

## Pin Descriptions (Refer to the Block Diagrams)

Pins	Description
1, 12	<b>SUB:</b> These pins make electrical contact with the substrate of the die. Ground them. For best thermal performance, ground them to the same large, uninterrupted copper plane as the PGND pins.
2	<b>SLEEP LOGIC:</b> Use this logic input to select the conversion mode; low selects PWM, high selects sleep, and high impedance (open) permits the LM2650 to move freely and automatically between the modes, using PWM for moderate to heavy loads and sleep for light loads.
3, 4, 9, 10	<b>PGND:</b> The ground return of the power stage. The power stage consists of the two power switches Q1 and Q2, the gate drivers DH and DL, and the linear voltage regulators VRegH and VRegL. For best electrical and thermal performance, ground these pins to a large, uninterrupted copper plane.
5, 8	<b>SW:</b> The output node of the power stage. It swings from slightly below ground to slightly below the voltage to PV <sub>IN</sub> . To minimize the effects of switching noise on nearby circuitry, keep all traces originating from SW short and to the point. Route all traces carrying signals well away from the SW traces.
6, 7	<b>PV<sub>IN</sub>:</b> The positive supply rail of the power stage. Bypass each PV <sub>IN</sub> pin to PGND with a 0.1 $\mu$ F capacitor. Use capacitors having low ESL and low ESR, and locate them close to the IC.
11	<b>BOOT:</b> The positive supply rail of the high-side gate driver DH. Connect a 0.1 $\mu$ F capacitor from this node to SW. Bootstrapping action creates a supply rail about 9V above that at PV <sub>IN</sub> , and DH uses this rail to override the gate of the NMOS power FET Q1. Overriding ensures low R <sub>DS(on)</sub> .
13	<b>FB:</b> The feedback input.
14	<b>V<sub>DD</sub>:</b> An internal regulator steps the input voltage down to a 4V rail used by the signal-level circuitry. V <sub>DD</sub> is the output node of this regulator. Bypass V <sub>DD</sub> to GND close to the IC with a 0.2 $\mu$ F capacitor.
15	<b>COMP:</b> The inverting input of the error amplifier EA.
16	<b>EA OUT:</b> The output node of the error amplifier EA.
17	<b>SS:</b> The soft start node. Connect a capacitor from SS to GND.
18	<b>GND:</b> The ground return of the signal-level circuitry.
19	<b>V<sub>IN</sub>:</b> The positive supply rail of the internal 4V regulator. Bypass V <sub>IN</sub> to GND close to the IC with a 0.1 $\mu$ F capacitor.
20	<b>FREQ ADJ:</b> The LM2650 switches at a nominal 90 kHz. Connect a resistor between FREQ ADJ and GND to adjust the frequency up from the nominal. Use the graph under Typical performance Characteristics to select the resistor.
21	<b>SYNC:</b> The synchronization input. If the switching frequency is to be synchronized with an external clock signal, apply the clock signal here. Ground if not used.
22	<b>SD:</b> Use this logic input to control shutdown; pull low for operation, high for shutdown.
23	<b>SLEEP OUT ADJ (SOA):</b> The value of the resistor connected between SIA and ground programs the sleep-in threshold. Higher values program lower thresholds.
24	<b>SLEEP IN ADJ (SIA):</b> The value of the resistor connected between SIA and ground programs the sleep-in threshold. Higher values program lower thresholds.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(All voltages are referenced to the PGND and GND pins.)	
DC Voltage at $PV_{IN}$ and $V_{IN}$	20V
DC Voltage at SD, SLEEP LOGIC and SYNC	15V
DC current into SW	$\pm 7.5A$
Junction Temperature	Limited by the IC
DC Power Dissipation (Note 2)	1.28W
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$

Soldering Time, Temperature (Note 3)

Wave (4 seconds)	$260^{\circ}C$
Infrared (10 seconds)	$240^{\circ}C$
Vapor Phase (75 seconds)	$219^{\circ}C$
ESD Susceptibility (Note 4)	1.3 kV

## Operating Ratings (Note 1)

Supply Voltage Range ( $PV_{IN}$ and $V_{IN}$ )	4.5V to 18V
Junction Temperature Range	$-40^{\circ}C$ to $+125^{\circ}C$

## Electrical Characteristics

$V_{PVIN} = 15V$ ,  $V_{SLEEP LOGIC} = 0V$  and  $V_{SD} = 0V$  unless superseded under **Conditions**. Typical and limits appearing in plain type apply for  $T_A = T_J = +25^{\circ}C$ . Limits appearing in **boldface** type apply over the full junction temperature range shown under **Operating Ratings**.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
$V_{OUT}$	Output Voltage	$R1 = 75\text{ k}\Omega$ , 1%, $R2 = 25\text{ k}\Omega$ , 1%, $7.5V \leq V_{PVIN} \leq 18V$ $0.12A \leq I_{LOAD} \leq 3A$	5.00	4.80/ <b>4.75</b> 5.20/ <b>5.25</b>	V V(min) V(max)
$\eta_1$	System Efficiency	$I_{LOAD} = 1A$ , $T_A = 25^{\circ}C$ , $F_{OSC}$ Not Adjusted	94		%
$\eta_2$	System Efficiency	$I_{LOAD} = 3A$ , $T_A = 25^{\circ}C$ , $F_{OSC}$ Not Adjusted	89		%
$V_{REF}$	Reference Voltage	$V_{SLEEPLOGIC} = 3V$ (Note 7)	1.25	1.281/ <b>1.294</b> 1.219/ <b>1.206</b>	V(min) V(max)
$I_Q$	Quiescent Current in PWM mode	$V_{FB} = V_{REF}$ $-20mV$ (Note 8)	4.0	6.50/ <b>7.0</b>	mA mA(max)
$I_{QS}$	Quiescent Current in Sleep mode	$I_{VFB} = V_{REF} - 20mV$ , $V_{SLEEPLOGIC} = 3V$ (Note 8)	850	1.35/ <b>1.60</b>	$\mu A$ mA(max)
$I_{QSD}$	Quiescent Current in Shutdown mode	$V_{SD} = 3V$ (Note 8)	9	20/ <b>25</b>	$\mu A$ $\mu A$ (max)
$R_{DS(on) HS}$	DC On-Resistance Drain-to-Source of the High-Side Power Switch	$I_{DS} = 1A$ , $V_{SLEEPLOGIC} = 3V$ , $V_{FB} = 3V$ , $V_{BOOT} = 24V$	130	170/ <b>245</b>	$m\Omega$ $m\Omega$ (max)
$R_{DS(on) LS}$	DC On-Resistance Drain-to-Source of the Low-Side Power Switch	$I_{DS} = 1A$ , $V_{FB} = 3V$	125	175/ <b>245</b>	$m\Omega$ $m\Omega$ (max)
$I_{L HS}$	Leakage current of the High-Side Power Switch	$V_{PVIN} = 18V$ , $V_{SW} = 0V$ , $V_{SD} = 3V$	100	<b>10</b>	nA $\mu A$ (max)
$I_{L LS}$	Leakage current of the Low-Side Power Switch	$V_{PVIN} = 18V$ , $V_{SW} = 18V$ , $V_{SD} = 3V$	95	<b>210</b>	$\mu A$ $\mu A$ (max)
$I_{LIMIT}$	Active Current Limit of the High-Side Power Switch	$V_{PVIN} = 15V$ , $V_{BOOT} = 24V$ , $V_{FB} = 3V$ , $V_{SLEEPLOGIC} = 3V$ ,	5.5	<b>3.5</b> <b>7.5</b>	A A(min) A(max)
$F_{OSC}$	Oscillator Frequency	$V_{FB} = V_{REF} - 20\text{ mV}$	90	80/ <b>75</b> 100/ <b>105</b>	kHz kHz(min) kHz(max)
$F_{MAX}$	Maximum Oscillator Frequency	$I_{FREQ ADJ} = 100\mu A$ , (Note 9) $V_{FB} = V_{REF} - 20\text{ mV}$	315	270/ <b>260</b> 360/ <b>370</b>	kHz kHz(min) kHz(max)
$D_{MAX}$	Maximum Duty Cycle	$V_{FB} = V_{REF} - 20\text{ mV}$ , $F_{OSC}$ Not Adjusted	97	94/ <b>93</b>	% %(min)

## Electrical Characteristics (Continued)

$V_{PVIN} = 15V$ ,  $V_{SLEEP\ LOGIC} = 0V$  and  $V_{SD} = 0V$  unless superseded under **Conditions**. Typical and limits appearing in plain type apply for  $T_A = T_J = +25^\circ C$ . Limits appearing in **boldface** type apply over the full junction temperature range shown under **Operating Ratings**.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
$D_{MIN}$	Minimum Duty Cycle	$V_{FB} = V_{REF} + 50\text{ mV}$ , $F_{OSC}$ Not Adjusted	2.8	<b>5</b>	% %(min)
$V_{DD}$	Internal Rail Voltage	$I_{VDD} = 1\text{ mA}$	4.0	3.6/ <b>3.4</b> 4.2/ <b>4.3</b>	V V(min) V(max)
$V_{BOOT}$	Bootstrap Regulator Voltage (VRegH)	$I_{BOOT} = 1\text{ mA}$	7.5	6.5/ <b>6.0</b>	V V(min)
$I_{SS}$	Soft Start Current		10	13.5/ <b>20.0</b>	$\mu A$ $\mu A$ (max)
$V_{HYST}$	Hysteresis of the Sleep Comparator (C2Figure 2)	$V_{SLEEPLOGIC} = 3V$	30	<b>10</b> <b>50</b>	mV mV(min) mV(max)
	$V_{IL}$ of SD			<b>0.95</b>	V(max)
	$V_{IH}$ of SD			<b>2.10</b>	V(min)
	$V_{IL}$ of SLEEP LOGIC			<b>0.9</b>	V(max)
	$V_{IH}$ of SLEEP LOGIC			<b>2.0</b>	V(min)
	$V_{IL}$ of SYNC			<b>0.50</b>	V(max)
	$V_{IH}$ of SYNC			<b>1.45</b>	V(min)
$T_{SD}$	$T_J$ for Thermal Shutdown		170		$^\circ C$

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which the device operates correctly. Operating ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics.

**Note 2:** This rating is calculated using the formula  $P_{DCmax} = (T_{Jmax} - T_A) / \theta_{JA}$ , where  $P_{DCmax}$  is the absolute maximum power dissipation,  $T_{Jmax}$  is the maximum junction temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance of the package. The  $P_{DCmax}$  rating of 1.28W results from substituting  $170^\circ C$ ,  $70^\circ C$  and  $78^\circ C/W$  for  $T_{Jmax}$ ,  $T_A$  and  $\theta_{JA}$  respectively. A  $\theta_{JA}$  of  $78^\circ C$  represents the worst condition of no heat sinking of the M24B small-outline package. Heat sinking allows the safe dissipation of more power. See Application Notes on thermal management. The LM2650 actively limits its junction temperature to about  $170^\circ C$ .

**Note 3:** For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook published by National Semiconductor Corporation.

**Note 4:** ESD is applied using the human-body model, a 100pF capacitor discharged through a 1.5k $\Omega$  resistor.

**Note 5:** A typical is the center of characterization data taken at  $T_A = T_J = 25^\circ C$ .

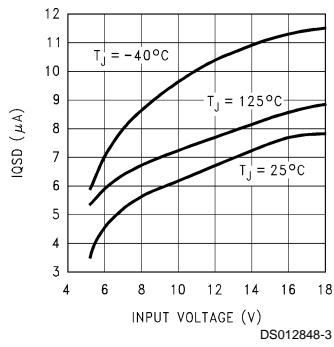
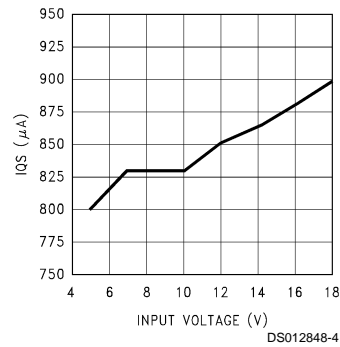
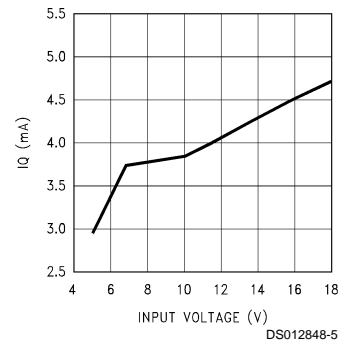
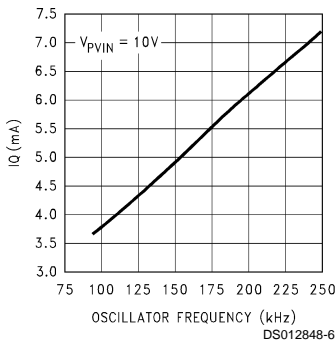
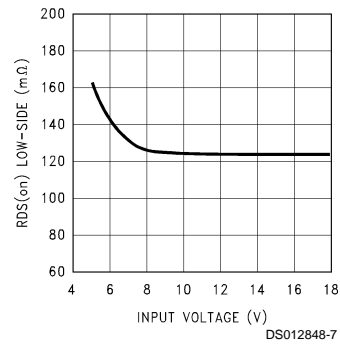
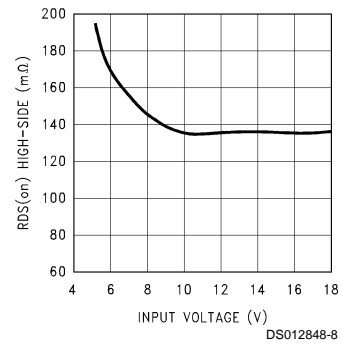
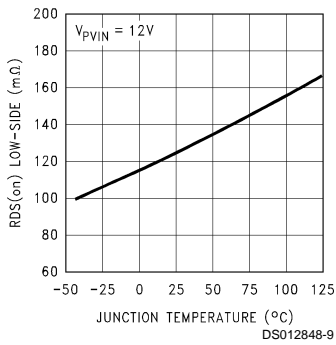
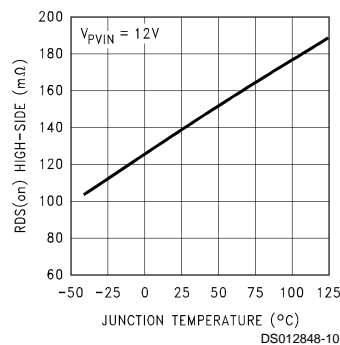
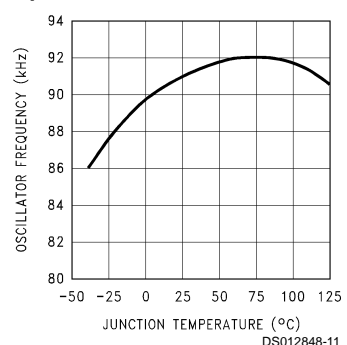
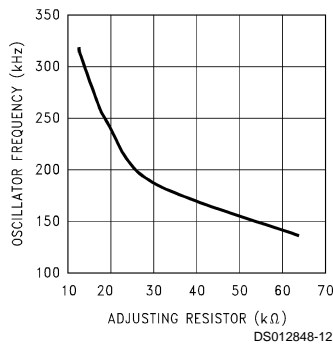
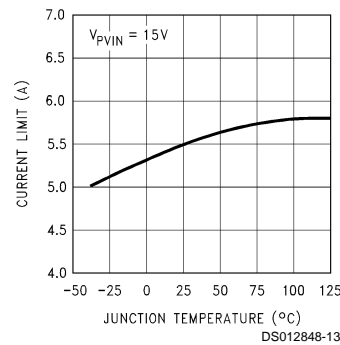
**Note 6:** All limits are guaranteed. The guarantee is backed with 100% testing at  $T_A = T_J = 125^\circ C$  and statistical correlation for room temperature and cold limits.

**Note 7:**  $V_{REF}$  is measured at SLEEP OUT ADJ.

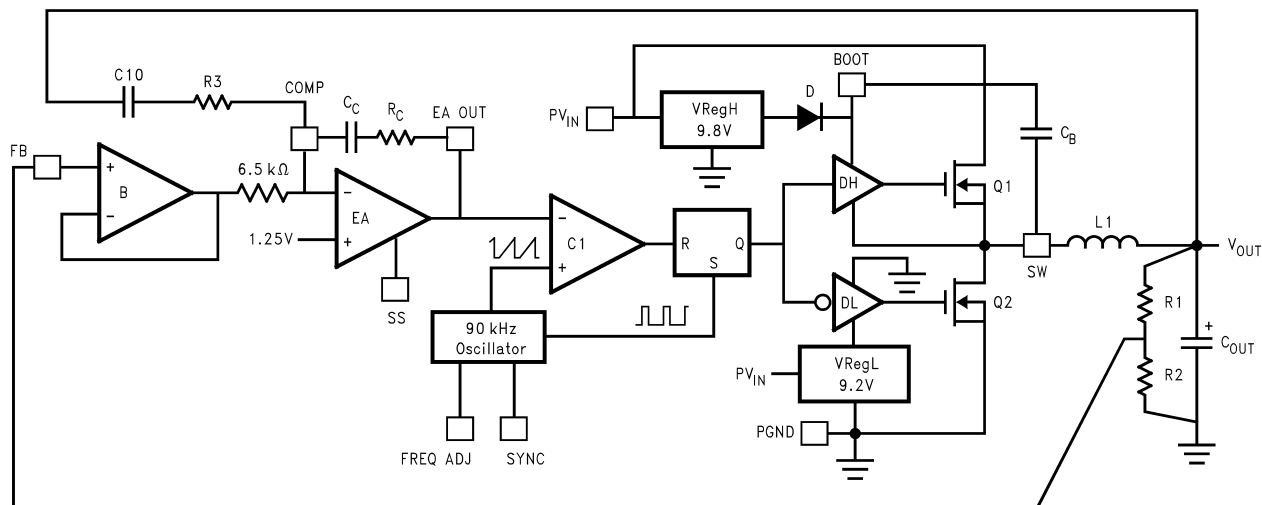
**Note 8:** Quiescent current is the total current flowing into the  $P_{VIN}$  and  $V_{IN}$  pins.  $I_Q$  includes the current used to drive the gates of the two NMOS power FETs at the nominal switching frequency.  $I_{QS}$  includes no such current.

**Note 9:** Pulling 100 $\mu A$  out of FREQ ADJ simulates adjusting the oscillator frequency with a 12.5 k $\Omega$  resistor connected from FREQ ADJ to GND. The sleep mode cannot be used at switching frequencies above 250 kHz.

# Typical Performance Characteristics

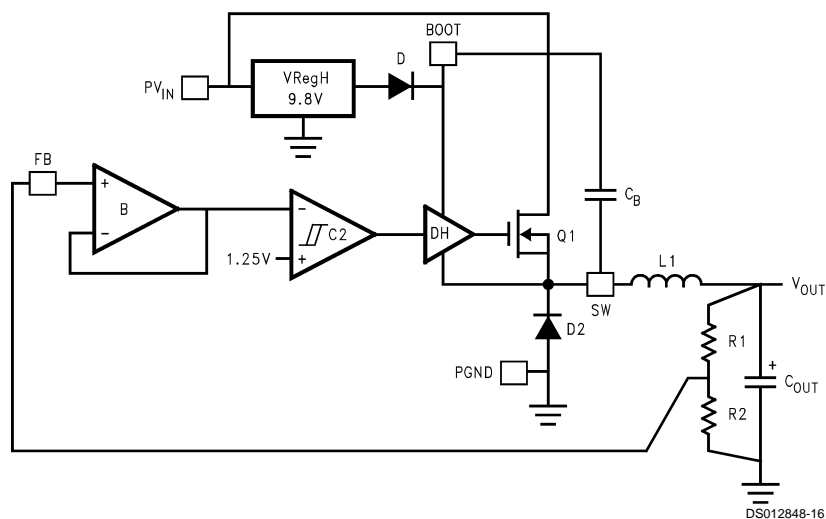
 **$I_{QSD}$  vs Input Voltage**

 **$I_{QS}$  vs Input Voltage**

 **$I_Q$  vs Input Voltage**

 **$I_Q$  vs Oscillator Frequency**

 **$R_{DS(on)}$  Low-Side vs Input Voltage**

 **$R_{DS(on)}$  High-Side vs Input Voltage**

 **$R_{DS(on)}$  Low-Side vs Junction Temperature**

 **$R_{DS(on)}$  High-Side vs Junction Temperature**

**Oscillator Frequency vs Junction Temperature**

**Oscillator Frequency vs Adjusting Resistor**

**Current Limit vs Junction Temperature**


## Block Diagrams



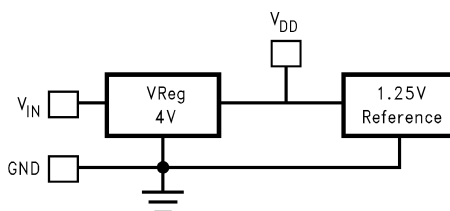
DS012848-15

FIGURE 1. The PWM Circuit with External Components in a Closed Control Loop



DS012848-16

FIGURE 2. The Hysteretic or "Sleep" Circuit with External Components in a Closed Control Loop



DS012848-21

FIGURE 3. The Internal Voltage Regulator and Voltage Reference used by Both the PWM and Hysteretic Circuits

## Operation

### OVERVIEW

The LM2650 uses two step-down conversion modes: fixed-frequency pulse-width modulation (PWM) and hysteretic. It moves freely and automatically between them, using PWM for moderate to heavy loads and hysteretic for light loads.

For clarity, separate block diagrams for each conversion mode have been included. See *Figure 1* and *Figure 2*. Blocks used in both modes appear in both diagrams with the same label. For example, both modes use the input buffer B. To keep the diagrams simple, most power supply rails have been omitted. R3, C10, R<sub>C</sub>, C<sub>C</sub>, C<sub>B</sub>, L1, R1, R2, and C<sub>OUT</sub> are outside the IC.

### THE PWM CIRCUIT (*Figure 1*)

The PWM is a fixed-frequency, voltage-mode pulse-width modulator. It consists of four functional blocks: an input buffer, an error amplifier, a modulator, and a power stage.

1. The input buffer B: B is a voltage follower. A fraction of the output voltage is fed back to its noninverting input FB. Circumventing B by using the COMP input as the feedback input will cause the IC to malfunction.
2. The error amplifier EA: EA is a voltage amplifier. It subtracts the feedback voltage from the 1.25V reference and amplifies the difference to produce an error voltage for the control loop. For the purpose of loop compensation, EA is typically configured as an integrator. In this configuration, a capacitor C<sub>C</sub> and a resistor R<sub>C</sub> are connected in series between the inverting input COMP and the output terminal EA OUT. The capacitor and the internal 6.5kΩ resistor create a pole, while the capacitor and series resistor create a zero.
3. The modulator: The modulator is the heart of the PWM circuit. It consists of the 90 kHz oscillator, the voltage comparator C1, and output logic represented here as a simple SR latch.

The modulator generates a continuous stream of rectangular, signal-level. It generates the pulses at a fixed frequency, and it modulates or varies their widths in response to variations in the error voltage. The pulses appear at Q, the output of the SR latch. An increase in the error voltage results in a proportional increase in the pulse widths, and, conversely, a decrease in the error voltage results in a proportional decrease in the pulse widths.

The oscillator produces a 90 kHz sawtooth that ramps between 1V and 2V. At the beginning of each ramp, the oscillator sets the SR latch sending Q high. As the ramp voltage surpasses the error voltage, C1 resets the SR latch sending Q low. An increase in the error voltage increases the time between the setting and the resetting of the SR latch which, in turn, results in an equal increase in pulse widths: that is, an equal increase in the time Q spends high in each cycle. A decrease in the error voltage has the opposite effect on the pulse widths as it decreases the time between the setting and resetting of the SR latch.

4. The power stage: The power stage puts some punch between the output of the modulator by translating the stream of signal-level pulses generated by the modulator into a stream of power pulses that swing from ground up to the input voltage while sinking and sourcing as much as 3.5A. The power stage consists of two gate

drivers DH and DL, two linear voltage regulators VRegH and VRegL, and two NMOS power FETs Q1 and Q2.

The power pulses appear at the SW mode. When Q goes high, DL drives the gate of Q2 low turning Q2 off. While Q2 turns off, the SW potential may remain at just below ground as the body diode of Q2 conducts what was previously reverse current (source-to-drain) in Q2, or the SW potential may swing up to just above the input voltage as the body diode of Q1 conducts what was previously forward current (drain-to-source) in Q2. About 50 ns after Q goes high, DH drives the gate of Q1 high turning Q1 on. If the task remains, Q1 pulls the SW potential up, if not, Q1 simply takes over the conduction responsibility from its own body diode. When Q goes low, the inverse action occurs resulting in the SW potential swinging from the input voltage to the ground. The 50 ns delay between one switch beginning to turn off and the other switch beginning to turn on prevents the switches from "shooting through" directly from the input supply to the ground.

The PWM circuit drives the pulse stream into the low-pass filter made up of L1 and C<sub>OUT</sub>. The filter passed the DC component of the stream and attenuates the AC components. The output of the filter is the DC voltage V<sub>OUT</sub> superimposed with a small ripple voltage. Since the DC component of any periodic waveforms the average value of the waveform, V<sub>OUT</sub> can be found using:

$$V_{OUT} = \frac{1}{T} \times \int_0^T v(t) dt. \quad (1)$$

Here T is the switching period in seconds V(t) is the pulse stream. Under DC steady-state conditions, (1) yields

$$V_{OUT} = V_{IN} \times \frac{t_{ON}}{T} = V_{IN} \times D. \quad (2)$$

Here V<sub>IN</sub> is the input voltage, and therefore the height of the pulses, in volts, is the width of the pulses in seconds, and D is the ratio of t<sub>ON</sub> to T, the duty or the duty cycle.

The output voltage is programmed using the resistive divider made up for R1 and R2,

$$V_{OUT} = 1.25 \times \left(1 + \frac{R1}{R2}\right). \quad (3)$$

As Q1 turns on, its source voltage swings up to just below the input voltage. The LM2650 uses a simple technique called "bootstrapping" to pull the positive supply rail of DH (at BOOT) up along with the source voltage of Q1, but to a voltage above the input voltage. Because the source of Q1 and the positive supply rail of DH make the same voltage swing together, DH maintains the positive gate-to-source voltage required to turn Q1 on. Q12 plays an active role in pulling the supply rail of DH up and is therefore said to pull itself up by its "bootstraps", thus the name of the technique and of the BOOT pin.

In the typical application, a capacitor CB is connected outside the IC between the BOOT and SW pins. When Q2 is on, the input supply charges CB through VRegH and the internal diode D.

### THE HYSTERETIC CIRCUIT AND LOOP (*Figure 2*)

Except for C2, the hysteretic circuit borrows all its circuit blocks from the PWM circuit.

The hysteretic comparator C2 is a voltage comparator with built-in hysteresis V<sub>HYST</sub> of typically 30mV centered at 1.25V.

## Operation (Continued)

The diode D2 is the body diode of Q2. The hysteretic circuit uses D2 as a rectifier instead of switching Q2 as a synchronous rectifier.

When the load current drops below the prescribed sleep-in threshold, the LM2650 shuts down the PWM loop and starts up the hysteretic loop. The hysteretic loop supports light loads more efficiently because it uses less power to support its own operation; it uses less bias power because it's a simpler loop having less circuit blocks to bias, and it switches slower, so it incurs lower switching losses.

The hysteretic control loop does not switch at a constant frequency. Instead, it monitors  $V_{OUT}$  and switches only when  $V_{OUT}$  reaches either side of a narrow window centered on the desired output voltage. C2 directs the switching based on its reading of the feedback voltage. Switching in this manner yields a regulated output voltage consisting of the desired output voltage and an AC ripple voltage. The magnitude of the AC component can be approximated using

$$V_{OUT\_PP} = V_{HYST} \times \frac{(R1 + R2)}{R2} \quad (4)$$

For example, with  $V_{OUT}$  set to 5V,  $V_{OUT\_PP}$  is approximately 120mV,

$$V_{OUT\_PP} = 0.03 \times \frac{(75 + 24.9)}{24.9} = 120 \text{ mV}. \quad (5)$$

When it starts up, the hysteretic loop turns Q1 on. While Q1 is on, the input power supply charges  $C_{OUT}$  and supplies current to the load. Current from the supply reaches C and the load via the series path provided by Q1 and L1. As the feedback voltage just surpasses the upper hysteretic threshold of C2, the output of C2 changes from high to low, and HD responds by pulling the gate of Q1 down turning Q1 off. As Q1 turns off, L1 generates a negative-going voltage transient that D2 clamps at just below ground. D2 remains on only briefly as the current in L1 runs out. While both Q1 and D2 are off,  $C_{OUT}$  alone supplies current to the load. As the

feedback voltage just surpasses the lower hysteretic threshold of C2, the output of C2 changes states from low to high, and DH responds by pulling the gate of Q1 up turning Q1 on and starting the hysteretic cycle over.

Note that as the load current decreases, it takes increasingly longer periods for the load current to discharge  $C_{OUT}$  through the hysteretic window, and as the load current increases, the periods become even shorter. It can be seen from the above observation that the switching frequency of the hysteretic loop varies as the load varies. The switching frequency can be approximated using

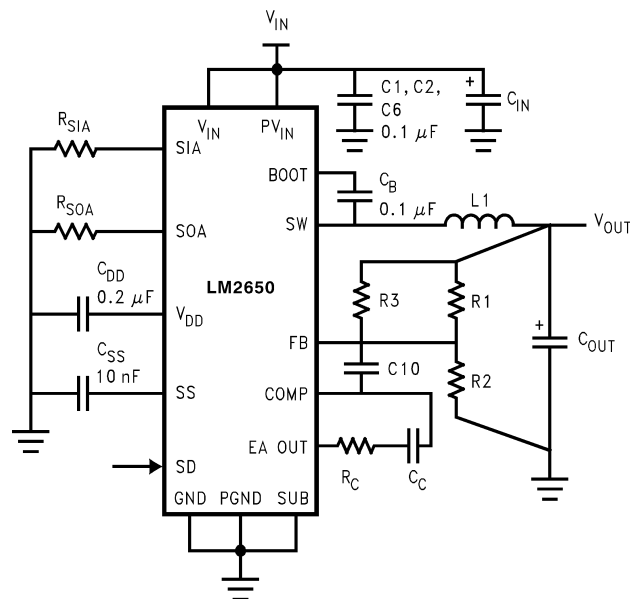
$$f = \frac{I}{(C_{OUT} \times V_{OUT\_PP})} \quad (6)$$

Here  $f$  is the switching frequency in hertz,  $I$  is the load current in amperes,  $C_{OUT}$  is the value of the capacitor in farads, and  $V_{OUT\_PP}$  is the magnitude of the AC ripple voltage in volts. Typical switching frequencies range anywhere from a few hertz for very light loads to a few thousand hertz for light loads bordering on the moderate level.

## Application Circuits

Figure 4 is a schematic of the typical application circuit. Use the component values shown in the figure and those contained in Table 1 to build a 5V, 3A, or 3.3V, 3A step-down DC/DC converter. As with the design of any DC/DC converter, the design of these circuits involved tradeoffs between efficiency, size, and cost. Here more weight was given to efficiency than to size as evidenced by the low switching frequency which keeps switching losses low but pushes the value and size of the inductor up.

From a smaller circuit, use the component values shown in Figure 4 and those contained in Table 3. These circuits trade slightly higher switching losses for a much smaller inductor. Note, Figure 4 does not show  $R_{FA}$ , the resistor required to adjust the switching frequency from 90 kHz up to 200 kHz. Connect  $R_{FA}$  between the FREQ ADJ pin and ground.



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FIGURE 4. The Typical 90 kHz Application Circuit

## Application Circuits (Continued)

**TABLE 1. Components for the Typical 90 kHz Application Circuit**

Input Voltage	7V to 18V IN	
Applicable Cell Stacks	8 to 12 Cell NiCd or NiMh, 3 to 4 Cell Li Ion, 8 to 11 Cell Alkaline, 6 Cell Lead Acid	
Output	5V, 3A Out	3.3V, 3A out
Input Capacitor $C_{IN}$	2 x 22 $\mu$ F, 35V AVX TPS Series or Sprague 593D Series	2 x 22 $\mu$ F, 35V AVX TPS Series or Sprague 593D Series
Inductor L1	40 $\mu$ H (See Table 2)	33 $\mu$ H (See Table 2)
Output Capacitor $C_{OUT}$	3x220 $\mu$ F, 10V AVX TPS Series or Sprague 593D Series	3x220 $\mu$ F, 10V AVX TPS Series or Sprague 593D Series
Feedback Resistors R1 and R2	R1 = 75k $\Omega$ , 1%, R2 = 24.9k $\Omega$ , 1%,	R1 = 41.2k $\Omega$ , 1%, R2 = 24.9k $\Omega$ , 1%,
Compensation Components $R_C$ , $C_C$ , $R_3$ , and $C_{10}$	$R_C$ = 37.4 k $\Omega$ , $C_C$ = 4.7 nF, $R_3$ = 3.57 k $\Omega$ , $C_{10}$ = 5.6 nF	$R_C$ = 23.2 k $\Omega$ , $C_C$ = 8.2 nF, $R_3$ = 2.0 k $\Omega$ , $C_{10}$ = 10 nF
Sleep Resistors $R_{SIA}$ and $R_{SOA}$	$R_{SIA}$ = 33 k $\Omega$ , $R_{SOA}$ = 200 k $\Omega$	$R_{SIA}$ = 39 k $\Omega$ , $R_{SOA}$ = 130 k $\Omega$

**TABLE 2. Toroidal Inductors Using Cores from MICROMETALS, INC.**

	Core Number	Core Material	Wire Gauge	Number of Strands	Number of Turns
15 $\mu$ H	T38	-52	AWG # 23	1	21
20 $\mu$ H	T38	-52	AWG # 23	1	25
33 $\mu$ H	T50	-52	AWG # 21	1	41
40 $\mu$ H	T50 (B)	-18	AWG # 21	1	41

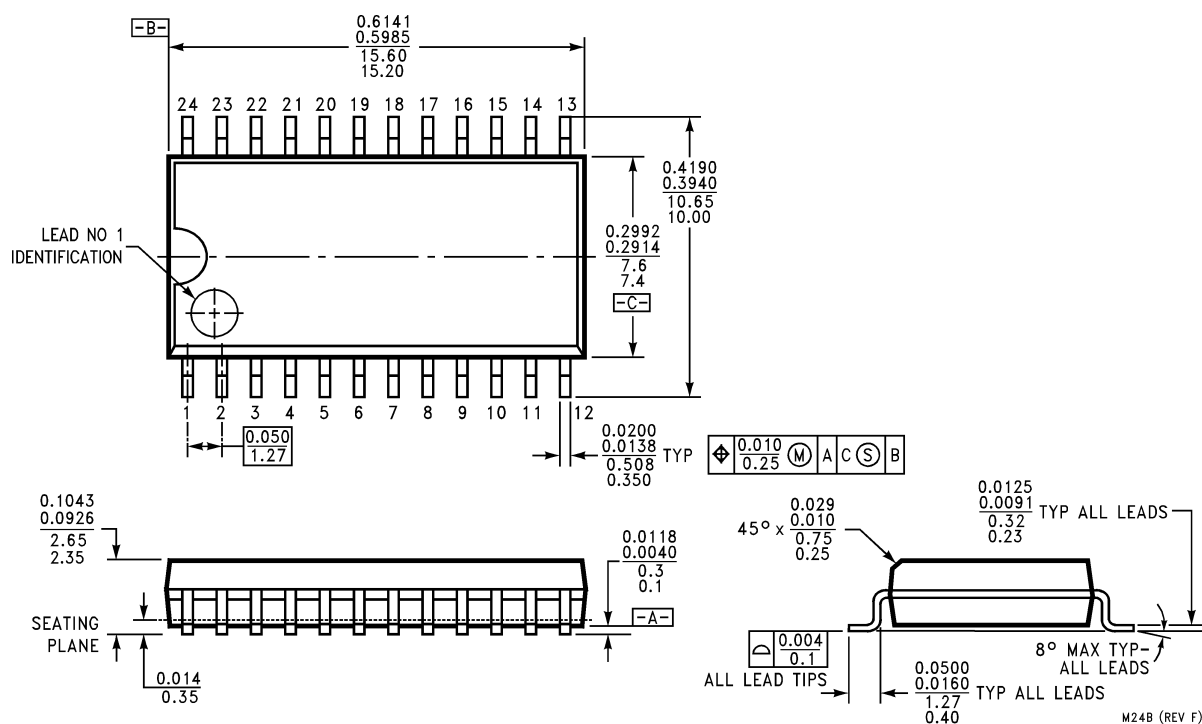
MICROMETALS  
5615 E. La Palma Ave. Anaheim, CA 92807 USA (800) 356-5977

**TABLE 3. Components for Typical 200 kHz Applications**

Input Voltage	7V to 18V IN	
Applicable Cell Stacks	8 to 12 Cell NiCd or NiMh, 3 to 4 Cell Li Ion, 8 to 11 Cell Alkaline, 6 Cell Lead Acid	
Output	5V, 3A Out	3.3V, 3A out
Input Capacitor $C_{IN}$	2 x 22 $\mu$ F, 35V AVX TPS Series or Sprague 593D Series	2 x 22 $\mu$ F, 35V AVX TPS Series or Sprague 593D Series
Inductor L1	20 $\mu$ H (See Table 2)	15 $\mu$ H (See Table 2)
Output Capacitor $C_{OUT}$	3x220 $\mu$ F, 10V AVX TPS Series or Sprague 593D Series	3x220 $\mu$ F, 10V AVX TPS Series or Sprague 593D Series
Feedback Resistors R1 and R2	R1 = 75k $\Omega$ , 1%, R2 = 24.9k $\Omega$ , 1%,	R1 = 41.2k $\Omega$ , 1%, R2 = 24.9k $\Omega$ , 1%,
Compensation Components $R_C$ , $C_C$ , $R_3$ , and $C_{10}$	$R_C$ = 53.6 k $\Omega$ , $C_C$ = 2.7 nF, $R_3$ = 4.02 k $\Omega$ , $C_{10}$ = 4.7 nF	$R_C$ = 33.2 k $\Omega$ , $C_C$ = 3.9 nF, $R_3$ = 3.01 k $\Omega$ , $C_{10}$ = 6.8 nF
Sleep Resistors $R_{SIA}$ and $R_{SOA}$	$R_{SIA}$ = 33 k $\Omega$ , $R_{SOA}$ = 200 k $\Omega$	$R_{SIA}$ = 47 k $\Omega$ , $R_{SOA}$ = 91 k $\Omega$
Frequency Adjusting Resistor $R_{FA}$	$R_{FA}$ = 24.9 k $\Omega$	$R_{FA}$ = 24.9 k $\Omega$



### FIGURE 5. An Efficient, 2% Accurate 5V to 3.3V Converter



**24-Lead Small-Outline Package (M)**  
**Order Number LM2650M-ADJ**  
**NS Package Number M24B**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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