

LM4548

AC '97 Rev 2 Codec with Sample Rate Conversion and National 3D Sound

General Description

The LM4548 is an audio codec for PC systems which is fully PC98 compliant and performs the analog intensive functions of the AC'97 Rev2 architecture. Using 18-bit Sigma-Delta A/D's and D/A's, the LM4548 provides 90dB of Dynamic Range.

The LM4548 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 4 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. The LM4548 also provides the additional True Line-Level output and National's 3D Sound stereo enhancement.

The LM4548 supports variable sample rate conversion as defined in the AC'97 Rev2 specification. The sample rate for the A/D and D/A can be programmed separately to convert any rate between 4kHz - 48kHz with a resolution of 1Hz. The AC'97 architecture separates the analog and digital functions of the PC audio system allowing both for system design flexibility and increased performance.

Key Specifications

| | |
|------------------------------|------------|
| ■ Analog Mixer Dynamic Range | 97dB (typ) |
| ■ D/A Dynamic Range | 89dB (typ) |
| ■ A/D Dynamic Range | 90dB (typ) |

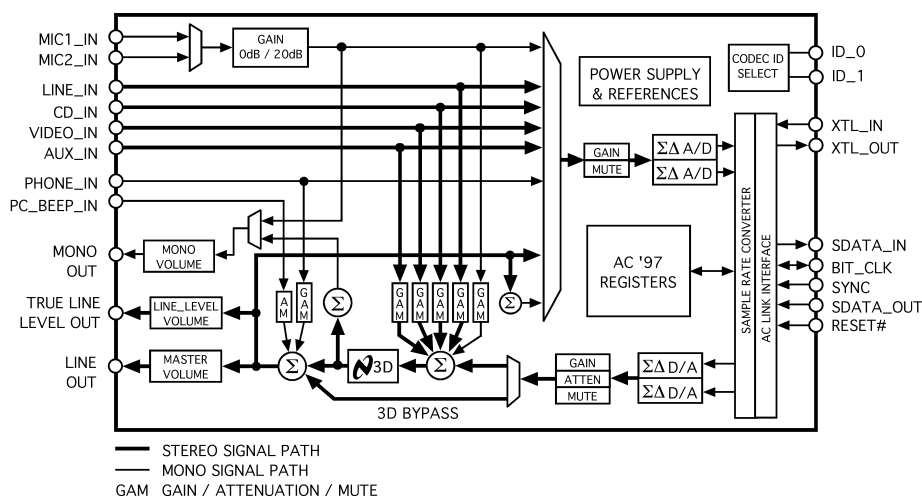
Features

- AC'97 Rev2 compliant
- National's 3D Sound circuitry
- High quality Sample Rate Conversion (SRC) from 4kHz to 48kHz in 1Hz increments.
- Multiple Codec Support
- True Line Level Output with volume control in addition to standard Line Out
- Advanced power management support
- Digital 3V and 5V compliant

Applications

- Desktop PC Audio Systems
- Portable PC Systems
- Mobile PC Systems

Block Diagram



DS100987-1

FIGURE 1. LM4548 Block Diagram

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------------|--------------------------|
| Supply Voltage | 6.0V |
| Storage Temperature | -40°C to +150°C |
| Input Voltage | -0.3V to $V_{DD} + 0.3V$ |
| ESD Susceptibility (Note 5) | 2500V |
| pins 27, 28 | 1500V |
| pin 3 | 750V |
| ESD Susceptibility (Note 6) | 200V |
| pin 3 | 100V |
| Junction Temperature | 150°C |

Soldering Information

| | |
|-----------------------|-------|
| TQFP Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

| | |
|------------------------------|--------|
| θ_{JA} (typ) — VBH48A | 74°C/W |
|------------------------------|--------|

Operating Ratings

| | |
|---------------------------------|-------------------------------|
| Temperature Range | |
| $T_{MIN} \leq T_A \leq T_{MAX}$ | -40°C $\leq T_A \leq$ 85°C |
| Analog Supply Range | 4.2V $\leq AV_{DD} \leq$ 5.5V |
| Digital Supply Range | 3.0V $\leq DV_{DD} \leq$ 5.5V |

Electrical Characteristics (Notes 1, 3)

The following specifications apply for $AV_{DD} = 5V$, $DV_{DD} = 5V$, $F_s = 48kHz$, single codec configuration, unless otherwise noted. Limits apply for $T_A = 25^\circ C$. The reference for 0dB is 1Vrms unless otherwise specified.

| Symbol | Parameter | Conditions | LM4548 | | Units (Limits) |
|-------------------------------------|--|--|------------------|----------------|--------------------|
| | | | Typical (Note 7) | Limit (Note 8) | |
| AV_{DD} | Analog Supply Range | | | 4.2 5.5 | V (min) V (max) |
| DV_{DD} | Digital Supply Range | | | 3.0 5.5 | V (min) V (max) |
| D_{IDD} | Digital Quiescent Power Supply Current | $DV_{DD} = 5V$ $DV_{DD} = 3.3V$ | 43 20 | | mA mA |
| A_{IDD} | Analog Quiescent Power Supply Current | | 53 | | mA |
| I_{DSD} | Digital Shutdown Current | | 500 | | μA |
| I_{ASD} | Analog Shutdown Current | | 30 | | μA |
| V_{REF} | Reference Voltage | | 2.23 | | V |
| PSRR | Power Supply Rejection Ratio | | 40 | | dB |
| Analog Loopthru Mode | | | | | |
| | Dynamic Range (Note 2) | CD Input to Line Output, -60dB Input THD+N, A-Weighted | 97 | 90 | dB (min) |
| THD | Total Harmonic Distortion | $V_O = -3dB$, $f = 1kHz$, $R_L = 10k\Omega$ | 0.01 | 0.02 | % (max) |
| Analog Input Section | | | | | |
| V_{IN} | Line Input Voltage | | 1 | | Vrms |
| | Mic Input with 20dB Gain | | 0.1 | | Vrms |
| | Mic Input with 0dB Gain | | 1 | | Vrms |
| Xtalk | Crosstalk | CD Left to Right | -95 | | dB |
| Z_{IN} | Input Impedance (Note 2) | | 40 | 10 | k Ω (min) |
| C_{IN} | Input Capacitance | | 15 | | pF |
| | Interchannel Gain Mismatch | CD Left to Right | 0.01 | | dB |
| Record Gain Amplifier - A/D | | | | | |
| A_S | Step Size | 0dB to 22.5dB | 1.5 | | dB |
| Mixer Section | | | | | |
| A_S | Step Size | +12dB to -34.5dB | 1.5 | | dB |
| A_M | Mute Attenuation | | 86 | | dB |
| Analog to Digital Converters | | | | | |
| | Resolution | | 18 | | Bits |

Electrical Characteristics (Notes 1, 3) (Continued)

The following specifications apply for $AV_{DD} = 5V$, $DV_{DD} = 5V$, $F_s = 48kHz$, single codec configuration, unless otherwise noted. Limits apply for $T_A = 25^\circ C$. The reference for 0dB is 1Vrms unless otherwise specified.

| Symbol | Parameter | Conditions | LM4548 | | Units (Limits) |
|--|-------------------------------------|---|---------------------|-------------------|-------------------|
| | | | Typical (Note 7) | Limit (Note 8) | |
| Analog to Digital Converters | | | | | |
| | Dynamic Range (Note 2) | -60dB Input THD+N, A-Weighted | 90 | 86 | dB (min) |
| | Frequency Response | -1dB Bandwidth | 20 | | kHz |
| Digital to Analog Converters | | | | | |
| | Resolution | | 18 | | Bits |
| | Dynamic Range (Note 2) | -60dB Input THD+N, A-Weighted | 89 | 85 | dB (min) |
| THD | Total Harmonic Distortion | V _{IN} = -3dB, f≈1kHz, R _L = 10kΩ | 0.01 | | % |
| | Frequency Response | | 20 - 21k | | Hz |
| | Group Delay (Note 2) | | | 2 | mS (max) |
| | Out of Band Energy | | -40 | | dB |
| | Stop Band Rejection | | 70 | | dB |
| D _T | Discrete Tones | | -96 | | dB |
| True Line Level Output Volume Section | | | | | |
| A _S | Step Size | 0dB to -46.5dB | 1.5 | | dB |
| A _M | Mute Attenuation | | 86 | | dB |
| Digital I/O (Note 2) | | | | | |
| V _{IL} | Low level input voltage | | | 0.30 x DVDD | V (max) |
| V _{HI} | High level input voltage | | | 0.40 x DVDD | V (min) |
| V _{OH} | High level output voltage | | | 0.50 x DVDD | V (min) |
| V _{OL} | Low level output voltage | | | 0.20 x DVDD | V (max) |
| I _L | Input Leakage Current | AC Link inputs | | ±10 | µA |
| I _L | Tri state Leakage Current | High impedance AC Link outputs | | ±10 | µA |
| I _{DR} | Output drive current | AC Link outputs | 5 | | mA |
| Digital Timing Specifications (Note 2) | | | | | |
| F _{BC} | BIT_CLK frequency | | 12.288 | | MHz |
| T _{BCP} | BIT_CLK period | | 81.4 | | nS |
| T _{CH} | BIT_CLK high | Variation of BIT_CLK period from 50% duty cycle | | ±20 | % (max) |
| F _{SYNC} | SYNC frequency | | 48 | | kHz |
| T _{SP} | SYNC period | | 20.8 | | µS |
| T _{SH} | SYNC high pulse width | | 1.3 | | µS |
| T _{SL} | SYNC low pulse width | | 19.5 | | µS |
| T _{SETUP} | Setup Time | SDATA_IN, SDATA_OUT to falling edge of BIT_CLK | | 15 | nS (min) |
| T _{HOLD} | Hold Time | Hold time of SDATA_IN, SDATA_OUT from falling edge of BIT_CLK | | 5 | nS (min) |
| T _{RISE} | Rise Time | BIT_CLK, SYNC, SDATA_IN or SDATA_OUT | | 6 | nS (max) |
| T _{FALL} | Fall Time | BIT_CLK, SYNC, SDATA_IN or SDATA_OUT | | 6 | nS (max) |
| T _{RST_LOW} | RESET# active low pulse width | For cold reset | | 1.0 | µS (min) |
| T _{RST2CLK} | RESET# inactive to BIT_CLK start up | For cold reset | | 162.8 | nS (min) |

Electrical Characteristics (Notes 1, 3) (Continued)

The following specifications apply for $AV_{DD} = 5V$, $DV_{DD} = 5V$, $F_s = 48kHz$, single codec configuration, unless otherwise noted. Limits apply for $T_A = 25^\circ C$. The reference for 0dB is 1Vrms unless otherwise specified.

| Symbol | Parameter | Conditions | LM4548 | | Units (Limits) |
|--|-----------------------------------|-------------------|---------------------|-------------------|-------------------|
| | | | Typical (Note 7) | Limit (Note 8) | |
| Digital Timing Specifications (Note 2) | | | | | |
| T _{SH} | SYNC active high pulse width | For warm reset | 1.3 | | μS |
| T _{SYNC2CLK} | SYNC inactive to BIT_CLK start up | For warm reset | | 162.8 | nS (min) |
| T _{SU2RST} | Setup to trailing edge of RESET# | For ATE Test Mode | | 15 | nS (min) |
| T _{RST2HZ} | Rising edge of RESET# to Hi-Z | For ATE Test Mode | | 25 | nS (max) |

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: These specifications are guaranteed by design and characterization; they are not production tested.

Note 3: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4548, $T_{JMAX} = 150^\circ C$. The typical junction-to-ambient thermal resistance is $74^\circ C/W$ for package number VBH48A.

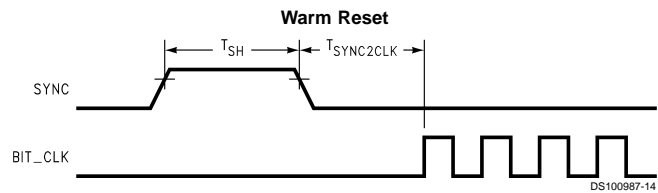
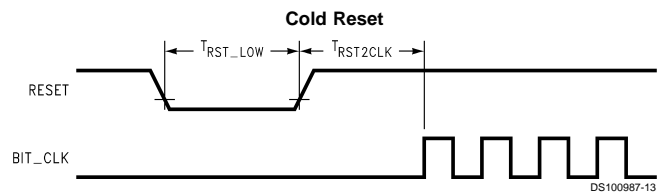
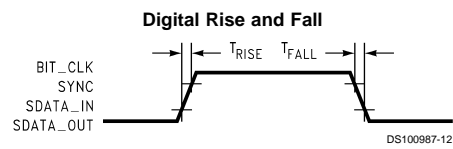
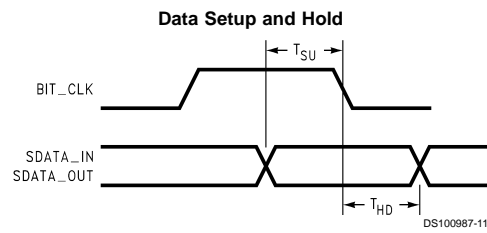
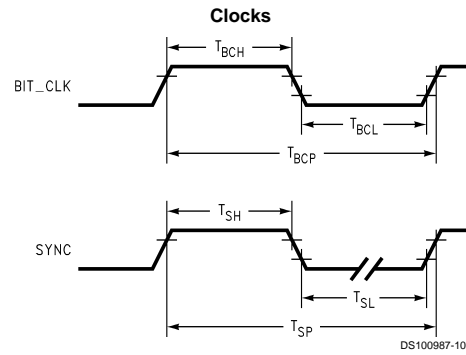
Note 5: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 6: Machine Model, 220 pF–240 pF discharged through all pins.

Note 7: Typicals are measured at $25^\circ C$ and represent the parametric norm.

Note 8: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Timing Diagrams



Typical Application

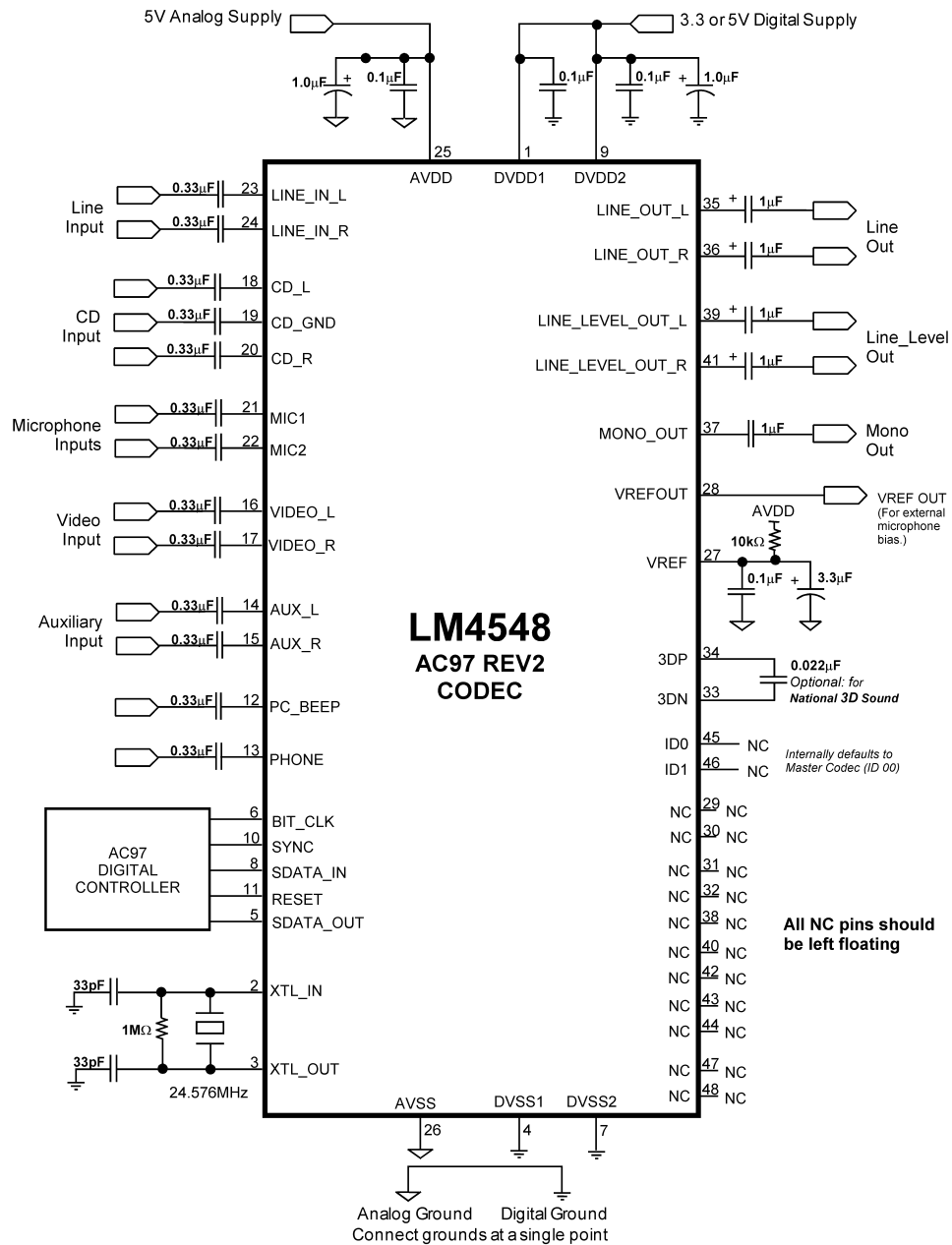
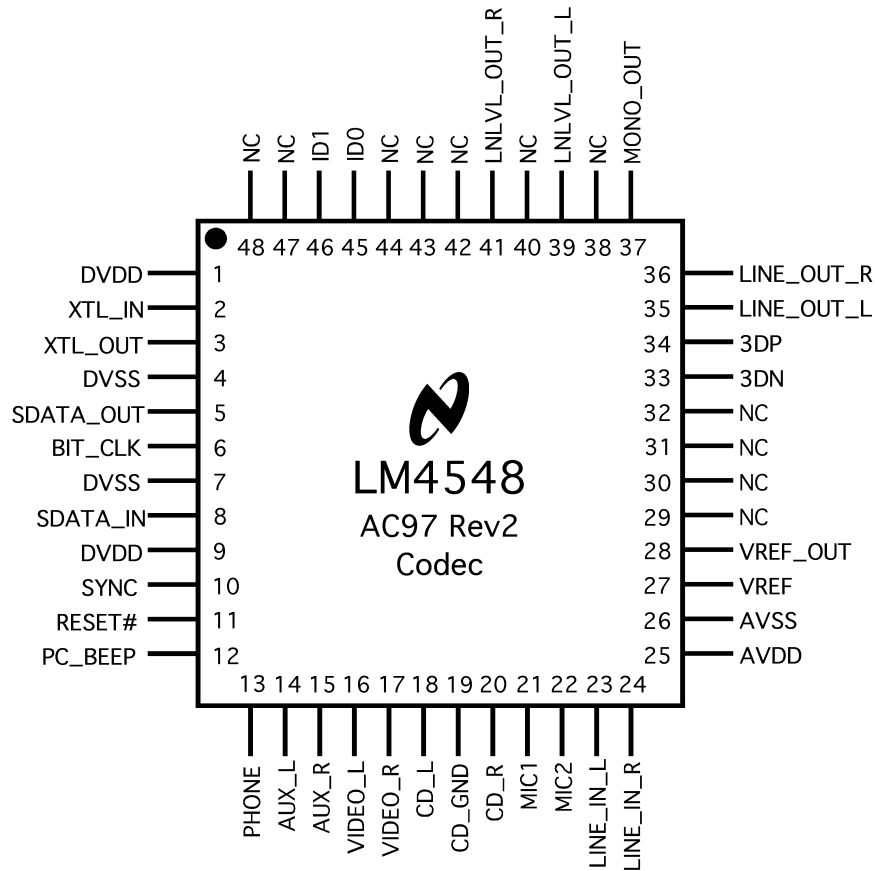


FIGURE 2. LM4548 Typical Application Circuit

DS100987-3

Connection Diagram



DS100987-2

Top View
Order Number LM4548VH
See NS Package Number VBH48A

Pin Description

Analog I/O

| Name | Pin | I / O | Functional Description |
|---------|-----|-------|--|
| PC_BEEP | 12 | I | This is a mono input which gets summed into both the stereo line out and the true line level out after the National 3D Sound block. The PC_BEEP level can be adjusted from 0dB to -45dB in 3dB steps, or muted, via register 0Ah. |
| PHONE | 13 | I | This is a mono input which gets summed into both the stereo line out and the true line level out after the National 3D Sound block. The PHONE level can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 0Ch. |
| AUX_L | 14 | I | This line level input can be routed through the Input Mux and recorded by the left ADC. In addition, this analog input gets summed into the left output stream. The amount of AUX_L signal mixed in the left output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 16h. |

Pin Description (Continued)

Analog I/O (Continued)

| Name | Pin | I / O | Functional Description |
|-------------|-----|-------|---|
| AUX_R | 15 | I | This line level input can be routed through the Input Mux and recorded by the right ADC. In addition, this analog input gets summed into the right output stream. The amount of AUX_R signal mixed in the right output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 16h. |
| VIDEO_L | 16 | I | This line level input can be routed through the Input Mux and recorded by the left ADC. In addition, this analog input gets summed into the left output stream. The amount of VIDEO_L signal mixed in the left output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 14h. |
| VIDEO_R | 17 | I | This line level input can be routed through the Input Mux and recorded by the right ADC. In addition, this analog input gets summed into the right output stream. The amount of VIDEO_R signal mixed in the right output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 14h. |
| CD_L | 18 | I | This line level input can be routed through the Input Mux and recorded by the left ADC. In addition, this analog input gets summed into the left output stream. The amount of CD_L signal mixed in the left output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 12h. |
| CD_GND | 19 | I | This input can be used to reject common mode signals on the CD_L and CD_R inputs. CD_GND is an AC ground point and not a DC ground point. This input must be AC-coupled to the source signal's ground. |
| CD_R | 20 | I | This line level input can be routed through the Input Mux and recorded by the right ADC. In addition, this analog input gets summed into the right output stream. The amount of CD_R signal mixed in the right output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 12h. |
| MIC1 | 21 | I | Either MIC1 or MIC2 can be selected via software and routed through the Input Mux for recording. The 20dB boost circuit is enabled/disabled via register 0Eh. Also, the amount of mic signal mixed in the output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 0Eh. |
| MIC2 | 22 | I | Either MIC1 or MIC2 can be selected via software and routed through the Input Mux for recording. The 20dB boost circuit is enabled/disabled via register 0Eh. Also, the amount of mic signal mixed in the output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 0Eh. |
| LINE_IN_L | 23 | I | This line level input can be routed through the Input Mux and recorded by the left ADC. In addition, this analog input gets summed into the left output stream. The amount of LINE_IN_L signal mixed in the left output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 10h. |
| LINE_IN_R | 24 | I | This line level input can be routed through the Input Mux and recorded by the right ADC. In addition, this analog input gets summed into the right output stream. The amount of LINE_IN_R signal mixed in the right output stream can be adjusted from +12dB to -34.5dB in 1.5dB steps as well as muted via register 10h. |
| LINE_OUT_L | 35 | O | This is a post-mixed output for the left audio channel. The level of this output can be adjusted from 0dB to -45dB in 1.5dB steps as well as muted via register 02h. |
| LINE_OUT_R | 36 | O | This is a post-mixed output for the right audio channel. The level of this output can be adjusted from 0dB to -45dB in 1.5dB steps as well as muted via register 02h. |
| MONO_OUT | 37 | O | This line level output is either the post-mixed output or the mic input. The level of this output can be adjusted from 0dB to -45dB in 1.5dB steps as well as muted via register 06h. |
| LNLVL_OUT_L | 39 | O | This is a post-mixed output for the left audio channel. The level of this output can be adjusted from 0dB to -45dB in 1.5dB steps as well as muted via register 04h. |
| LNLVL_OUT_R | 41 | O | This is a post-mixed output for the right audio channel. The level of this output can be adjusted from 0dB to -45dB in 1.5dB steps as well as muted via register 04h. |

Pin Description (Continued)

Digital I/O and Clocking

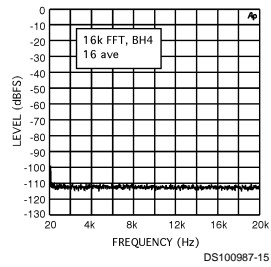
| Name | Pin | I / O | Functional Description |
|-----------|-----|-------|--|
| XTL_IN | 2 | I | 24.576 MHz crystal input. Use a fundamental-mode type crystal. When operating from a crystal, a 1M Ω resistor must be connected across pins 2 and 3. |
| XTL_OUT | 3 | O | 24.576 MHz crystal output. When operating from a crystal, a 1M Ω resistor must be connected across pins 2 and 3. |
| SDATA_OUT | 5 | I | This data stream contains both control data and DAC audio data. This input is sampled by the LM4548 on the falling edge of BIT_CLK. |
| BIT_CLK | 6 | I/O | OUTPUT when in Primary Codec Mode: This pin outputs a 12.288 MHz clock which is derived (internally divided by two) from the 24.576MHz crystal input (XTL_IN). INPUT when in Secondary Codec Mode (Multiple Codec configurations only): 12.288MHz clock is to be supplied from an external source, such as from the BIT_CLK of a Primary Codec. |
| SDATA_IN | 8 | O | This data stream contains both control data and ADC audio data. This output is clocked out by the LM4548 on the rising edge of BIT_CLK. |
| SYNC | 10 | I | 48kHz sync pulse which signifies the beginning of both the SDATA_IN and SDATA_OUT serial streams. SYNC must be synchronous to BIT_CLK. |
| RESET# | 11 | I | This active low signal causes a hardware reset which returns the control registers to their default conditions. |
| ID0 | 45 | I | ID0 and ID1 set the codec address for multiple codec use where ID0 is the LSB. Connect these pins to DVdd or GND as required. If these pins are not connected (NC), they default to Master Codec setting (same as connecting both pins to GND). These pins are of the same polarity as their internal ID0, ID1 registers. If pin 45 is connected to GND, then ID0 will be set to "0" internally. Connection to DVdd corresponds to a "1" internally. |
| ID1 | 46 | I | ID0 and ID1 set the codec address for multiple codec use where ID1 is the MSB. Connect these pins to DVdd or GND as required. If these pins are not connected (NC), they default to Master Codec setting (same as connecting both pins to GND). These pins are of the same polarity as their internal ID0, ID1 registers. If pin46 is connected to GND, then ID1 will be set to "0" internally. Connection to DVdd corresponds to a "1" internally. |

Power Supplies and References

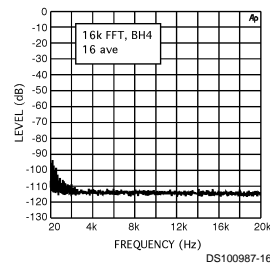
| Name | Pin | I / O | Functional Description |
|----------|-------|-------|--|
| AVDD | 25 | I | Analog supply. |
| AVSS | 26 | I | Analog ground. |
| DVDD | 1,9 | I | Digital supply. |
| DVSS | 4,7 | I | Digital ground. |
| VREF | 27 | O | Nominal 2.2V reference output. Not intended to sink or source current. Bypassing of this pin should be done with short traces to maximize performance. |
| VREFOUT | 28 | O | Nominal 2.2V reference output. Can source up to 5mA of current and can be used to bias a microphone. |
| AFILT1 | 29 | O | This pin is not used and should be left open (NC). However, a capacitor to ground on this pin is permitted - it will not affect performance. |
| AFILT2 | 30 | O | This pin is not used and should be left open (NC). However, a capacitor to ground on this pin is permitted - it will not affect performance. |
| 3DP, 3DN | 33,34 | O | These pins are used to complete the National 3D Sound circuit. Connect a 0.022 μ F capacitor between pins 3DP and 3DN. The National 3D Sound can be turned on and off via bit D13 in control register 20h. This is a fixed-depth type stereo enhance circuit, thus writing to register 22h has no effect. If National 3D Sound is not needed, then these pins should be left as no connect (NC). |

Typical Performance Characteristics

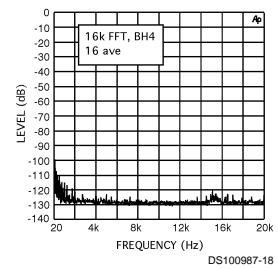
ADC Noise Floor



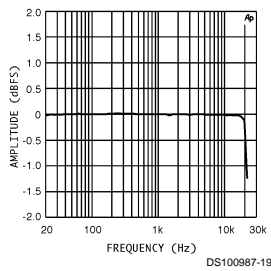
DAC Noise Floor



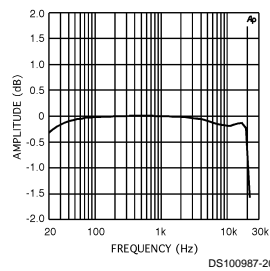
Analog Loopthru Noise Floor



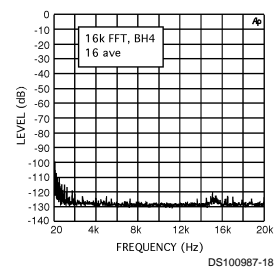
ADC Frequency Response



DAC Frequency Response



True Line Level Out Noise Floor (Analog Loopthrough)



LM4548 Register Map

| REG | Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|--------------------------------|------|------|------|------|------|------|-----|-----|------|------|-----|-----|-----|-----|-----|-----|---------|
| 00h | Reset | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0d50h |
| 02h | Master Volume | Mute | X | X | ML4 | ML3 | ML2 | ML1 | ML0 | X | X | X | MR4 | MR3 | MR2 | MR1 | MR0 | 8008h |
| 04h | True Line Level Out Volume | Mute | X | X | ML4 | ML3 | ML2 | ML1 | ML0 | X | X | X | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h |
| 06h | Master Volume Mono | Mute | X | X | X | X | X | X | X | X | X | X | MM4 | MM3 | MM2 | MM1 | MM0 | 8000h |
| 08h | Reserved | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0000h |
| 0Ah | PC BEEP Volume | Mute | X | X | X | X | X | X | X | X | X | X | PV3 | PV2 | PV1 | PV0 | X | 0000h |
| 0Ch | Phone Volume | Mute | X | X | X | X | X | X | X | X | X | X | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 0Eh | Mic Volume | Mute | X | X | X | X | X | X | X | X | 20dB | X | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 10h | Line In Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 12h | CD Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 14h | Video Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 16h | Aux Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 18h | PCM Out Vol | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 1Ah | Record Select | X | X | X | X | X | SL2 | SL1 | SL0 | X | X | X | X | X | SR2 | SR1 | SR0 | 0000h |
| 1Ch | Record Gain | Mute | X | X | X | GL3 | GL2 | GL1 | GL0 | X | X | X | X | GR3 | GR2 | GR1 | GR0 | 8000h |
| 1Eh | Reserved | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0000h |
| 20h | General Purpose | POP | X | 3D | X | X | X | MIX | MS | LPBK | X | X | X | X | X | X | X | 0000h |
| 22h | 3D Control (3D is fixed depth) | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0000h |
| 24h | Reserved | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0000h |
| 26h | Powerdown Ctrl/Stat | X | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | X | X | X | X | REF | ANL | DAC | ADC | na |
| 28h | Extended Audio ID | ID1 | ID0 | X | X | X | X | X | 0 | 0 | 0 | X | X | 0 | X | 0 | 1 | X001h |
| 2Ah | Extended Audio Status/Control | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | VRA | XXX0h |
| 2Ch | PCM Front DAC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h |
| 32h | PCM ADC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h |
| 5Ah | Vendor Reserved | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 7Ah | Vendor Reserved | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 7Ch | Vendor ID1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 4E53h |
| 7Eh | Vendor ID2 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4300h |

Application Information

AC Link Serial Interface Protocol

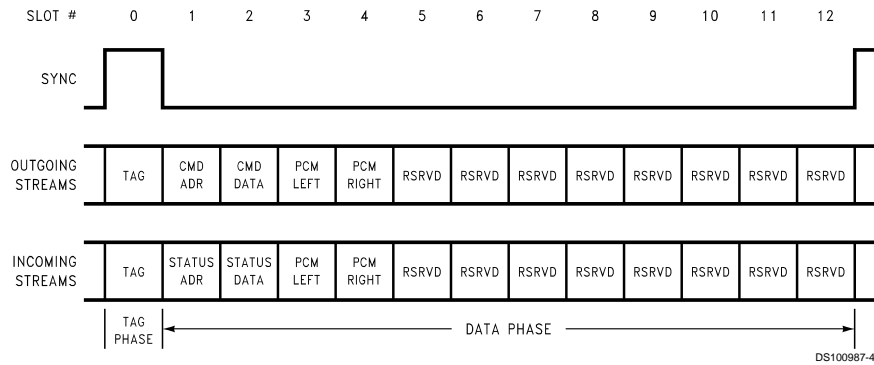


FIGURE 3. AC '97 Bidirectional Audio Frame

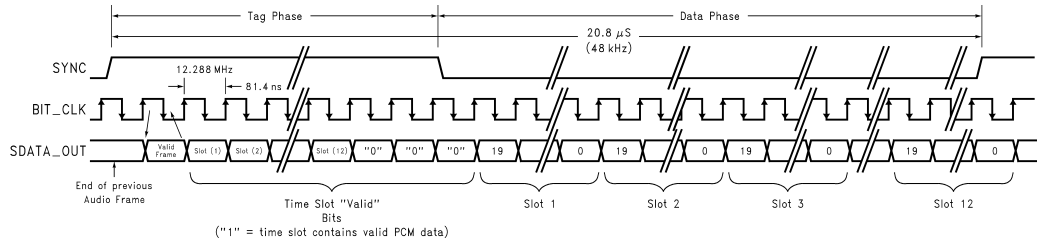


FIGURE 4. AC Link Audio Output Frame

AC Link Output Frame: SDATA_OUT (output from controller, input to LM4548)

The audio output frame (output from AC '97 Controller) contains control and PCM data targeted for the LM4548 control registers and stereo DAC. The Tag slot, slot 0, contains 16 bits that tell the AC Link interface circuitry on the LM4548 the validity of the following data slots.

A new audio output frame is signaled with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the next rising edge of BIT_CLK, the AC '97 Controller drives SDATA_OUT with the first bit of slot 0. The LM4548 samples SDATA_OUT on the falling edge of BIT_CLK. The AC '97 Controller will continue outputting the SDATA_OUT stream on each successive rising edge of BIT_CLK.

SDATA_OUT Slot 0: Tag Phase

The first bit of slot 0 is designated the "Valid Frame" bit. If this bit is 1, it indicates that the current data frame contains at least one slot of valid data and the LM4548 will further sample the next four bits to determine which frames do in fact have valid data. Valid slots are signified by a 1 in their respective slot bit position.

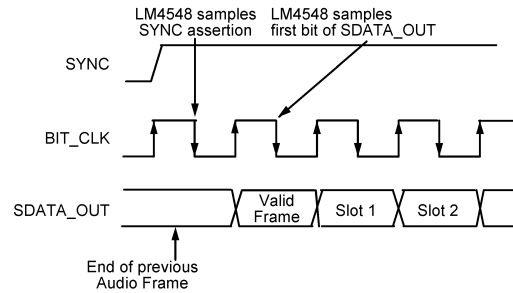


FIGURE 5. Start of Audio Output Frame

| Bit | Description | Comment |
|-----|--------------------------|--------------------------------|
| 15 | Valid Frame | 1 = This frame has valid data. |
| 14 | Control register address | 1 = Control Address is valid. |
| 13 | Control register data | 1 = Control Data is valid. |
| 12 | Left Playback PCM Data | 1 = Left PCM Data is valid. |

Application Information (Continued)

| Bit | Description | Comment |
|-----|-------------------------|------------------------------|
| 11 | Right Playback PCM Data | 1 = Right PCM Data is valid. |

SDATA_OUT Slot 1: Control Address

Slot 1 is used both to write to the LM4548 registers as well as read back a register's current value. The MSB of Slot 1 (bit 19) signifies whether the current control operation is a read or a write. Bits 18 through 12 are used to specify the register address of the read or write operation. The least significant twelve bits are reserved and should be stuffed with zeros by the AC'97 controller.

| Bits | Description | Comment |
|-------|------------------|---------------------------------|
| 19 | Read/Write | 0 = Read, 1 = Write |
| 18:12 | Control Register | Identifies the Control Register |
| 11:0 | Reserved | Set to "0" |

SDATA_OUT Slot 2: Control Data

Slot 2 is used to transmit 16 bit control data to the LM4548 in the event that the current operation is a write operation. The least significant four bits should be stuffed with zeros by the AC '97 controller. If the current operation is a register read, the entire slot, bits 19 through 0 should be stuffed with zeros.

| Bits | Description | Comment |
|------|-----------------------------|-----------------------------------|
| 19:4 | Control Register Write Data | Set bits to "0" if read operation |
| 3:0 | Reserved | Set to "0" |

SDATA_OUT Slot 3: PCM Playback Left Channel

Slot 3 is a 20 bit field used to transmit data intended for the left DAC on the LM4548. Any unused bits should be padded with zeros. The LM4548 DAC's have 18 bit resolution and thus will use the first 18 bits of the 20 bit PCM stream.

| Bits | Description | Comment |
|------|-----------------------------|------------------------|
| 19:0 | PCM Audio Data for Left DAC | Set unused bits to "0" |

SDATA_OUT Slot 4: PCM Playback Right Channel

Slot 4 is a 20 bit field used to transmit data intended for the right DAC on the LM4548. Any unused bits should be padded with zeros. The LM4548 DAC's have 18 bit resolution and thus will use the first 18 bits of the 20 bit PCM stream.

| Bits | Description | Comment |
|------|------------------------------|------------------------|
| 19:0 | PCM Audio Data for Right DAC | Set unused bits to "0" |

SDATA_OUT Slots 5-12: Reserved

Set these SDATA_OUT slots to "0" as they are not currently implemented and are reserved for future use.

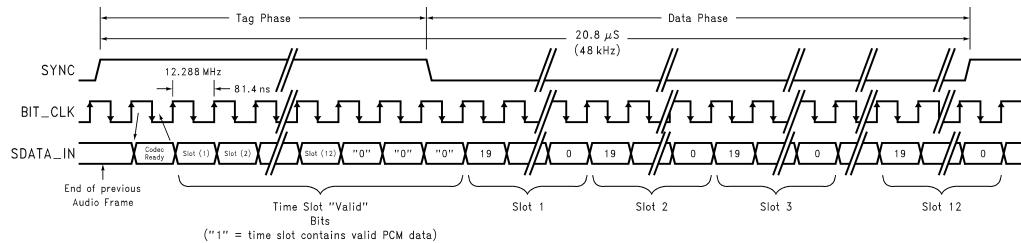


FIGURE 6. AC Link Audio Input Frame

AC Link Input Frame: SDATA_IN (input to controller, output from LM4548)

The audio input frame (input to the AC '97 Digital Controller) contains status and PCM data from the LM4548 control registers and stereo ADC. The Tag slot, slot 0, contains 16 bits that tell the AC '97 Digital Controller whether the LM4548 is ready and the validity of data from certain device subsections.

A new audio input frame is signaled with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the next rising edge of BIT_CLK, the LM4548 drives SDATA_IN with the first bit of slot 0. The Digital Controller samples SDATA_IN on the falling edge of BIT_CLK. The LM4548 will continue outputting the SDATA_IN stream on each successive rising edge of BIT_CLK. The LM4548 outputs data MSB first, in a MSB justified format. All reserved bits and slots are stuffed with "0" 's by the LM4548.

SDATA_IN Slot 0: Codec Status Bits

The first bit of SDATA_IN Slot 0 (bit 15) indicates when the Codec is ready. The digital controller must probe further to see which other subsections are ready.

Application Information (Continued)

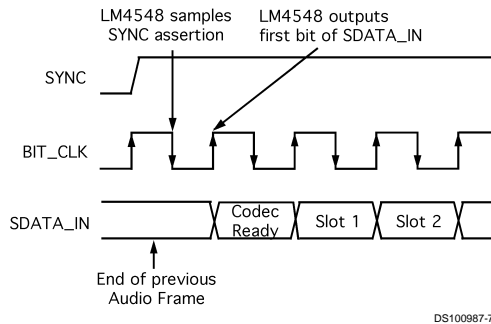


FIGURE 7. Start of Audio Input Frame

| Bit | Description | Comment |
|-----|-------------------|-------------------------------|
| 15 | Codec Ready Bit | 0=Not Ready, 1=Ready |
| 14 | Slot 1 data valid | Status Address is valid |
| 13 | Slot 2 data valid | Status Data is valid |
| 12 | Slot 3 data valid | Left Audio PCM Data is valid |
| 11 | Slot 4 data valid | Right Audio PCM Data is valid |

SDATA_IN Slot 1: Status Address / Slot Request Bits

This slot echoes the control register which a read was requested on. The address echoed was initiated by a read request in the previous SDATA_OUT frame, slot 1. Bits 11 and 10 are slot request bits that support Sample Rate Conversion (SRC) functionality. If bit 11 is set to 0, then the controller should respond with a valid PCM left sample in slot 3 of the next frame. If bit 10 is set to 0, then the controller should respond with a valid PCM right sample in slot 4 of the next frame. If bits 11 or 10 are set to 1, the controller should not send data in the next frame. Bits 9 through 2 are unused. Bits 1 and 0 are reserved and should be set to 0.

| Bits | Description | Comment |
|-------|--------------------------------|--|
| 19 | Reserved | Stuffed with "0" |
| 18:12 | Control Register Index | Echo of Control Register for which data is being returned. |
| 11 | Slot 3 Request bit (PCM left) | 0 = Controller should send valid slot 3 data in the next frame, 1 = Controller should not send slot 3 data in the next frame |
| 10 | Slot 4 Request bit (PCM right) | 0 = Controller should send valid slot 4 data in the next frame, 1 = Controller should not send slot 4 data in the next frame |

| Bits | Description | Comment |
|------|-------------------------|----------------|
| 9:2 | Other Slot Request bits | Unused |
| 1,0 | Reserved | Stuff with "0" |

SDATA_IN Slot 2: Status Data

The slot returns the control register data. The data returned was initiated by a read request in the previous SDATA_OUT frame, slot 1.

| Bits | Description | Comment |
|------|----------------------------|---------------------|
| 19:4 | Control Register Read Data | |
| 3:0 | Reserved | Stuffed with "0" 's |

SDATA_IN Slot 3: PCM Record Left Channel

This slot contains the left ADC sample data. The signal to be digitized is selected via register 1Ah and subsequently routed through the Input Mux for recording by the left ADC. This is a 20-bit slot, where the digitized 18-bit PCM data is output from the codec MSB first and the last remaining 2 bits will zeros.

| Bits | Description | Comment |
|------|------------------------------|-----------------------------------|
| 19:2 | PCM Record Left Channel data | 18 bit audio sample from left ADC |
| 1:0 | Reserved | Stuffed with "0" 's |

SDATA_IN Slot 4: PCM Record Right Channel

This slot contains the right ADC sample data. The signal digitized is selected via register 1Ah and subsequently routed through the Input Mux for recording by the right ADC. This is a 20-bit slot, where the digitized 18-bit PCM data is output from the codec MSB first and the last remaining 2 bits will zeros.

| Bits | Description | Comment |
|------|-------------------------------|------------------------------------|
| 19:2 | PCM Record Right Channel data | 18 bit audio sample from right ADC |
| 1:0 | Reserved | Stuffed with "0" 's |

SDATA_IN Slots 5-12: Reserved

These SDATA_IN slots are set to "0" as they are reserved for future use.

AC Link Low Power Mode

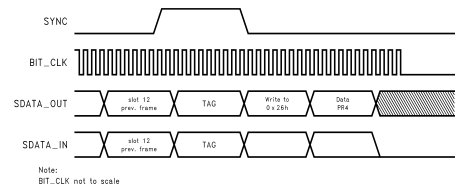


FIGURE 8. AC Link Powerdown Timing

Application Information (Continued)

Register Descriptions

Reset Register (00h)

Writing any value to this register causes a register reset which changes all of the registers back to their default values. If a read is performed on this register, the LM4548 will return a value of 0D50h indicating that National 3D Sound is implemented, 18bit data is supported for both the ADC's and DAC's, and the volume control for True Line Level Out is supported.

Master Volume Registers (02h, 04h, 06h)

These registers allow the output levels from LINE_OUT, LN_LVL_OUT and MONO_OUT to be attenuated or muted. There are 6-bits of volume control, plus one mute bit. It is a 5-bit volume range, where each step is nominally 1.5dB and each output can be individually muted by either setting the most significant bit (Mx5), and/or the mute bit (D15) to "1."

| Mute | Mx5:Mx0 | Function |
|----------------|---------|--------------------|
| 0 | 00 0000 | 0dB attenuation |
| 0 | 01 1111 | 46.5dB attenuation |
| 0 | 1X XXXX | 46.5dB attenuation |
| 1 | XX XXXX | mute |
| Default: 8000h | | |

PC Beep Register (0Ah)

This register controls the level of the PC_BEEP input. The PC_BEEP can be both attenuated and muted via register 0Ah. Step size is nominally 3dB. The signal present after the attenuation and mute block is summed into both the left and right channels.

| Mute | PV3:0 | Function |
|----------------|-------|------------------|
| 0 | 0000 | 0dB attenuation |
| 0 | 1111 | 45dB attenuation |
| 1 | XXXX | mute |
| Default: 0000h | | |

Mixer Input Volume Registers (Index 0Ch - 18h)

These registers set the input volume levels including mute. Each volume control is 5 bit which provides from a range of +12dB gain to 34.5dB attenuation in 1.5dB steps. For stereo ports, the left and right levels can be independently set. Muting a given port is accomplished by setting the MSB to 1. Setting the MSB to 1 for stereo ports mutes both the left and right channel. Register 0Eh has an additional 20dB boost for a microphone level input. This is enabled by setting bit 6 of register 0Eh to 1.

| Mute | Gx4:Gx0 | Function |
|---|---------|--------------------|
| 0 | 00000 | +12dB gain |
| 0 | 01000 | 0dB gain |
| 0 | 11111 | 34.5dB attenuation |
| 1 | XXXXX | mute |
| Default: 8008h (mono regs.), 8808h (stereo regs.) | | |

Record Select Register (1Ah)

This register independently controls the source for the right and left channel which will be recorded by the stereo ADC. The default value is 0000h which corresponds to Mic in.

| SL2:SL0 | Left Record Source |
|---------|--------------------|
| 0 | Mic |
| 1 | CD In (L) |
| 2 | Video In (L) |
| 3 | Aux In (L) |
| 4 | Line In (L) |
| 5 | Stereo Mix (L) |
| 6 | Mono Mix (L) |
| 7 | Phone |

| SR2:SR0 | Right Record Source |
|---------|---------------------|
| 0 | Mic |
| 1 | CD In (R) |
| 2 | Video In (R) |
| 3 | Aux In (R) |
| 4 | Line In (R) |
| 5 | Stereo Mix (R) |
| 6 | Mono Mix (R) |
| 7 | Phone |

Record (Input) Gain Register (1Ch)

This registers controls the Record (Input) Gain level for the stereo input selected via the Record Select Control Register (1Ah). The gain can be programmed from 0dB to +22.5dB in 1.5dB steps. The level for the left and right channel can be individually controlled. The input can also be muted by setting the MSB to 1.

| Mute | Gx3:Gx0 | Function |
|----------------|---------|-------------|
| 0 | 1111 | 22.5dB gain |
| 0 | 0000 | 0dB gain |
| 1 | XXXX | mute |
| Default: 8000h | | |

General Purpose Register (20h)

This register controls many miscellaneous functions implemented on the LM4548. The miscellaneous functions include POP which allows the PCM to bypass the National 3D Sound circuitry, 3D which enables or disables the National 3D Sound circuitry, MIX which selects the MONO_OUT source, MS which selects the microphone mux source and LPBK which connects the output of the stereo ADC to input of the stereo DAC. LPBK provides for a digital loopthru path when enabled.

| BIT | Function |
|------|--|
| POP | PCM out path and mute, 0 = pre 3D, 1 = post 3D |
| 3D | National 3D Sound on / off 1 = on |
| MIX | Mono output select 0 = Mix, 1 = Mic |
| MS | Mic select 0 = Mic1 1 = Mic2 |
| LPBK | ADC/DAC loopback |

Powerdown Control / Status Register (26h)

This read/write register is used to monitor subsystem readiness and also to program the LM4548 powerdown states. The lower half of this register is read only with a "1", indicating the subsection is ready. Writing to the lower 8 bits will have no effect.

Application Information (Continued)

When the AC Link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a "1", it indicates that the AC Link and AC '97 registers are in a fully operational state. The AC '97 Controller must further probe the Powerdown Control / Status Register to determine exactly which subsections are ready.

| BIT | Function |
|-----|------------------------------------|
| REF | Vref's up to nominal level |
| ANL | Analog mixers ready |
| DAC | DAC section ready to accept data |
| ADC | ADC section ready to transmit data |

Supported powerdown modes.

| BIT | Function |
|-----|--|
| PRO | PCM in ADC's and Input Mux powerdown |
| PR1 | PCM out DAC's powerdown |
| PR2 | Analog Mixer powerdown (VREF still on) |
| PR3 | Analog Mixer powerdown (VREF off) |
| PR4 | Digital Interface (AC Link) powerdown (external clk off) |
| PR5 | Internal Clk disable |
| PR6 | not used |

Extended Audio ID Register (28h)

This read only register identifies which AC97 Extended Audio features are supported. The LM4548 provides for VRA (Variable Rate Audio) and Multiple Codec support. VRA is indicated by a "1" in the LSB of register 28h. The two MSB's, ID1 and ID0, show the current codec configuration as connected via external pins 45 and 46.

| Pin46 (ID1) | Pin45 (ID0) | Reg 28h ID1 | Reg 28h ID0 | Codec Mode |
|--------------------|--------------------|-------------|-------------|-------------|
| NC (not connected) | NC (not connected) | 0 | 0 | Primary |
| GND | GND | 0 | 0 | Primary |
| GND | DVdd | 0 | 1 | Secondary 1 |
| DVdd | GND | 1 | 0 | Secondary 2 |
| DVdd | DVdd | 1 | 1 | Secondary 3 |

Extended Audio Status/Control Register (2Ah)

This read/write register provides status and control of the Variable Sample Rate function. Setting the LSB of this register to "1" enables Variable Rate Audio (VRA) mode and allows DAC and ADC sample rates to be programmed via registers 2Ch and 32h.

| BIT | Function |
|-----|---------------------------------------|
| VRA | 0 = VRA off (48kHz fixed), 1 = VRA on |

Sample Rate Control Registers (2Ch, 32h)

These read/write registers are used to set the sample rate for the left and right channels of the DAC (2Ch) and the ADC (32h). When Variable Rate Audio is enabled via bit-0 of Register 2Ah, the sample rates can be programmed, in 1Hz increments, to be any value from 4kHz to 48kHz. Below is a list of the most common sample rates and their corresponding register values.

| SR15:SR0 | Sample Rate (Hz) |
|----------|------------------|
| 1F40h | 8000 |

| SR15:SR0 | Sample Rate (Hz) |
|----------|------------------|
| 2B11h | 11025 |
| 3E80h | 16000 |
| 5622h | 22050 |
| AC44h | 44100 |
| BB80h | 48000 |

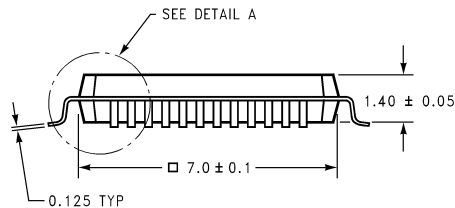
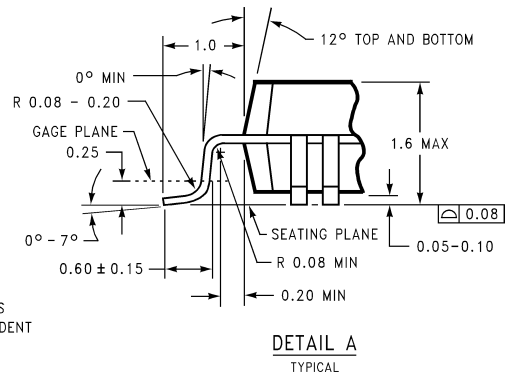
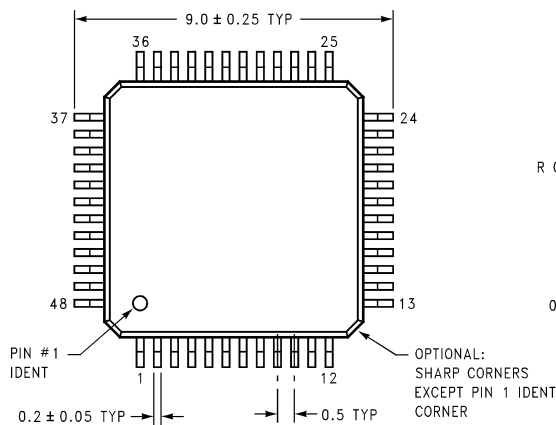
Reserved Registers

Do not write to these registers as they are reserved.



Physical Dimensions inches (millimeters) unless otherwise noted

METRIC ONLY



48-Lead, TQFP, 7 X 7 X 1.4mm, JEDEC (M)
Order Number LM4548VH
NS Package Number VBH48A

VBH48A (REV C)

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