

LM4921 Boomer[®] Audio Power Amplifier Series

Low Voltage I²S 16-Bit Stereo DAC with Stereo Headphone Power Amplifiers and Volume Control

General Description

The LM4921 combines a 16-bit resolution stereo I²S input digital-to-analog converter (DAC) with a stereo headphone audio power amplifier. It is primarily designed for demanding applications in mobile phones and other portable communication device applications. The LM4921 features an I²S serial interface for the digital audio information and a 16-bit SPI serial interface for internal register control and communication. With AV_{DD} and $DV_{DD} = 3.0V_{DC}$ and driving a 32Ω single-ended load to a $26mW_{RMS}$ output level the distortion (THD+N) of the LM4921 will be less than 0.5%. The LM4921 also features a programmable 32-step digital volume control accessed through an SPI interface.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is, therefore, ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4921 features a low-power consumption shutdown mode, and also has an internal thermal shutdown protection mechanism.

Key Specifications

■ PSRR at 217Hz, $A/DV_{DD} = 3V$, (Fig. 1)	52dB (typ)
■ P_{OUT} at $AV_{DD} = 3.0V$, 32Ω	
< 0.05% THD	13mW (typ)
< 0.5% THD	26mW (typ)
■ Supply voltage range	
DV_{DD}	2.6V to 5.0V
AV_{DD} (Note 8)	2.6V to 5.5V
■ Shutdown current	1 μ A (typ)

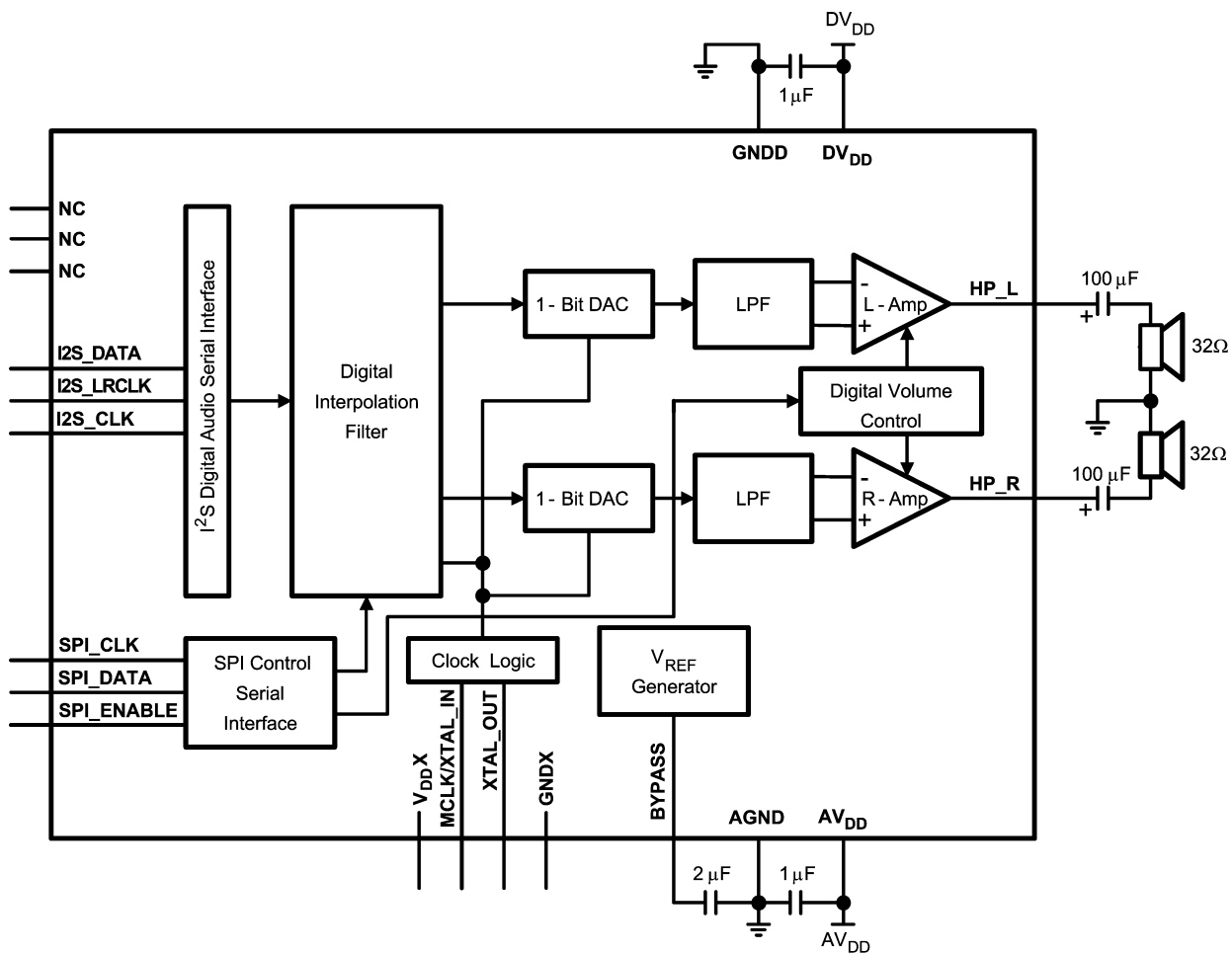
Features

- 16-bit resolution stereo DAC
- I²S digital audio data serial interface
- SPI serial interface (control register)
- Volume Control (32 steps; 1.5 dB increments)
- Up to 50mW/channel stereo headphone amplifier
- Zero Crossing Detection for Silent Attenuation Steps
- 2.6V_{DC} to 5.0V_{DC} digital supply voltage range
- 2.6V_{DC} to 5.5V_{DC} analog supply voltage range (Note 8)
- Unity-gain stable headphone amplifiers
- Available in the 20-bump microSMD package

Applications

- Mobile phones
- PDAs
- Portable electronic devices

Typical Application

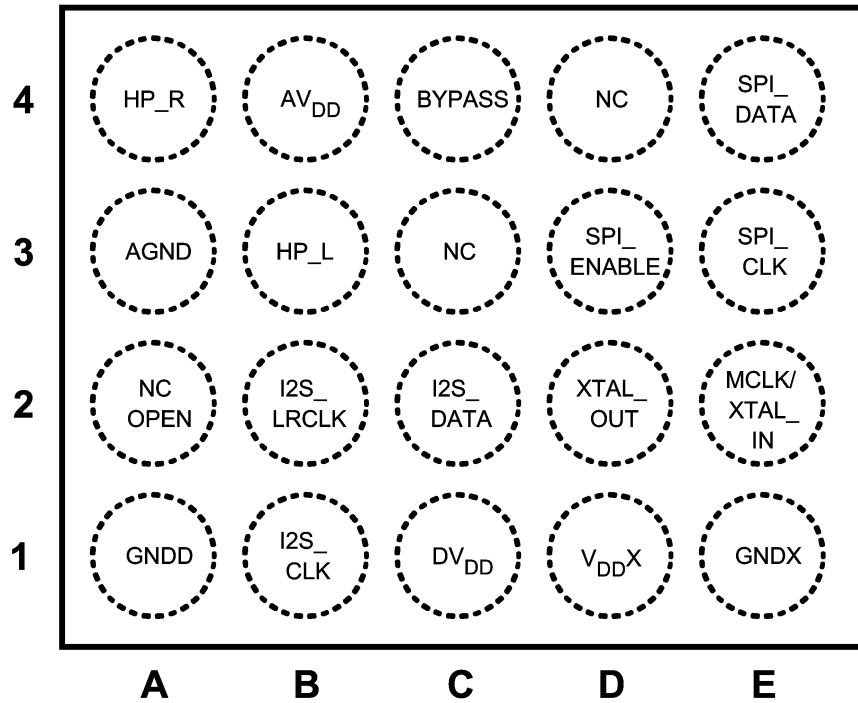


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FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

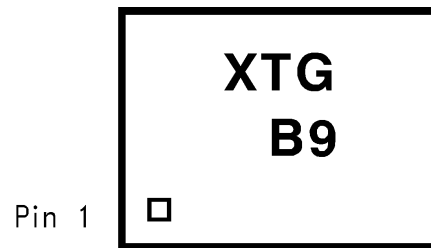
LM4921 Pin Configuration



200486F8

Top View
 20-Bump micro SMD
 Order Number LM4921ITL, LM4921ITLX
 See NS Package Number TLA20JKA
 NC - No Connection

20-Bump micro SMD Marking



200486F9

X - Date Code
 T - Die Traceability
 G - Boomer Family
 B9 - LM4921ITL

LM4921 I/O Pin Descriptions

PIN # (ITL)	PIN NAME	PIN TYPE Input-I, Output-O, Power-P, No Connect-NC	PIN DESCRIPTION
B1	I2S_CLK	I/O	I2S Clock
C2	I2S_DATA	I	I2S data
B2	I2S_WS	I/O	I2S L/R word select
E3	SPI_CLK	I	SPI clock
E4	SPI_DATA	I	SPI data
D3	SPI_ENABLE	I	SPI Enable
E2	MCLK/XTAL_IN	I	Master Clock / Xtal input
D2	XTAL_OUT	O	Xtal output
C4	BYPASS	I/O	Analog VDD/2 bypass capacitor connection point
B4	AV _{DD}	P	Analog supply
A3	AGND	P	Analog Ground
C1	DV _{DD}	P	Digital Supply
A1	GNDD	P	Digital ground
D1	VDDX	P	XTAL Oscillator circuit supply
E1	GNDX	P	XTAL Oscillator circuit ground
B3	HP_L	O	HP left output
A4	HP_R	O	HP right output
A2	No Connect	O	Must let float
C3	No Connect	NC	NC
D4	No Connect	NC	NC

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility	
Human body model (Note 4)	2000V
Machine model (Note 5)	200V

Junction Temperature	150°C
Thermal Resistance	
θ_{JA}	60°C/W

Operating Ratings

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
Supply Voltage		
DV_{DD}		$2.6V \leq DV_{DD} \leq 5.0V$
AV_{DD}		$2.6V \leq AV_{DD} \leq 5.5V$

Electrical Characteristics $DV_{DD} = 3.0V$, $AV_{DD} = 5.0V$, $R_L = 32\Omega$ (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4921		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
DV_{DD}	Digital Power Supply Voltage	Note 8	3.0		V
AV_{DD}	Analog Power Supply Voltage	Note 8	5.0		V
DI_{DD}	Digital Power Supply Quiescent Current	$R_{Load} = \infty$, $f_{MCLK} = 11.2896\text{MHz}$	3.5	7.5	mA (max)
AI_{DD}	Analog Power Supply Quiescent Current	$R_{Load} = \infty$, $f_{MCLK} = 0\text{MHz}$	6	10	mA (max)
I_{SD}	Total Shutdown Power Supply Current	SHUTDOWN SPI bits 1 & 2 set to logic 0, SPI, M_{CLK} and I^2S inputs at GND	1	5	$\mu\text{A}(\text{max})$
I_{SB}	Standby Current	Analog and Digital together All clocks off	25		μA
V_{FS}	Full-Scale Output Voltage	Gain set at max	3.5		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	$f_{IN} = 1\text{kHz}$, $P_{OUT} = 12\text{mW}$ (Vol Control = 11111, I^2S input adj to get 12mW at output)	0.03		%
P_O	Headphone Amplifier Output Power	THD = (0.5%), $f_{OUT} = 1\text{kHz}$	50	40	mW (min)
PSRR	Power Supply Rejection Ratio	$AV_{DD} C_{BYPASS} = 2.0\mu\text{F}$ $V_{RIPPLE} = 200\text{mV}_{P-P} 217\text{Hz}$	62	45	dB (min)
SNR	Signal-to-Noise Ratio	$f_{IN} = 1\text{kHz}$ sinewave at -60dB_{FS} , A-weighted- $f_{CONV} = 44.1\text{kHz}$	82		dB
DR	Dynamic Range	$f_{IN} = 1\text{kHz}$ sinewave at -60dB_{FS} , A-weighted	84		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Mismatch	$f_{IN} = 1\text{kHz}$	0.06		dB
X_{TALK}	Channel-to-Channel Crosstalk	$f_{CONV} = 44.1\text{kHz}$, $f_{IN} = 1\text{kHz}$ sinewave at -3dB_{FS}	72		dB
	Volume Control Range	Minimum Attenuation	+3.0		dB
		Maximum Attenuation	-43.5		dB
	Volume Control Control Step Size		1.5		dB
	Mute Attenuation		-102		dB

Electrical Characteristics $DV_{DD} = 3.0V$, $AV_{DD} = 3.0V$, $R_L = 32\Omega$ (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	LM4921		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
DV_{DD}	Digital Power Supply Voltage	Note 8	3.0		V
AV_{DD}	Analog Power Supply Voltage	Note 8	3.0		V
DI_{DD}	Digital Power Supply Quiescent Current	$R_{Load} = \infty$, $f_{MCLK} = 11.2896MHz$	3.5	7.5	mA (max)
AI_{DD}	Analog Power Supply Quiescent Current	$R_{Load} = \infty$, $f_{MCLK} = 0MHz$	5	9.0	mA (max)
I_{SD}	Total Shutdown Power Supply Current	SHUTDOWN SPI bits 1 & 2 set to logic 0, SPI, M_{CLK} and I^2S inputs at GND	1		μA (max)
I_{SB}	Standby Current	Analog and Digital together All clocks off	15		μA
V_{FS}	Full-Scale Output Voltage	Gain set at max	2.6		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	$f_{IN} = 1kHz$, $P_{OUT} = 12mW$ (Vol Cont = 11011, I^2S input adj to get 12mW at output)	0.05		%
P_O	Headphone Amplifier Output Power	THD = (0.5%), $f_{OUT} = 1kHz$	26		mW (min)
PSRR	Power Supply Rejection Ratio	$AV_{DD} C_{BYPASS} = 2.0\mu F$ $V_{RIPPLE} = 200mV_{P-P}$ 217Hz	52		dB (min)
SNR	Signal-to-Noise Ratio	$f_{IN} = 1kHz$ sinewave at $-60dB_{FS}$, A-weighted- $f_{CONV} = 44.1kHz$	79		dB
DR	Dynamic Range	$f_{IN} = 1kHz$ sinewave at $-60dB_{FS}$, A-weighted	81		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Mismatch	$f_{IN} = 1kHz$	0.06		dB
X_{TALK}	Channel-to-Channel Crosstalk	$f_{CONV} = 44.1kHz$, $f_{IN} = 1kHz$ sinewave at $-3dB_{FS}$	72		dB
	Volume Control Range	Minimum Attenuation Maximum Attenuation	0 -43.5		dB dB
	Volume Control Control Step Size		1.5		dB
	Mute Attenuation		-100		dB

Electrical Characteristics-Digital Inputs $DV_{DD} = 3.0V$ (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	LM4921		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
	Resolution		16		Bits
I ² S	Audio Data Interface Format	Standard, I ² S, Left Justified			
f _{MCLK}	Master Clock Frequency		11.2896 (256FS)		MHz
f _{CONV}	Sampling Clock Frequency Range		44.1	48	kHz
V _{IL}	Digital Input: Logic Low Voltage Level			0.3 X DV _{DD}	V (max)
V _{IH}	Digital Input: Logic High Voltage Level			0.7 X DV _{DD}	V (min)
t _{ES}	SPI_ENB Setup Time			20	ns (min)
t _{EH}	SPI_ENB Hold Time			20	ns (min)
t _{EL}	SPI_ENB Low Time			30	ns (min)
t _{DS}	SPI_Data Setup Time			20	ns (min)
t _{DH}	SPI_Data Hold Time			20	ns (min)
t _{CS}	SPI_CLK Setup Time			20	ns (min)
t _{CH}	SPI_CLK High Pulse Width			100	ns (min)
t _{CL}	SPI_CLK Low Pulse Width			100	ns (min)
f _{CLK}	SPI_CLK Frequency			5	MHz (max)
t _{CLKI²S}	I ² S_CLK Period			50	ns (min)
t _{HI²S}	I ² S_CLK High Pulse Width			20	ns (min)
t _{LO²S}	I ² S_CLK Low Pulse Width			20	ns (min)
	I ² S_LRCLK Duty Cycle		50		%
t _{SLRCLK}	I ² S_LRCLK to I ² S_CLK Setup Time			20	ns (min)
t _{HLRCLK}	I ² S_LRCLK to I ² S_CLK Hold Time			20	ns (min)
t _{SDI²S}	I ² S_Data to I ² S_CLK Setup Time			20	ns (min)
t _{HDI²S}	I ² S_Data to I ² S_CLK Hold Time			20	ns (min)

Note 1: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Note 4: Human body model, 100pF discharged through a 1.5k Ω resistor.

Note 5: Machine Model, 220pF – 240pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

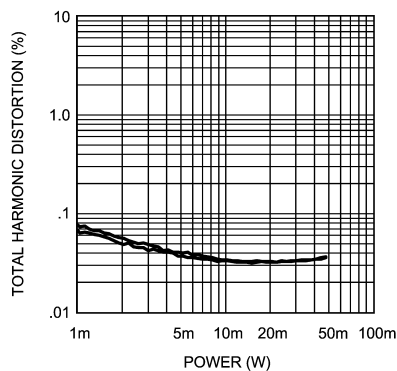
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Best operation is achieved by maintaining $3.0V \leq AV_{DD} \leq 5.0V$ and $3.0V \leq DV_{DD} \leq 5.0V$.

Note 9: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Typical Performance Characteristics

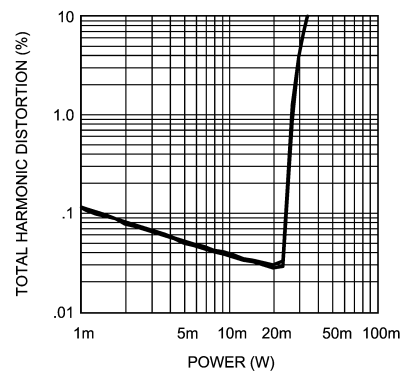
THD+N vs Output Power



200486G9

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, 44.1 kHz Sample Rate
 R & L Channels, Vol = 3dB, Frequency in = 1kHz

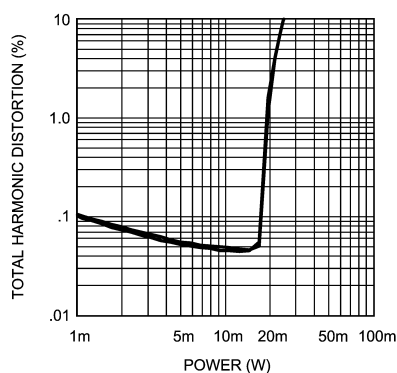
THD+N vs Output Power



200486G8

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, 44.1 kHz Sample Rate
 R & L Channels Shown, Vol = 3dB, Frequency in = 1kHz

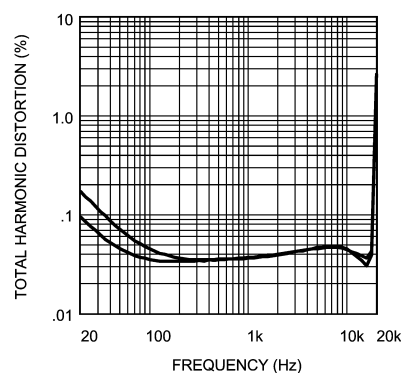
THD+N vs Output Power



200486G7

Analog $V_{DD} = 2.6V$, Digital $V_{DD} = 2.6V$
 $R_L = 32\Omega$, 44.1 kHz Sample Rate
 R & L Channels Shown, Vol = 3dB, Frequency in = 1kHz

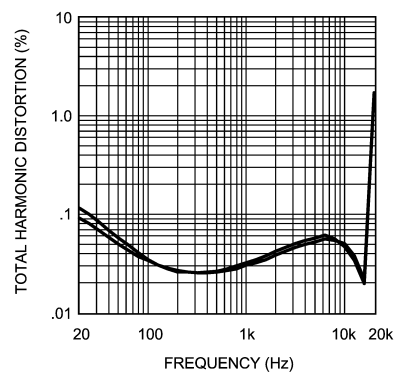
THD+N vs Frequency



200486G6

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Power Level = 50mW
 R & L Channels Shown, 44.1kHz Sample Rate

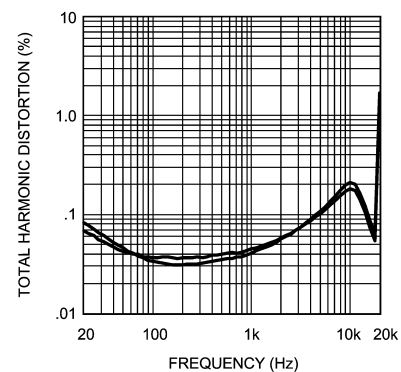
THD+N vs Frequency



200486G5

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Power Level = 12mW
 R & L Channels Shown, 44.1kHz Sample Rate

THD+N vs Frequency

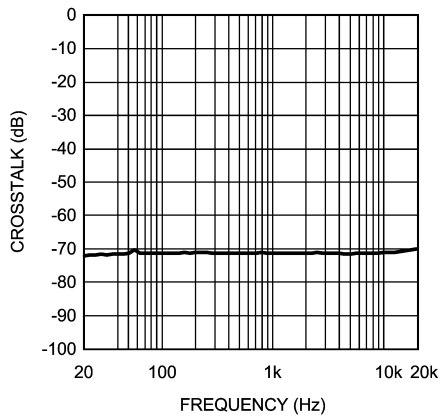


200486G4

Analog $V_{DD} = 2.6V$, Digital $V_{DD} = 2.6V$
 $R_L = 32\Omega$, Power Level = 12mW
 R & L Channels Shown, 44.1kHz Sample Rate

Typical Performance Characteristics (Continued)

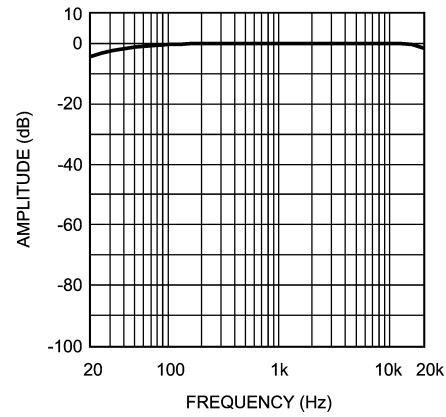
Crosstalk



200486C7

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, $V_{ol} = 3dB$
 44.1kHz Sample Rate, -3dB FFS

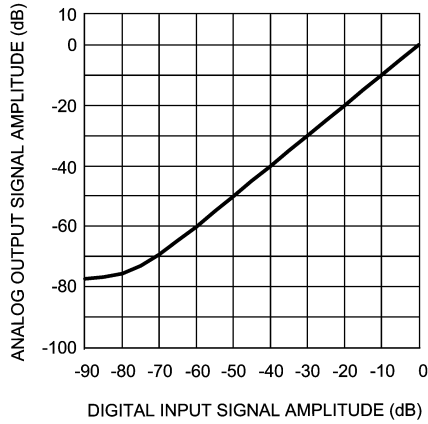
Frequency Response



200486E1

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, $V_{ol} = 0dB$
 44.1kHz Sample Rate, 0dB FFS

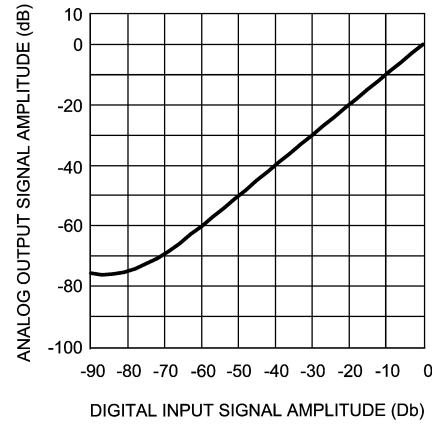
Linearity



200486E3

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, 44.1kHz Sample Rate

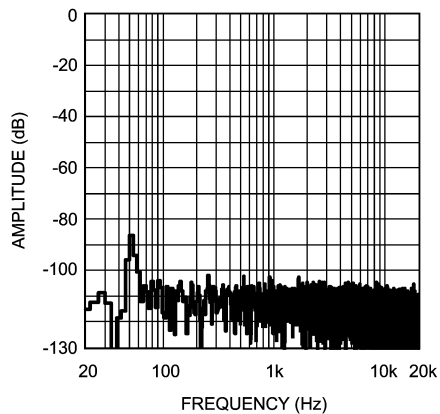
Linearity



200486E2

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, 44.1kHz Sample Rate

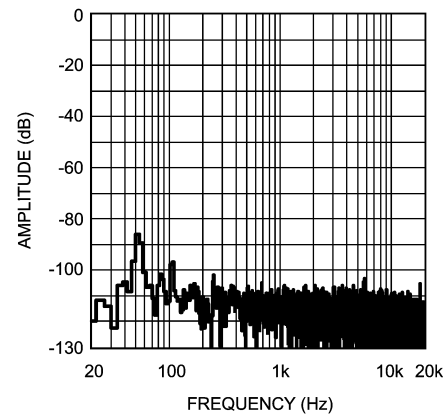
Noise Floor



200486F0

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, $V_{ol} = 3dB$, 44.1kHz Sample Rate

Noise Floor

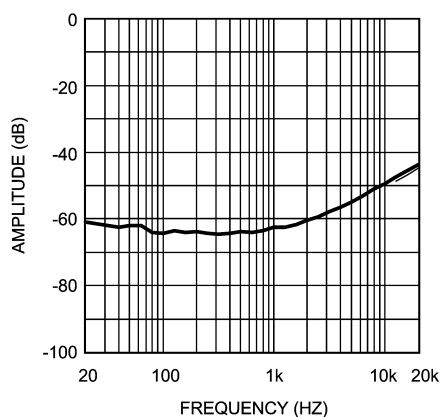


200486E9

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, $V_{ol} = 0dB$, 44.1kHz Sample Rate

Typical Performance Characteristics (Continued)

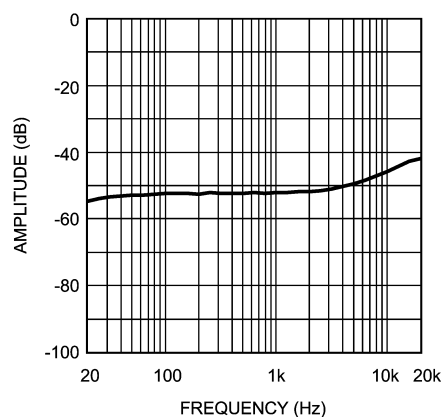
PSRR vs Frequency



200486G3

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Vol = 3dB, 44.1kHz Sample Rate

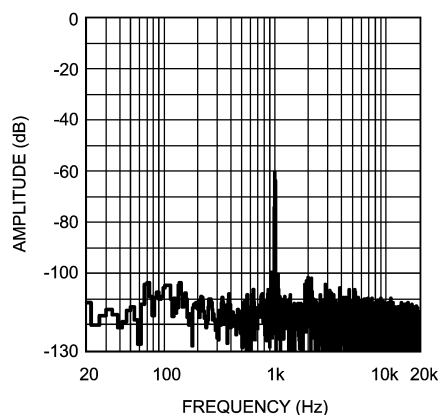
PSRR vs Frequency



200486E7

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Vol = 0dB, 44.1kHz Sample Rate

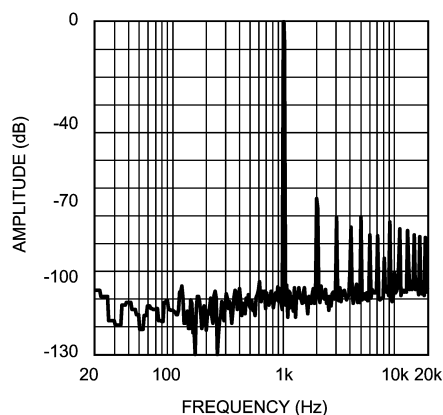
FFT @ 1kHz -60dB



200486D1

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Vol = 3dB, 44.1kHz Sample Rate

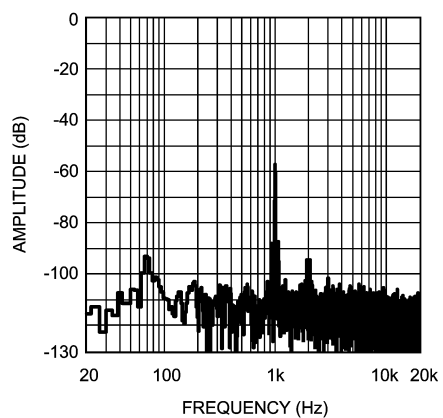
FFT @ 1kHz 0dB



200486C9

Analog $V_{DD} = 5V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Vol = 3dB, 44.1kHz Sample Rate

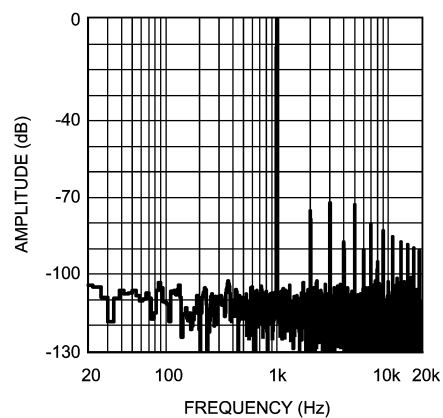
FFT @ 1kHz -60dB



200486D0

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Vol = 0dB, 44.1kHz Sample Rate

FFT @ 1kHz 0dB



200486F7

Analog $V_{DD} = 3V$, Digital $V_{DD} = 3V$
 $R_L = 32\Omega$, Vol = 0dB, 44.1kHz Sample Rate

Application Information

SPI OPERATIONAL DESCRIPTION

The serial data bits are organized into a field which contains 16 bits of data defined by TABLE 1. Bits 1 & 2 determine the output mode of the LM4921 as shown in TABLE 2. Bits 7 through 11 determine the volume level setting as illustrated by TABLE 3. Bit 12 sets the Bypass capacitor charging time.

Table 1. Bit Allocation

BIT #	Default Val	Function	Description
0 (LSB)	0	RESET_B	RESET_B = 0, Resets the DAC Must be high for the part to run.
1	0	MODE CONTROL	See Table 2
2	0		
3	0	MASTER/SLAVE	0 = SLAVE, 1 = MASTER
4	0	RESOLUTION	0 = 16 bit, 1 = 32 bit
5	0	RESERVED	Should always be set to '1'
6	0	ZERO CROSSING SET	0 = ZXD ENABLE, 1 = ZXD DISABLE
7	0	VOLUME CONTROL	See Table 3 - Volume Control Settings
8	0		
9	0		
10	0		
11	0		
12	0	BYP CHARGE RATE	0 = 1X, 1 = 2X
13	0	RESERVED	
14	0	RESERVED	
15 (MSB)	0	RESERVED	Should always be set to '0'

MODE CONTROL

Sets the modes as outlined in Table 2.

Table 2. Output Mode Selection (Bits 1 & 2 above)

Output Mode #	BIT 2	BIT 1	MODE
0	0	0	SD
1	0	1	STANDBY
2	1	0	MUTE
3	1	1	ACTIVE

Shutdown turns off the part completely for maximum power savings. The Standby mode turns off the clock but still consumes more power than the shutdown mode. However, coming out of standby mode allows the part to turn back on faster than from shutdown. In Mute mode the clocks remain on which uses more power but allows faster recovery and the ability to supply clock signals to other devices which is important when the part is used in master mode. Active mode turns the part on for normal operation.

MASTER/SLAVE SELECT

Allows the part to act as a master and supply the clock for the rest of the system or be a slave to the system clock.

RESOLUTION SET

Sets the resolution to be either 16 or 32 bits of stereo audio information. For most applications this will be set at 16 bits.

ZERO CROSSING DETECT SET

This pin turns on the zero crossing detection circuit. With this circuit enabled the part will not allow a volume step change, or shutdown mode, or standby mode to occur until the audio input signal passes through zero. This pin should be set to on for most applications.

Application Information (Continued)

VOLUME CONTROL

The internal Stereo Volume Control is set by changing bits 7 through 11 in the SPI interface, as shown in table 3 below. The zero dB setting is for 3V VDD operation and the +3dB is for 5V VDD.

Table 3. Volume Control Settings

Gain (dB) HP_L & HP_R	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7
-43.5	0	0	0	0	0
-42.0	0	0	0	0	1
-40.5	0	0	0	1	0
-39.0	0	0	0	1	1
-37.5	0	0	1	0	0
-36.0	0	0	1	0	1
-34.5	0	0	1	1	0
-33.0	0	0	1	1	1
-31.5	0	1	0	0	0
-30.0	0	1	0	0	1
-28.5	0	1	0	1	0
-27.0	0	1	0	1	1
-25.5	0	1	1	0	0
-24.0	0	1	1	0	1
-22.5	0	1	1	1	0
-21.0	0	1	1	1	1
-19.5	1	0	0	0	0
-18.0	1	0	0	0	1
-16.5	1	0	0	1	0
-15.0	1	0	0	1	1
-13.5	1	0	1	0	0
-12.0	1	0	1	0	1
-10.5	1	0	1	1	0
-9.0	1	0	1	1	1
-7.5	1	1	0	0	0
-6.0	1	1	0	0	1
-4.5	1	1	0	1	0
-3.0	1	1	0	1	1
-1.5	1	1	1	0	0
0.0	1	1	1	0	1
1.5	1	1	1	1	0
3.0	1	1	1	1	1

BYPASS CHARGE RATE BIT 12

This control pin allows the user to change the Bypass Capacitor's charge rate by a factor of two. Setting this bit at zero will set the circuit to its normal 1x rate. Setting the bit to High will double the charge rate and allow the part to turn on faster with a slight degradation in turn on click/pop noise.

SPI CONTROL INTERFACE BUS (J1)

SPI DATA: This is the serial data pin.

SPI CLK: This is the clock input pin.

SPI ENABLE: This is the SPI enable pin.

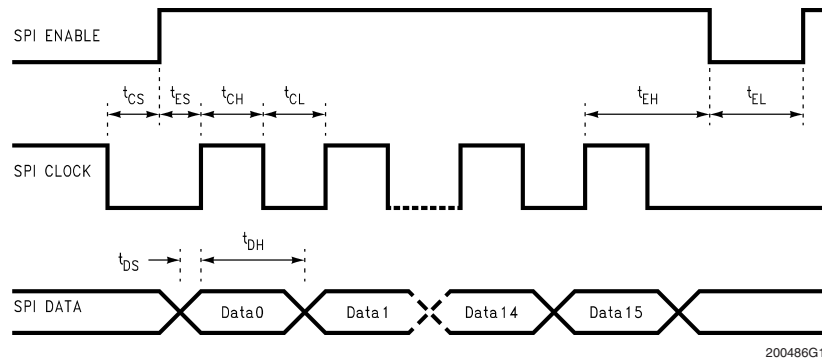
BITS 5, 13,14, and 15

Bits 13, 14, and 15 are all reserve bits and must be set to low/zero/ground.

Bit 5 must be set High.

Application Information (Continued)

SPI TIMING DIAGRAM



200486G1

SPI OPERATIONAL REQUIREMENTS

1. The maximum clock rate is 5MHz for the CLK pin.
2. CLK must remain logic-high for at least 100ns (t_{CH}) after the rising edge of CLK, and CLK must remain logic-low for at least 100ns (t_{CL}) after the falling edge of CLK.
3. Data bits are written to the DATA pin with the least significant bit (LSB) first.
4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 20ns (t_{DS}) before the rising edge of CLK. Also, any transition on DATA must occur at least 20ns (t_{DH}) after the rising edge of CLK and stabilize before the next rising edge of CLK.
5. ENABLE should be logic-high only during serial data transmission.
6. ENABLE must be logic-high at least 20ns (t_{ES}) before the first rising edge of CLK, and ENABLE has to remain logic-high at least 20ns (t_{EH}) after the sixteenth rising edge of CLK.
7. If ENABLE remains logic-low for more than 10ns before all 16 bits are transmitted then the data latch will be aborted.
8. If ENABLE is logic-high for more than 16 CLK pulses then only the first 16 data bits will be latched and activated at rising edge of sixteenth CLK.
9. ENABLE must remain logic-low for at least 30ns (t_{EL}).
10. Coincidental rising or falling edges of CLK and ENABLE are not allowed. If CLK is to be held logic-high after the data transmission, the falling edge of CLK must occur at least 20ns (t_{CS}) before ENABLE transitions to logic-high for the next set of data.

I2S INTERFACE BUS (J2 - Fig 2)

The I2S standard provides a uni-directional serial interface designed specifically for digital audio. For the LM4921, the interface provides access to a 48kHz, 16 bit full-range stereo

audio DAC. This interface uses a three wire system of clock (I2S_CLK), data (I2S_DATA), and word select (I2S_WS, sometimes called Right/Left Select).

A bit clock (I2S_CLK) at 32 or 64 times the sample frequency is established by the I2S system master and the word select (I2S_WS) line is driven at a frequency equal to the sampling rate of the audio data, in this case 48kHz. The word line is registered to change on the positive edge of the bit clock. The serial data (I2S_DATA) is sent MSB first, again registers on the positive edge of the bit clock, delayed by 1 bit clock cycle relative to the changing of the word line (typical I²S format).

MCLK/XTAL_IN (S1 MCLK SEL - Fig 2)

This is the input for an external Master Clock. The jumper at S1 must be removed (disconnecting the onboard crystal from the circuit) when using an external Master Clock.

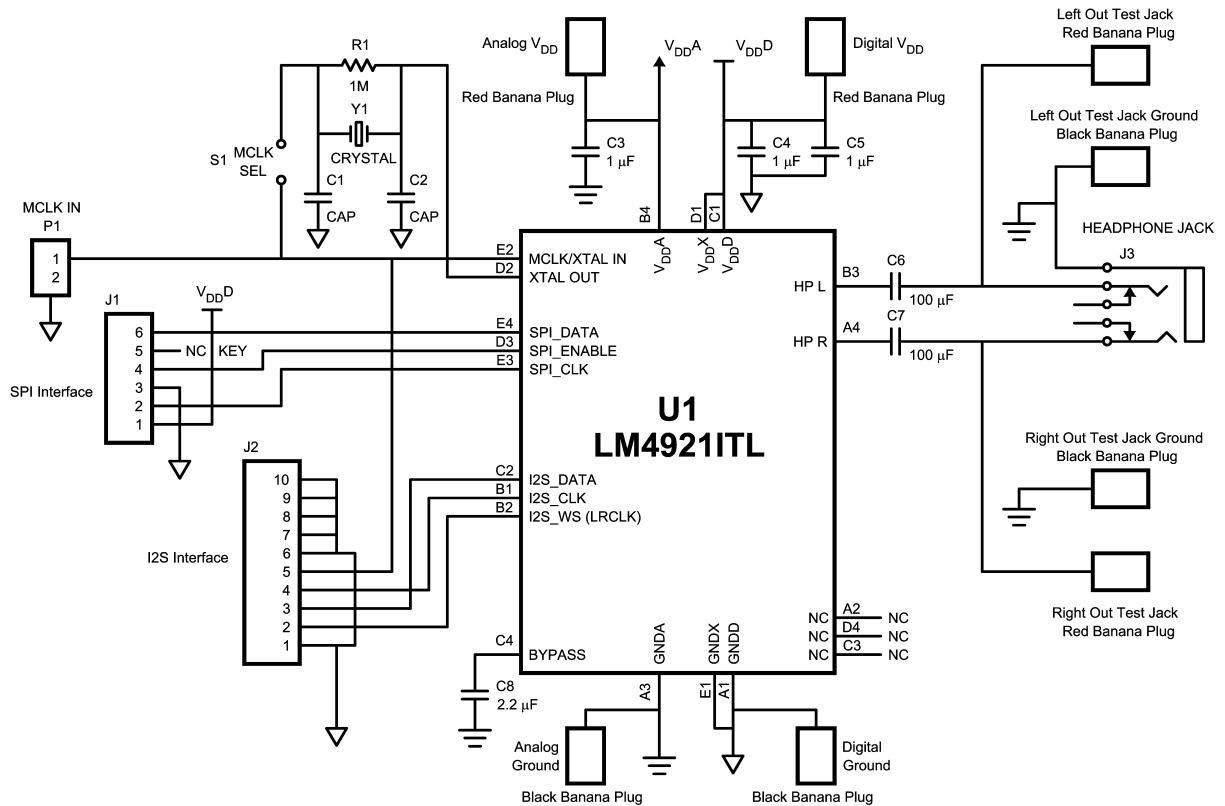
STEREO HEADPHONE OUTPUT JACK (J3 - Fig 2)

This is the stereo headphone output. Each channel is single-ended, with 100uF DC output blocking capacitors mounted on the demo board (C6 and C7). These capacitors are necessary to block the 1/2 VDD DC bias and prevent it from flowing through the headphone speakers (DC current will destroy most audio speakers) while allowing the audio ac signal to pass through. The jack features a typical stereo headphone pinout.

Application Information (Continued)

LM4921ITL DEMO BOARD OPERATION

The LM4921ITL demo board is a complete evaluation platform (Note 10), designed to give easy access to the control pins of the part and comprise all the necessary external passive components. There are separate analog and digital supply connectors, SPI interface bus (J1) for the control lines, I²S interface bus (J2) for full-range digital audio, stereo headphone output (J3), and an external MCLK input (P1) for use in place of the crystal on the demoboard.



200486G2

FIGURE 2. LM4921ITL Demo Board Schematic

Note 10: Parallel Port SPI Interface Card and control software available.

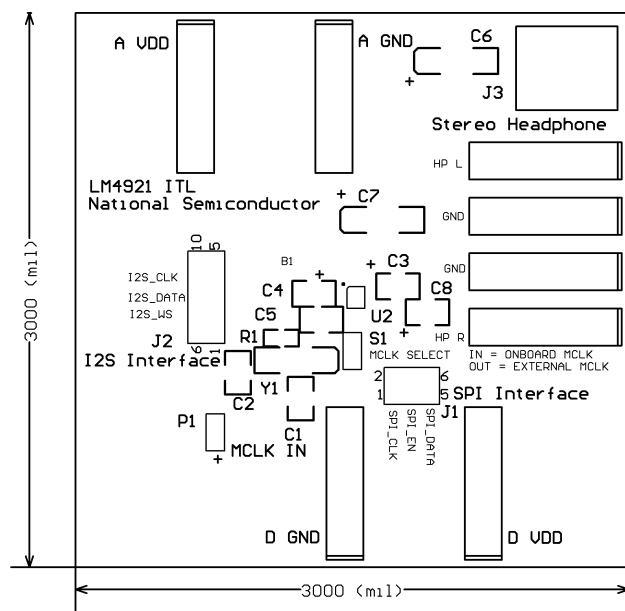
Application Information (Continued)

DEMO BOARD BILL OF MATERIALS

National Semiconductor Corporation Bill of Material				
Analog Audio LM4921ITL20 Eval Board				
Assembly Part Number: 980011973-100				
Revision A				
Item	Part Number	Part Description	Qty	Ref Designator
1	551011973-001	LM4921 Eval Board PCB etch 001	1	
2		LM4921 ITL20 micro SMD 20 Bumps	1	U1
3		Cer Cap 22pF 50V 10%, size 1206	2	C1, C2
4		Cer Cap 0.1pF 50V 10%, size 1206	1	C4
5		Tant Cap 1μF 16V 10%, 3216	3	C3, C5, C8
6		Tant Cap 220μF 16V 10%, 7243	2	C6, C7
7		1 meg ohm	1	R1
8		Crystal 11.2896MHz	1	Y1
9		Phone Jack 3.5mm Stereo	1	J3
10		Jumper Header 1X2	2	P1, S1
11		Jumper Header 1X3	2	J1
12		Jumper Header 1X5	2	J2
13		PCB Banana Jack, Black-Mouser 164-6218	4	A GND, D GND, GND (2)
14		PCB Banana Jack, Red-Mouser 164-6219	4	A VDD, D VDD, HP L, HP R

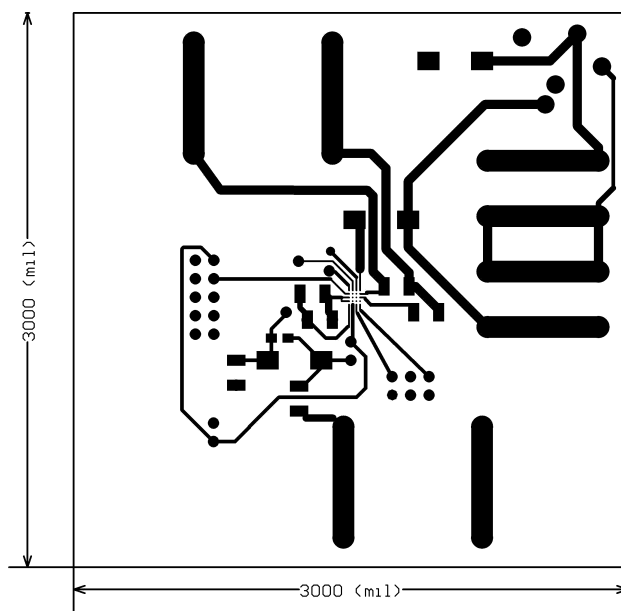
Application Information (Continued)

DEMO BOARD ARTWORKS



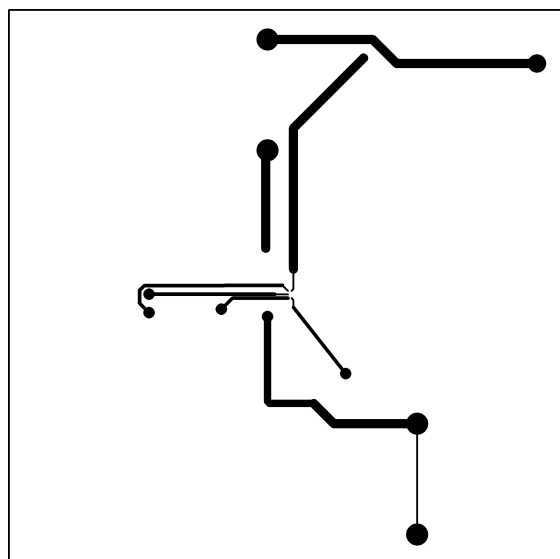
Silkscreen Layer

200486F3



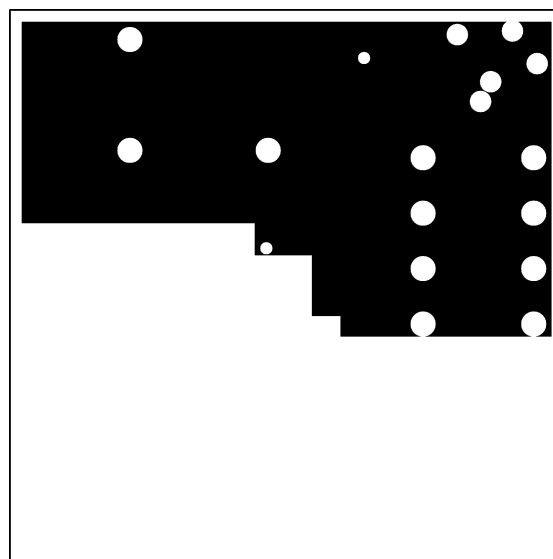
Top Layer

200486F1



Mid Layer 1

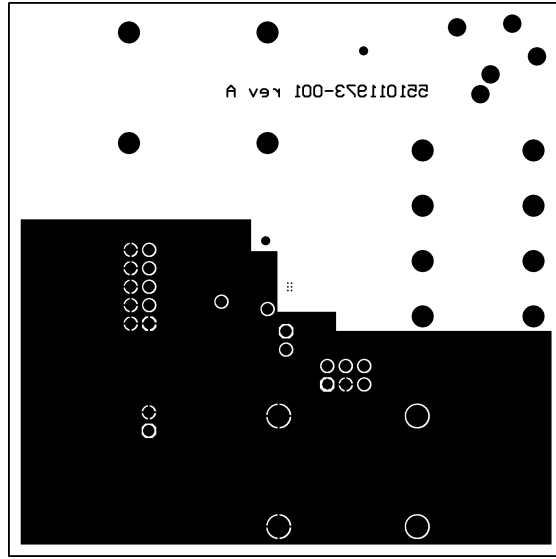
200486F2



Mid Layer 2

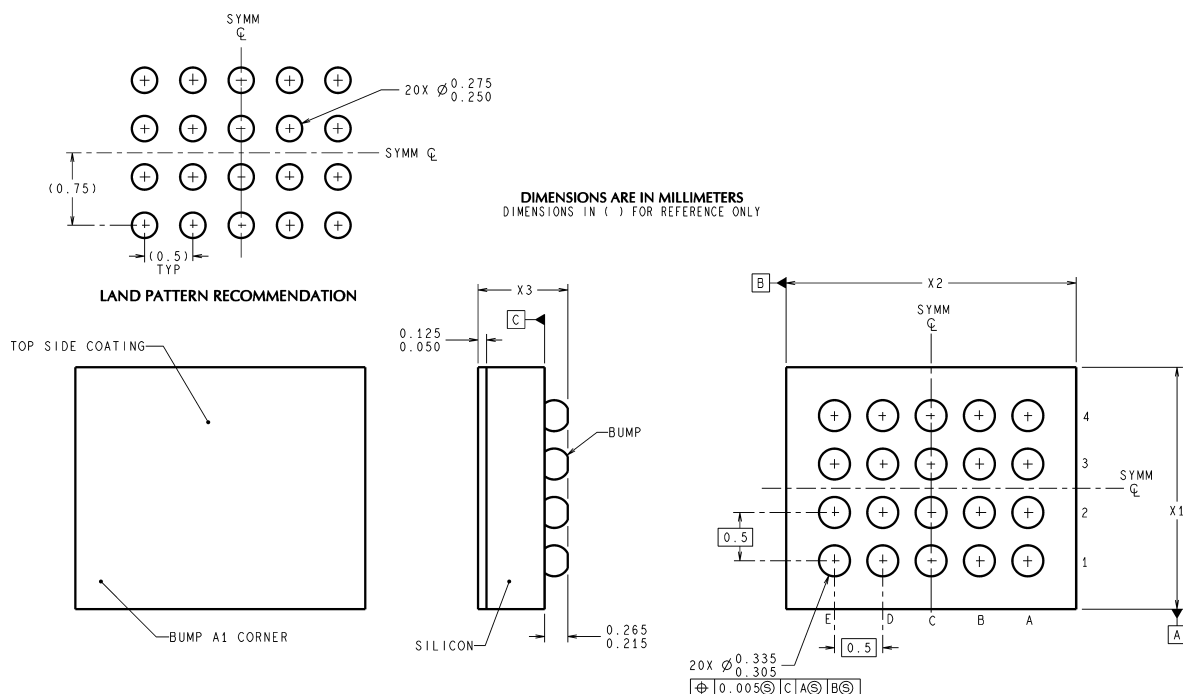
200486H1

Application Information (Continued)



Bottom Layer

Physical Dimensions inches (millimeters) unless otherwise noted



20 Bump micro SMD
Order Number LM4921ITL, LM4921ITLX
NS Package Number TLA20JKA
X1 = 2.200 ± 0.03mm X2 = 2.720 ± 0.03mm X3 = 0.600 ± 0.075mm

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