National Semiconductor

October 2006

LM4947 Boomer® Audio Power Amplifier Series
Mono Class D and Stereo Audio Subsystem with OCL Headphone Amplifier and National 3D

General Description

The LM4947 is an audio subsystem capable of efficiently delivering 500mW (Class D operation) of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N, 37mW (Class AB operation) power channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, or an output capacitor-less (OCL) configuration with identical specification as the SE configuration, from a 3.3V power supply.

The LM4947 has six input channels: one pair for a two-channel stereo signal, the second pair for a secondary two-channel stereo input, and the third pair for a differential single-channel mono input. Additionally, the two sets of stereo inputs may be configured as a single stereo differential input (differential left and differential right). The LM4947 features a 32-step digital volume control and eight distinct output modes. The digital volume control, 3D enhancement, and output modes are programmed through a two-wire I^2C compatible interface that allows flexibility in routing and mixing audio channels.

The RF suppression circuitry in the LM4947 makes it well-suited for GSM mobile phones and other portable applications in which strong RF signals generated by an antenna (and long output traces) may couple audibly into the amplifier.

The LM4947 is designed for cellular phones, PDAs, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only eight external components in the OCL mode (two additional components in SE mode).

Key Specifications

- THD+N at 1kHz, 500mW into 8Ω BTL (3.3V) — 1.0% (typ)
- THD+N at 1kHz, 37mW into 32Ω SE (3.3V) — 1.0% (typ)
- Single Supply Operation (V_{DD}) — 2.7 to 5.5V
- I^2C Single Supply Operation — 2.2 to 5.5V

Features

- I^2C Control Interface
- I^2C programmable National 3D Audio
- I^2C controlled 32 step digital volume control (-59.5dB to +18dB)
- Three independent volume channels (Left, Right, Mono)
- Eight distinct output modes
- Small, 25–bump micro SMD packaging
- “Click and Pop” suppression circuitry
- Thermal shutdown protection
- Low shutdown current (0.1μA, typ)
- RF suppression
- Differential mono and stereo inputs
- Stereo input mux

Applications

- Mobile Phones
- PDAs

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Typical Application

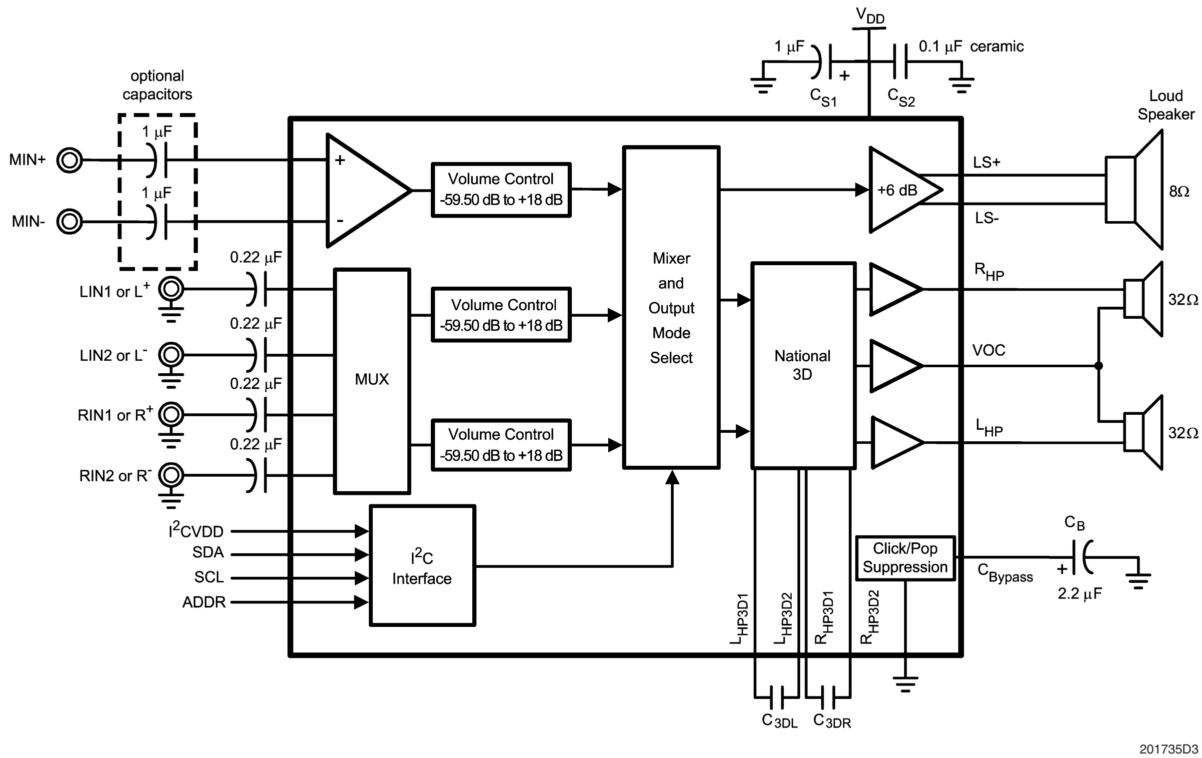


FIGURE 1. Typical Audio Amplifier Application Circuit-Output Capacitor-less

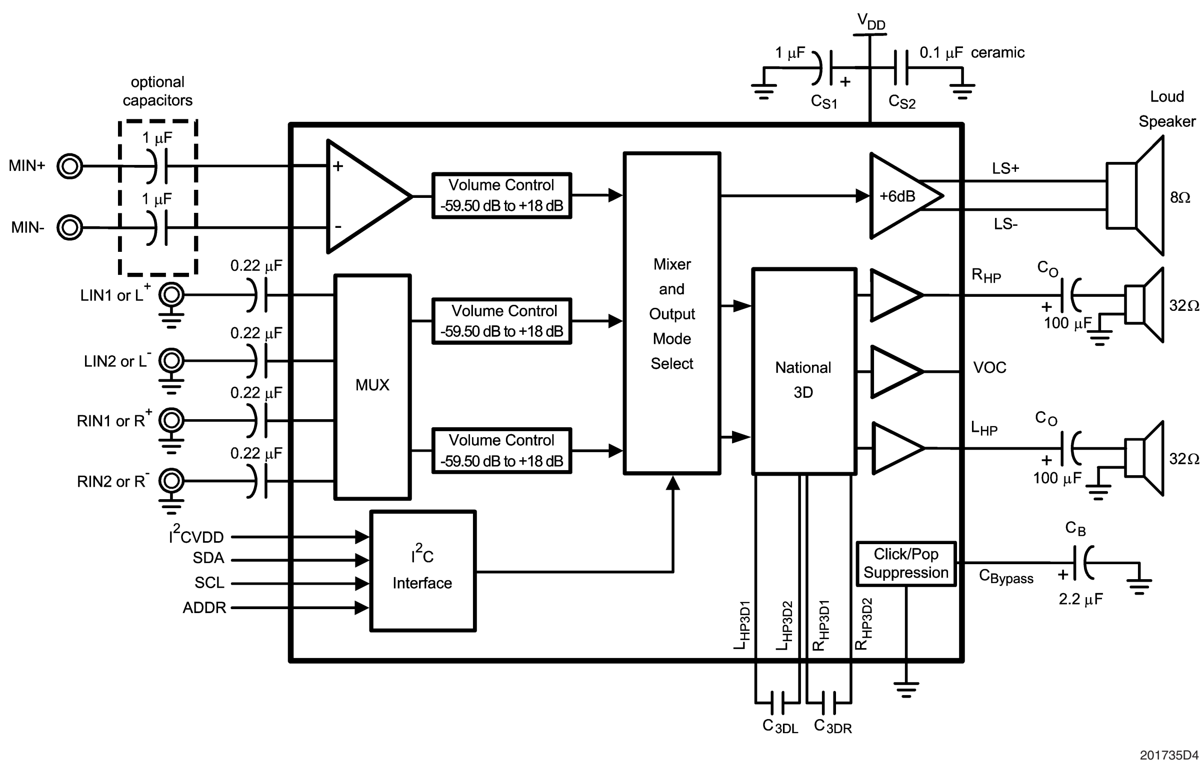
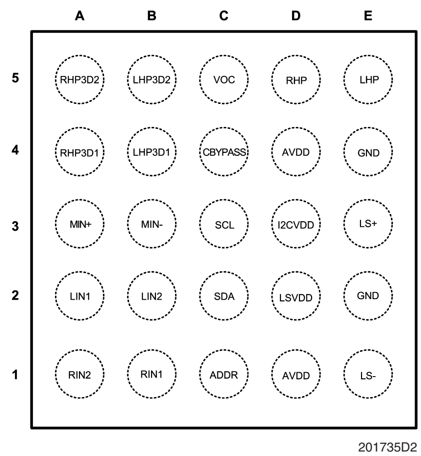


FIGURE 2. Typical Audio Amplifier Application Circuit-Single Ended

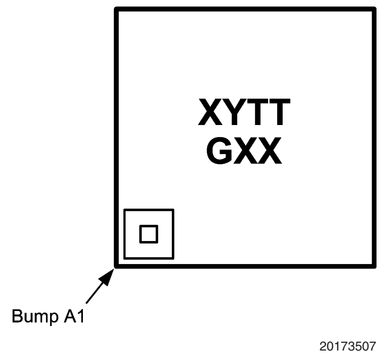
Connection Diagrams

25-Bump micro SMD



Top View

micro SMD Marking



Top View
XY - Date Code
TT - Die Traceability
G - Boomer Family
XX - H1

Pin Descriptions

Bump	Name	Description
A1	R_{IN2}	Right Input Channel 2 or Right Differential Input -
A2	L_{IN1}	Left Input Channel 1 or Left Differential Input +
A3	MIN+	Mono Channel Non-inverting Input
A4	RHP_{3D1}	Right Headphone 3D Input 1
A5	RHP_{3D2}	Right Headphone 3D Input 2
B1	R_{IN1}	Right Input Channel 1 or Right Differential Input +
B2	L_{IN2}	Left Input Channel 2 or Left Differential Input -
B3	MIN-	Mono Channel Inverting Input
B4	L_{HP3D1}	Left Headphone 3D Input 2
B5	L_{HP3D2}	Left Headphone 3D Input 1
C1	ADDR	Address Identification
C2	SDA	Serial Data Input
C3	SCL	Serial Clock Input
C4	C_{BYPASS}	Half-Supply Bypass Capacitor
C5	VOC	Headphone return bias output
D1	AV_{DD}	Analog Power Supply
D2	LSV_{DD}	Loudspeaker Power Supply
D3	$I2CV_{DD}$	I2C Interface Power Supply
D4	AV_{DD}	Analog Power Supply
D5	R_{HP}	Right Headphone Output
E1	LS-	Loudspeaker Output Negative
E2	GND	Ground
E3	LS+	Loudspeaker Output Positive
E4	GND	Ground
E5	L_{HP}	Left Headphone Output

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	–65˚C to +150˚C
Input Voltage	–0.3 to V_{DD} +0.3
ESD Susceptibility (Note 3)	2.0kV
ESD Machine model (Note 6)	200V
Junction Temperature (T_J)	150˚C
Solder Information	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
Thermal Resistance	
θ_{JA} (typ) - TLA25CBA	65˚C/W

Operating Ratings

Temperature Range	–40˚C to 85˚C
Supply Voltage (V_{DD})	2.7V ≤ V_{DD} ≤ 5.5V
Supply Voltage (I^2C)	2.2V ≤ V_{DD} ≤ 5.5V
Supply Voltage (Loudspeaker V_{DD})	2.7V ≤ V_{DD} ≤ 5.5V

Electrical Characteristics 3.3V (Notes 2, 7)

The following specifications apply for V_{DD} = 3.3V, T_A = 25˚C, and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical (Note 4)	Limits (Note 5)	
I_{DDQ}	Quiescent Supply Current	Output Modes 2, 4, 6 V_{IN} = 0V; No load, OCL = 0 (Table 2)	4.5	6.5	mA (max)
		Output Modes 1, 3, 5, 7 V_{IN} = 0V; No load, BTL, OCL = 0 (Table 2)	6.5	8	mA (max)
I_{SD}	Shutdown Current	Output Mode 0	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 7, Mono	2	15	mV (max)
		V_{IN} = 0V, Mode 7, Headphones	2	15	
P_O	Output Power	MONO $_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	500	400	mW (min)
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, SE, Mode 4	37	33	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	$MONO_{OUT}$ f = 1kHz, P_{OUT} = 250mW; R_L = 8Ω, BTL, Mode 1	0.03		%
		R_{OUT} and L_{OUT} f = 1kHz, P_{OUT} = 12mW; R_L = 32Ω, SE, Mode 4	0.02		%
N_{OUT}	Output Noise	A-weighted, 0dB inputs terminated, output referred			
		Speaker; Mode 1	39		µV
		Speaker; Mode 3	39		µV
		Speaker; Mode 5	42		µV
		Speaker; Mode 7	38		µV
		Headphone; SE, Mode 2	15		µV
		Headphone; SE, Mode 4	15		µV
		Headphone; SE, Mode 6	17		µV
		Headphone; OCL, Mode 2	12		µV
		Headphone; OCL, Mode 4	15		µV
		Headphone; OCL, Mode 6	17		µV

Electrical Characteristics 3.3V (Notes 2, 7) (Continued)

The following specifications apply for V_{DD} = 3.3V, T_A = 25˚C, and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical (Note 4)	Limits (Note 5)	
PSRR	Power Supply Rejection Ratio Loudspeaker out	V_{RIPPLE} = 200mV$_{PP}$; f = 217Hz, R_L = 8Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		BTL, Output Mode 1	79		dB
		BTL, Output Mode 3	78		dB
		BTL, Output Mode 5	79		dB
		BTL, Output Mode 7	80		dB
	Power Supply Rejection Ratio R_{OUT} and L_{OUT}	V_{RIPPLE} = 200mV$_{PP}$; f = 217Hz, R_L = 32Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		SE, Output Mode 2	78		dB
		SE, Output Mode 4	71		dB
		SE, Output Mode 6	71		dB
		OCL, Output Mode 2	83		dB
		OCL, Output Mode 4	74		dB
		OCL, Output Mode 6	74		dB
η	Class D Efficiency	Output Mode 1, 3, 5	86		%
CMRR	Common-Mode-Rejection Ratio	f = 217Hz, V_{CM} = 1Vpp, Mode 1, BTL, R_L = 8Ω	–49		dB
XTALK	Crosstalk	Headphone, P_O = 12mW, f = 1kHz, OCL, Mode 4, R_L = 32Ω	–58		dB
		Headphone, P_O = 12mW, f = 1kHz, SE, Mode 4, R_L = 32Ω	–73		
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, OCL, R_L = 32Ω	90		ms
		C_B = 2.2µF, SE, R_L = 32Ω	115		
	Volume Control Step Size Error		±0.2		dB
	Digital Volume Range	Input referred maximum attenuation	-59.5	–60.25 –58.75	dB (min) dB (max)
		Input referred maximum gain	+18	17.25 18.75	dB (min) dB (max)
	Mute Attenuation	Output Mode 1, 3, 5	87		dB
	MONO_IN Input Impedance R_{IN} and L_{IN} Input Impedance	Maximum gain setting	12	8 14	kΩ (min) kΩ (max)
		Maximum attenuation setting	100	75 125	kΩ (min) kΩ (max)

Electrical Characteristics 5V (Notes 2, 7)

The following specifications apply for V_{DD} = 5V, T_A = 25˚C and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical (Note 4)	Limits (Note 5)	
I_{DDQ}	Quiescent Supply Current	Output Modes 2, 4, 6 V_{IN} = 0V; No load, OCL = 0 (Table 2)	5.4	7.5	mA
		Output Modes 1, 3, 5, 7 V_{IN} = 0V; No load, BTL, OCL = 0 (Table 2)	7.6	12	mA
I_{SD}	Shutdown Current	Output Mode 0	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 7, Mono	2	15	mV (max)
		V_{IN} = 0V, Mode 7, Headphones	2	15	
P_O	Output Power	$MONO_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	1.19		W
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, SE, Mode 4	87		mW
THD+N	Total Harmonic Distortion + Noise	$MONO_{OUT}$ f = 1kHz, P_{OUT} = 500mW; R_L = 8Ω, BTL, Mode 1	0.04		%
		R_{OUT} and L_{OUT} f = 1kHz, P_{OUT} = 30mW; R_L = 32Ω, SE, Mode 4	0.01		%
N_{OUT}	Output Noise	A-weighted, 0dB inputs terminated, output referred			
		Speaker; Mode 1	38		µV
		Speaker; Mode 3	38		µV
		Speaker; Mode 5	39		µV
		Speaker; Mode 7	36		µV
		Headphone; SE, Mode 2	21		µV
		Headphone; SE, Mode 4	21		µV
		Headphone; SE, Mode 6	24		µV
		Headphone; OCL, Mode 2	16		µV
		Headphone; OCL, Mode 4	16		µV
		Headphone; OCL, Mode 6	19		µV

Electrical Characteristics 5V (Notes 2, 7) (Continued)

The following specifications apply for V_{DD} = 5V, T_A = 25˚C and all gains are set for 0dB unless otherwise specified.

Symbol	Parameter	Conditions	LM4947 Typical (Note 4)	LM4947 Limits (Note 5)	Units (Limits)
PSRR	Power Supply Rejection Ratio Loudspeaker out	V_{RIPPLE} = 200mV$_{PP}$; f = 217Hz, R_L = 8Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		BTL, Output Mode 1	70		dB
		BTL, Output Mode 3	61		dB
		BTL, Output Mode 5	64		dB
		BTL, Output Mode 7	61		dB
	Power Supply Rejection Ratio R_{OUT} and L_{OUT}	V_{RIPPLE} = 200mV$_{PP}$; f = 217Hz, R_L = 32Ω, C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		SE, Output Mode 2	72		dB
		SE, Output Mode 4	70		dB
		SE, Output Mode 6	65		dB
		OCL, Output Mode 2	76		dB
		OCL, Output Mode 4	72		dB
		OCL, Output Mode 6	70		dB
η	Class D Efficiency	Output Mode 1, 3, 5	86		%
CMRR	Common-Mode Rejection Ratio	f = 1kHz, V_{CM} = 1Vpp, 0dB gain, Mode 1, BTL, R_L = 8Ω	–49		dB
XTALK	Crosstalk	Headphone, P_O = 30mW, f = 1kHz, OCL, Mode 4	–55		dB
		Headphone, P_O = 30mW, f = 1kHz, SE, Mode 4	–72		
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, OCL, R_L = 32Ω	116		ms
		C_B = 2.2µF, SE, R_L = 32Ω	150		
	Volume Control Step Size Error		±0.2		dB
	Digital Volume Range	Input referred maximum attenuation	-59.5		dB
		Input referred maximum gain	+18		dB
	Mute Attenuation	Output Mode 1, 3, 5	90		dB
	MONO_IN Input Impedance R_{IN} and L_{IN} Input Impedance	Maximum gain setting	11		kΩ
		Maximum attenuation setting	100		kΩ

I^2C (Notes 2, 7)

The following specifications apply for V_{DD} = 5V and 3.3V, T_A = 25˚C unless otherwise specified.

Symbol	Parameter	Conditions	LM4947		Units (Limits)
			Typical (Note 4)	Limits (Note 5)	
t_1	Clock Period			2.5	µs (max)
t_2	Clock Setup Time			100	ns (min)
t_3	Data Hold Time			100	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	SPI Input Voltage High			0.7xI^2C V_{DD}	V (min)
V_{IL}	SPI Input Voltage Low			0.3xI^2C V_{DD}	V (max)

I^2C Protocol Information

The I^2C address for the LM4947 is determined using the ID_ENB pin. The LM4947's two possible I^2C chip addresses are of the form 111110$X_1$0 (binary), where X_1 = 0, if ID_ADDR is logic LOW; and X_1 = 1, if ID_ENB is logic HIGH. If the I^2C interface is used to address a number of chips in a system, the LM4947's chip address can be changed to avoid any possible address conflicts.

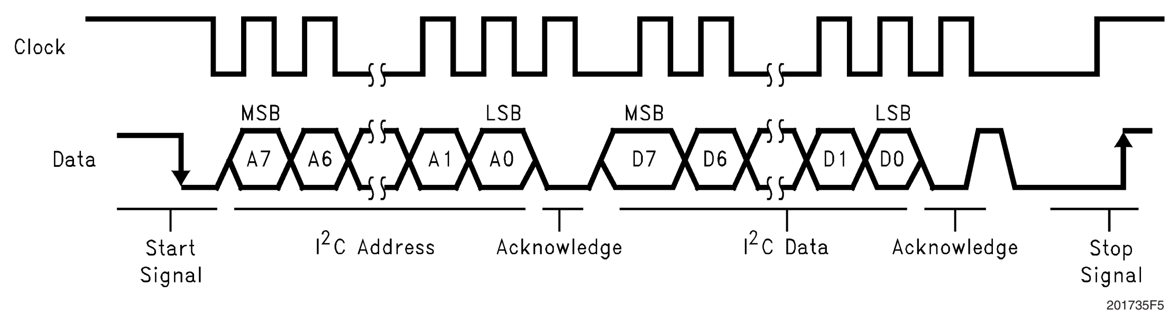


FIGURE 3. I^2C Bus Format

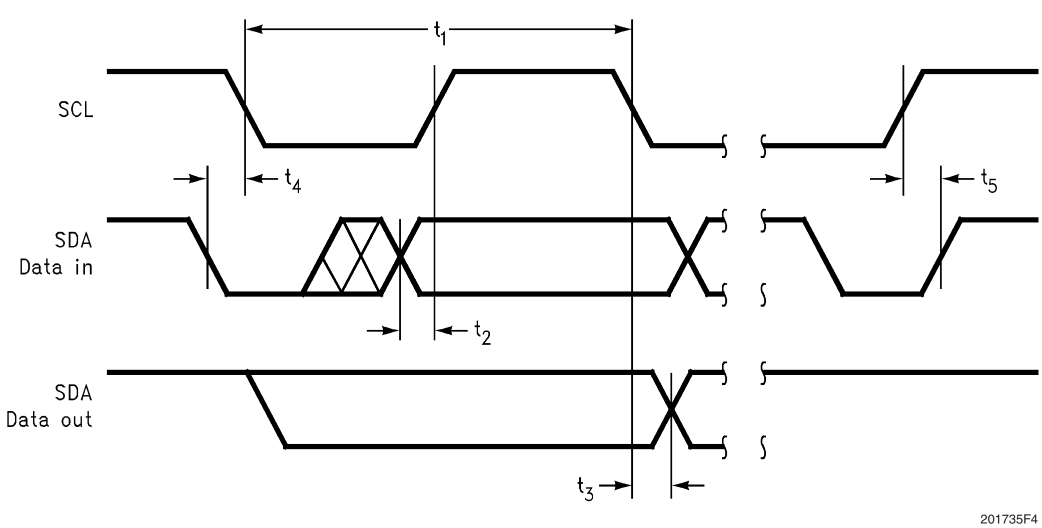


FIGURE 4. I^2C Timing Diagram

Note 1: See AN-450 "Surface Mounting and their effects on Product Reliability" for other methods of soldering surface mount devices.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 4: Typical specifications are specified at +25˚C and represent the most likely parametric norm.

Note 5: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

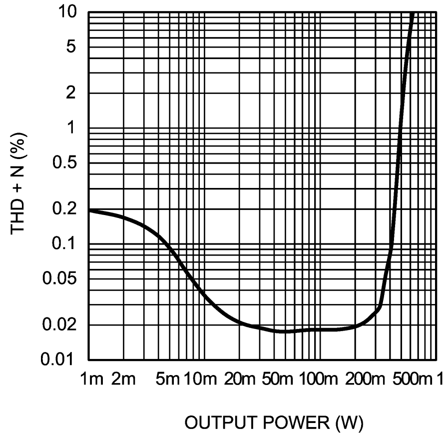
Note 7: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 8: The given θ_{JA} for an LM4947TL mounted on a demonstration board with a $9in^2$ area of 1oz printed circuit board copper ground plane.

Note 9: Datasheet min/max specifications are guaranteed by design, test, or statistical analysis.

Typical Performance Characteristics

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 1, MONO



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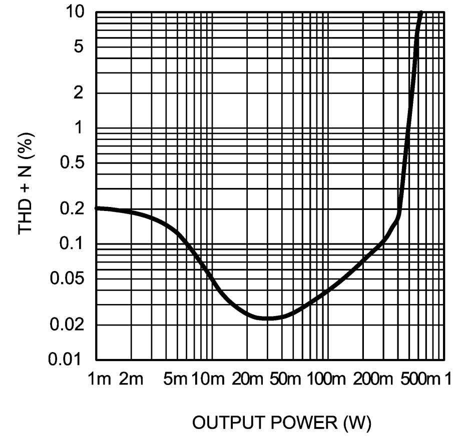
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 3, MONO



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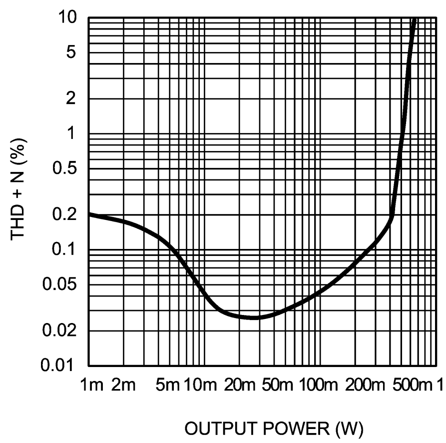
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 5, MONO



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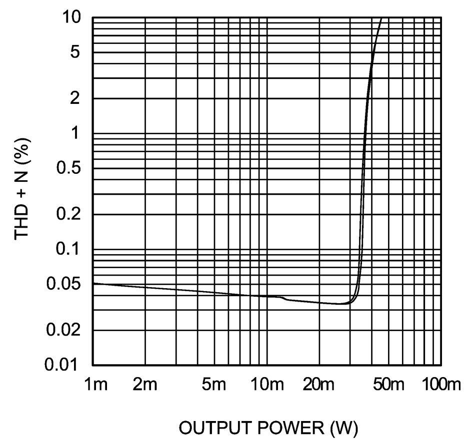
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, OCL



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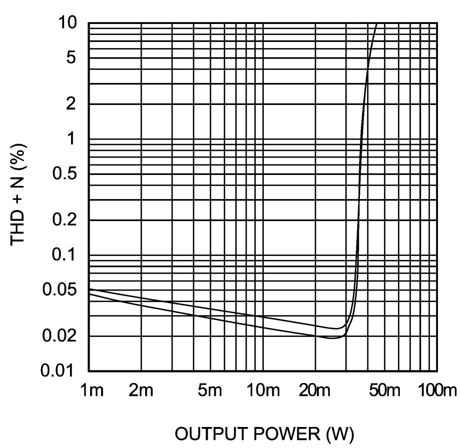
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, SE



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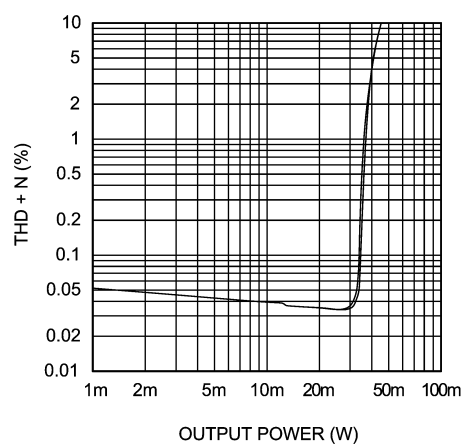
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, OCL



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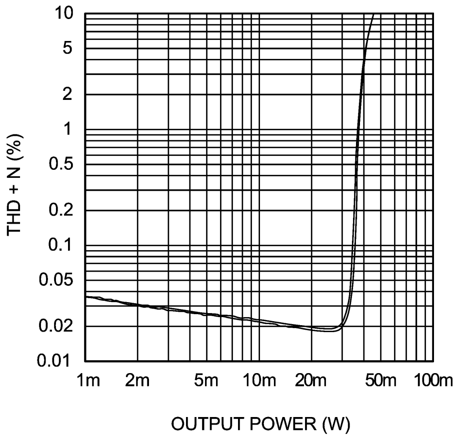
Typical Performance Characteristics (Continued)

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, SE



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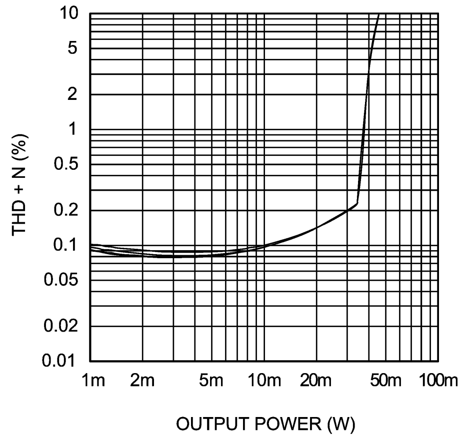
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, OCL



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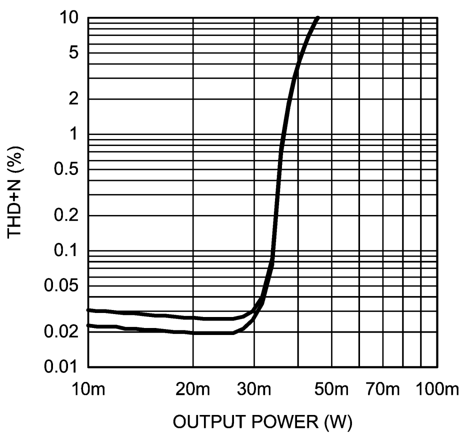
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, SE



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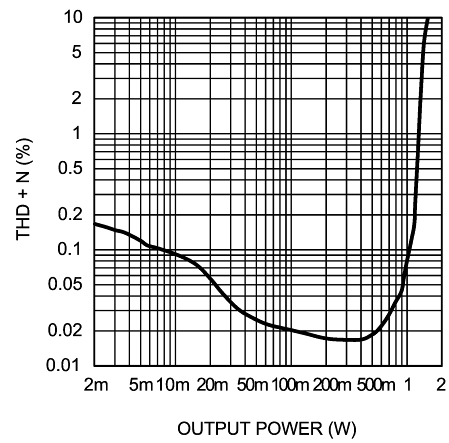
THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 1, MONO



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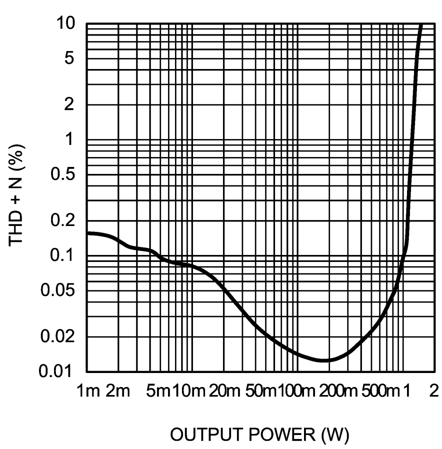
THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 3, MONO



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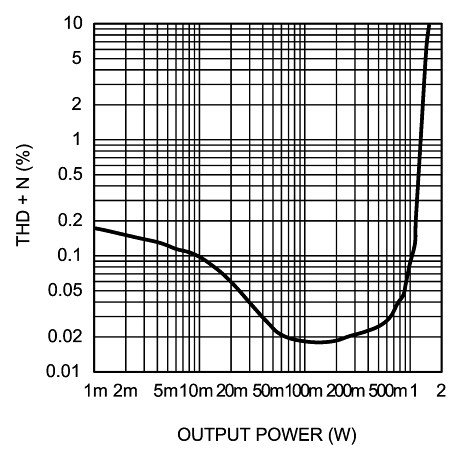
THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 5, MONO



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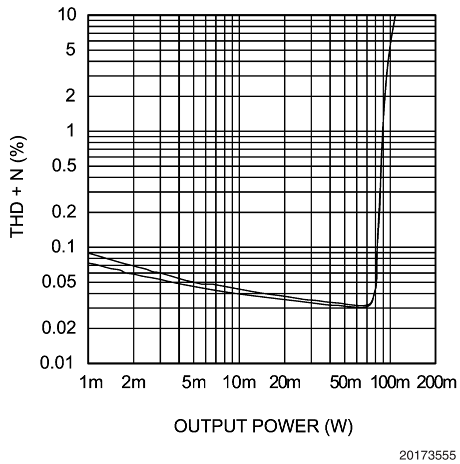
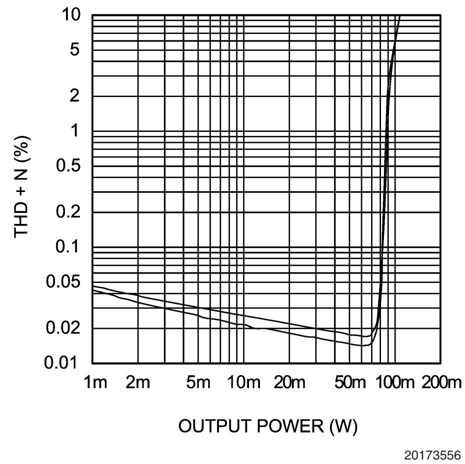
Typical Performance Characteristics (Continued)

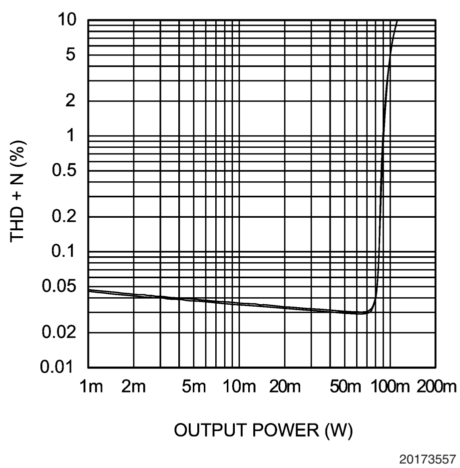
THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, OCL



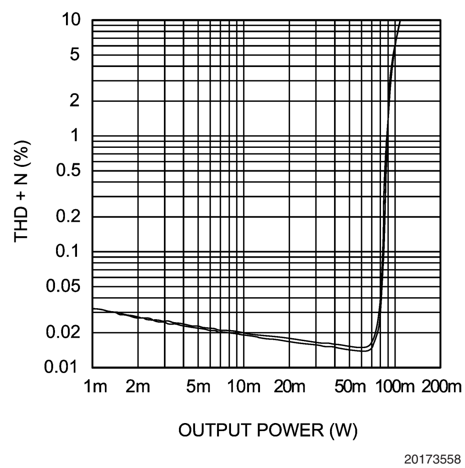
THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 2, SE



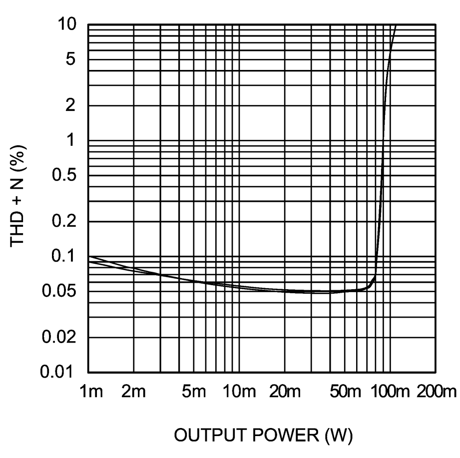
THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, OCL



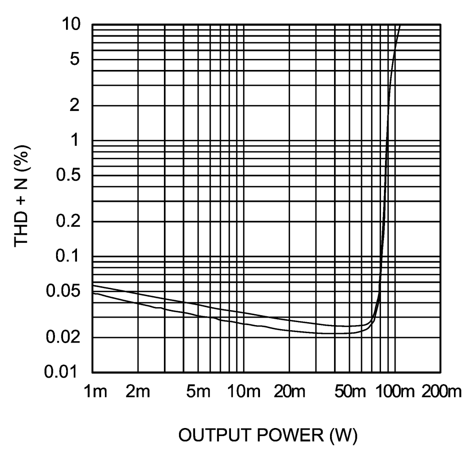
THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 4, SE



THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, OCL

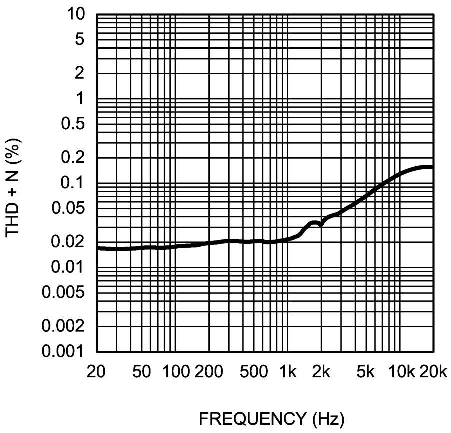


THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz, Diff In
Mode 6, SE



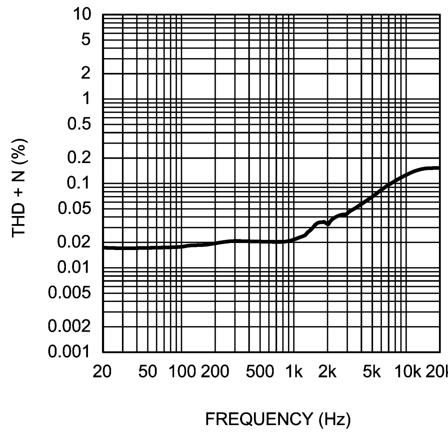
Typical Performance Characteristics (Continued)

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Diff In, Mode 1



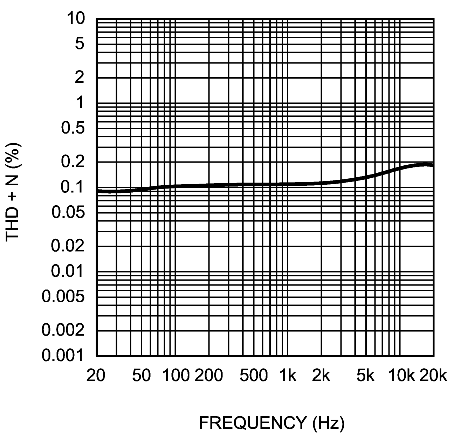
20173525

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Diff In, Mode 5



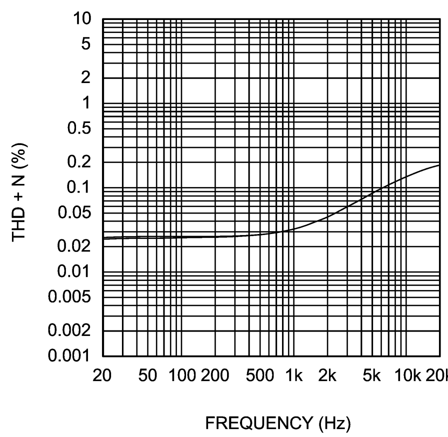
20173526

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Diff In, Mode 3



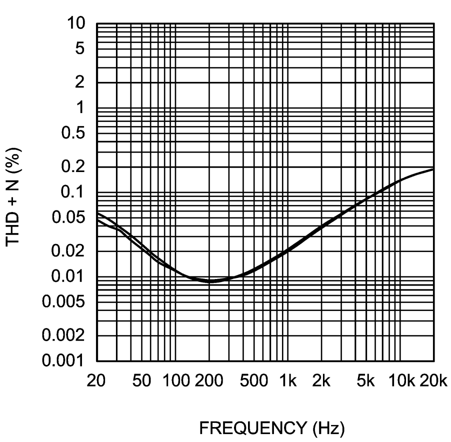
20173527

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 2, OCL



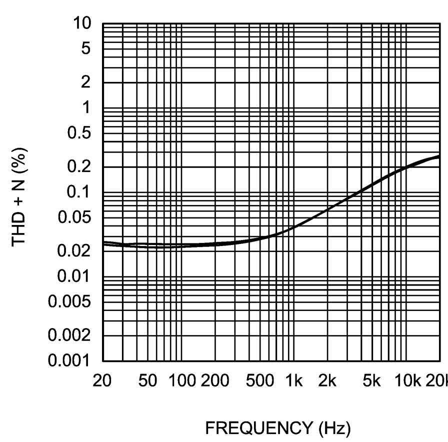
20173528

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 2, SE



20173529

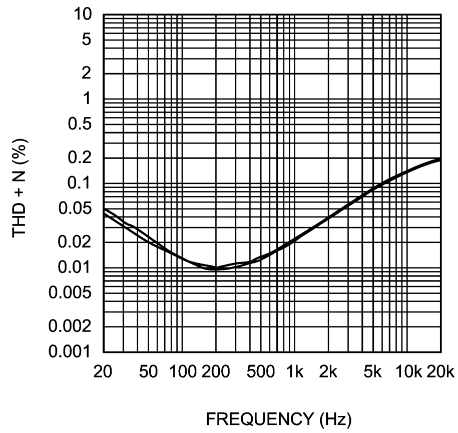
THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4,7, OCL



20173530

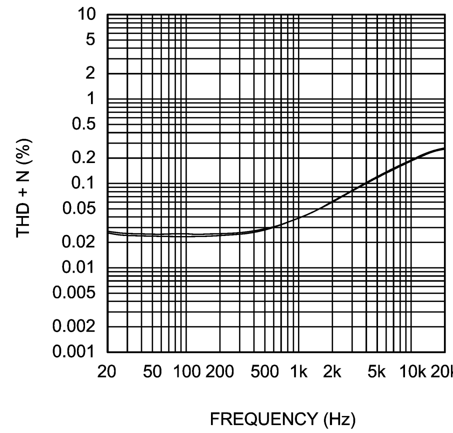
Typical Performance Characteristics (Continued)

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4,7, SE



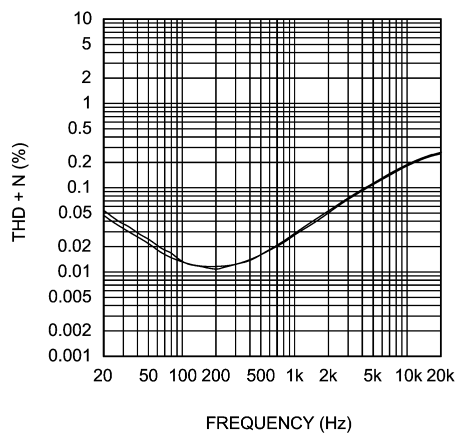
20173531

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 6, OCL



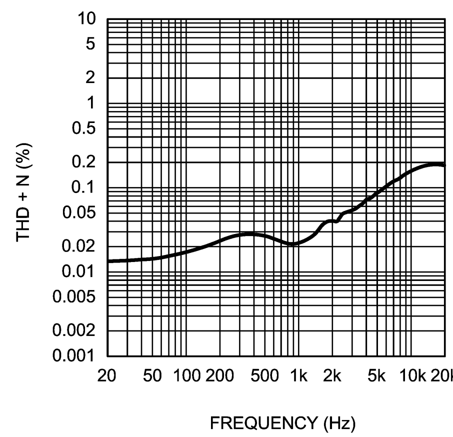
20173532

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 6, SE



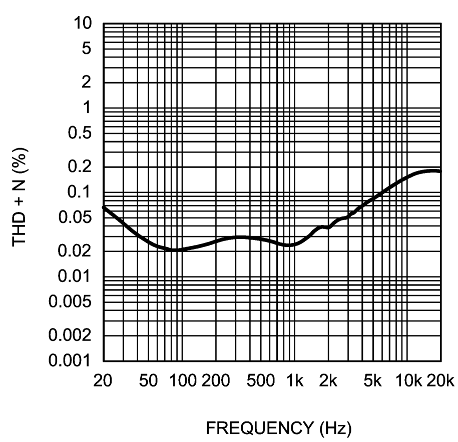
20173533

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Diff In, Mode 1



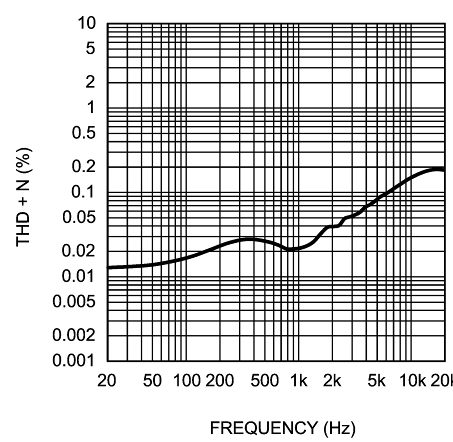
20173534

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Diff In, Mode 3



20173535

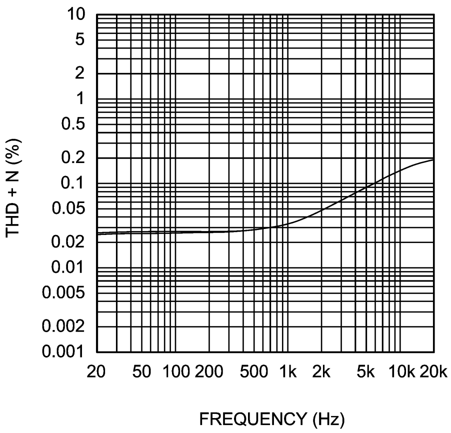
THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Diff In, Mode 5



20173536

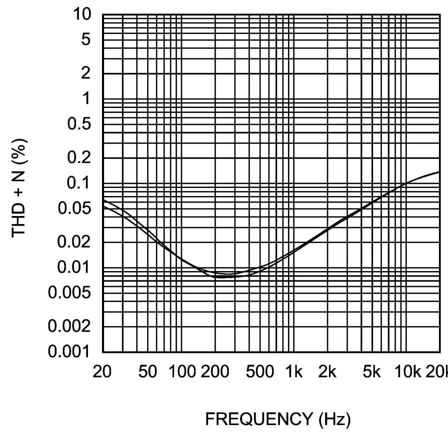
Typical Performance Characteristics (Continued)

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Diff In, Mode 2, OCL



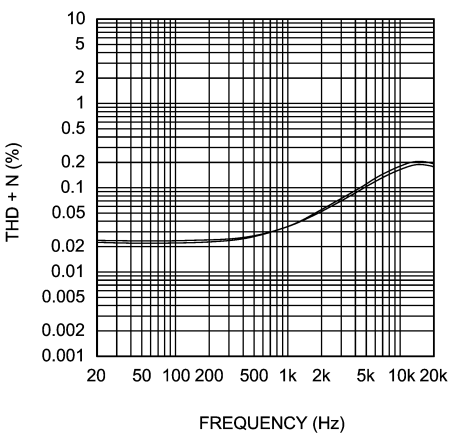
20173537

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Diff In, Mode 2, SE



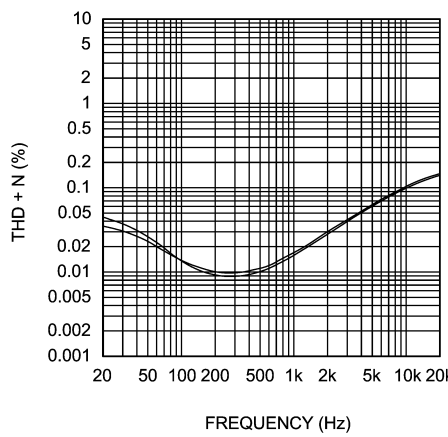
20173538

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Diff In, Mode 4,7, OCL



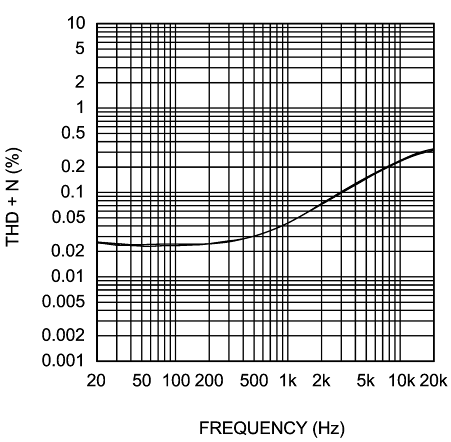
20173539

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Diff In, Mode 4,7, SE



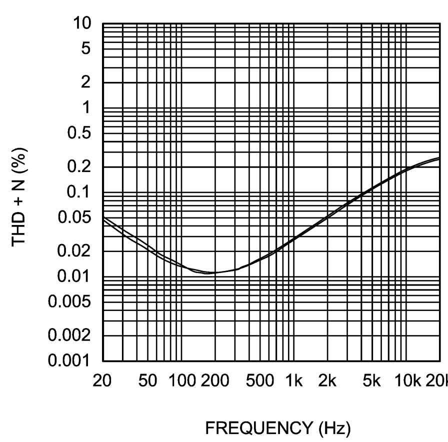
20173540

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Diff In, Mode 6, OCL



20173541

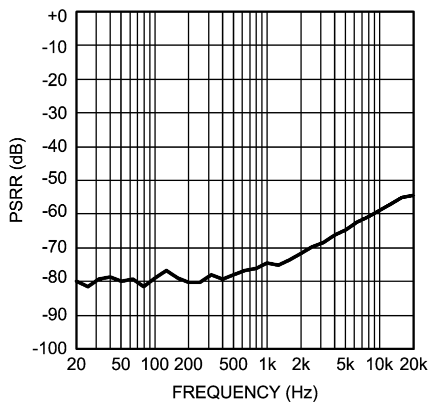
THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Diff In, Mode 6, SE



20173542

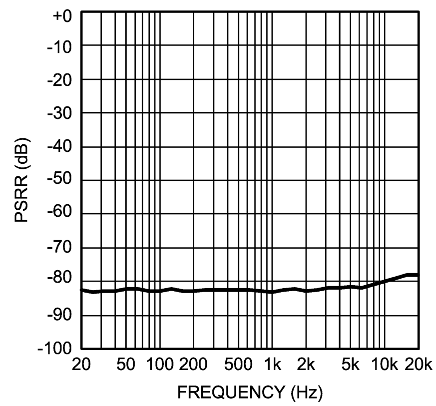
Typical Performance Characteristics (Continued)

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 1, MONO



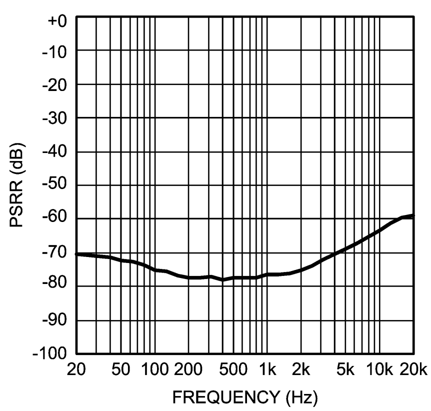
20173516

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 2, OCL



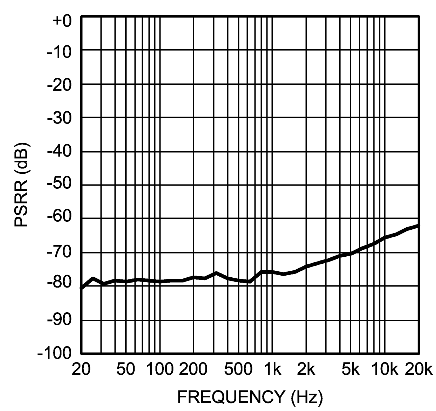
20173517

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 2, SE



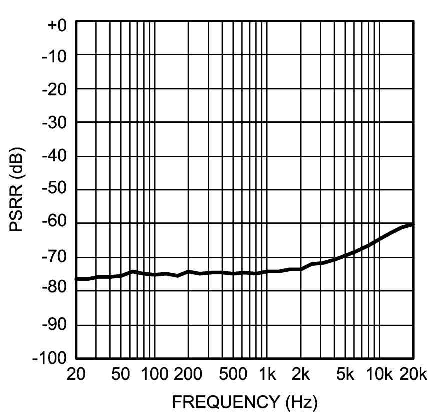
20173518

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 3, MONO



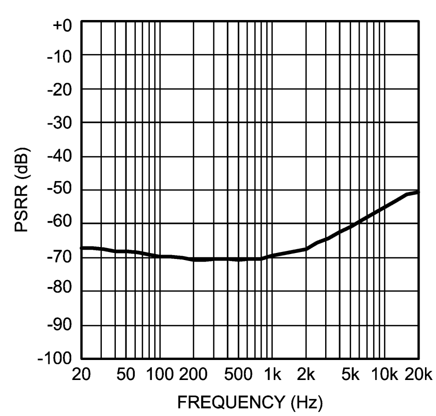
20173519

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 4, OCL



20173520

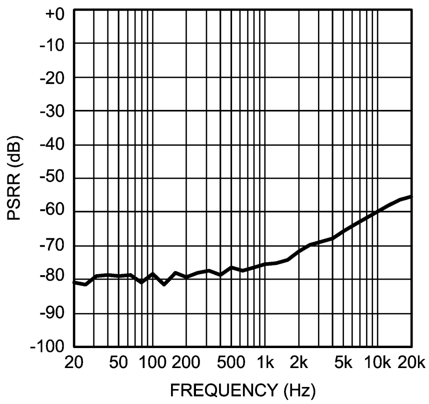
PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 4, SE



20173521

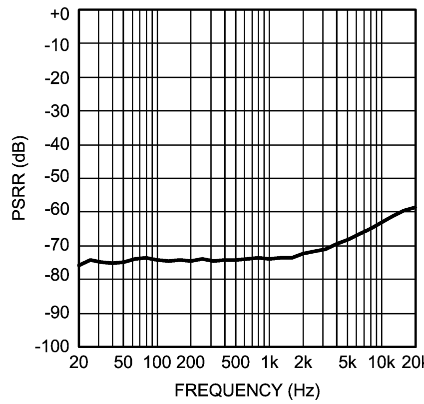
Typical Performance Characteristics (Continued)

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 5, MONO



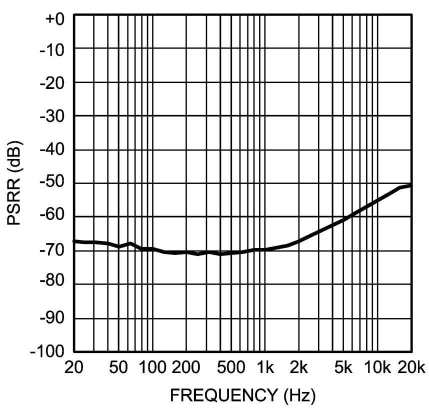
20173522

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 6, OCL



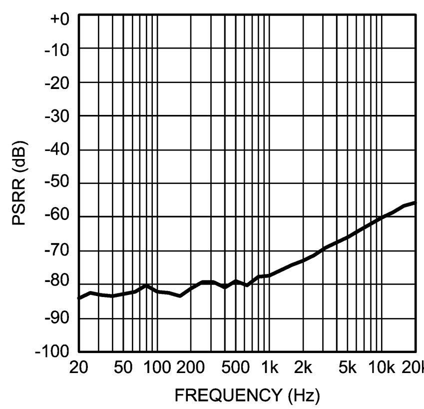
20173523

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 6, SE



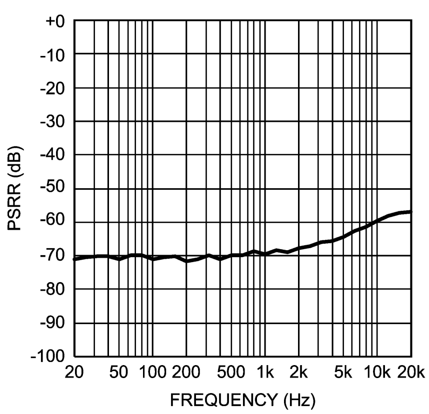
201735A4

PSRR vs Frequency
V_{DD} = 3.3V, A_V = 0dB
Mode 7, MONO



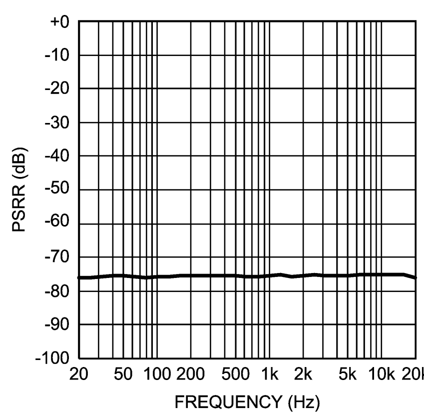
201735A5

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 1, MONO



201735A6

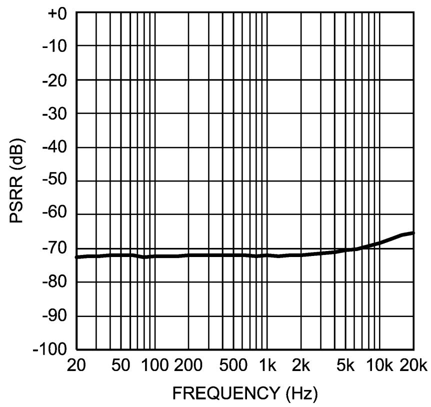
PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 2, OCL



201735A7

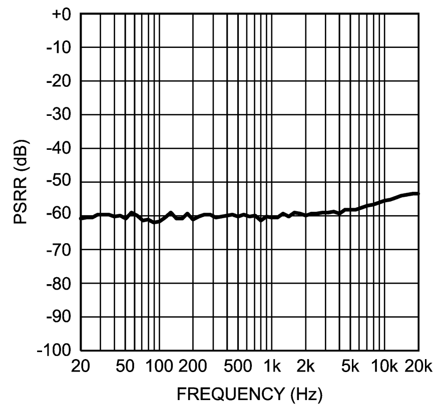
Typical Performance Characteristics (Continued)

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 2, SE



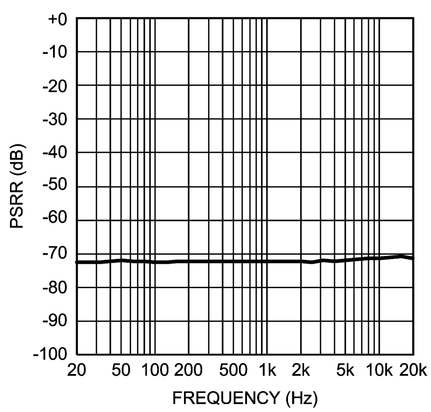
201735A8

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 3, MONO



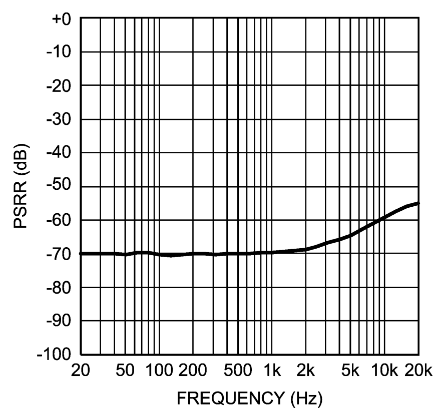
201735A9

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 4, OCL



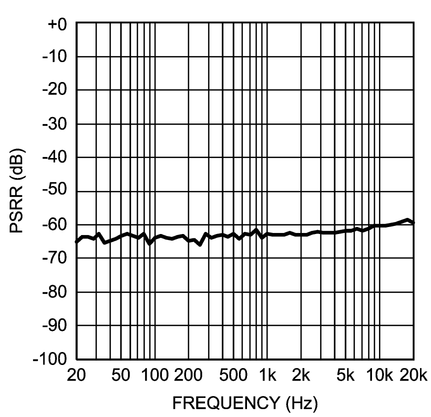
201735B0

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 4, SE



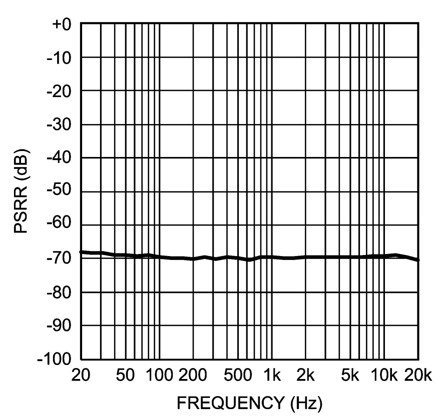
201735B1

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 5, MONO



201735B2

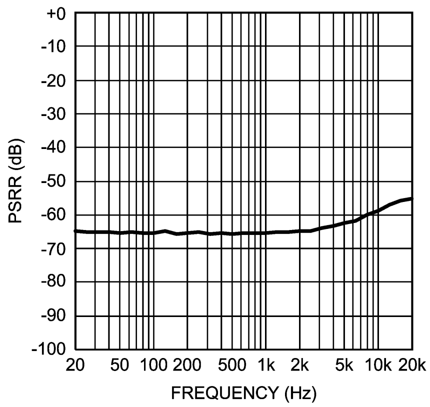
PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 6, OCL



201735B3

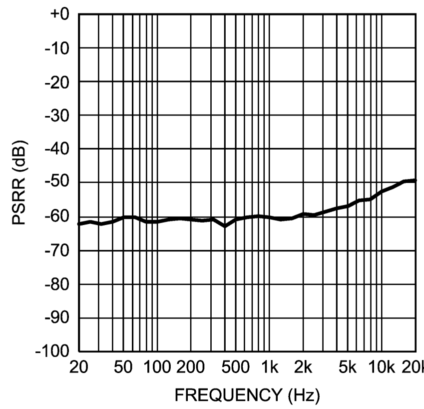
Typical Performance Characteristics (Continued)

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 6, SE



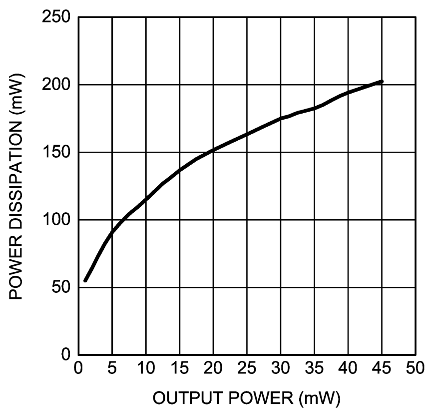
201735B4

PSRR vs Frequency
V_{DD} = 5V, A_V = 0dB
Mode 7, MONO



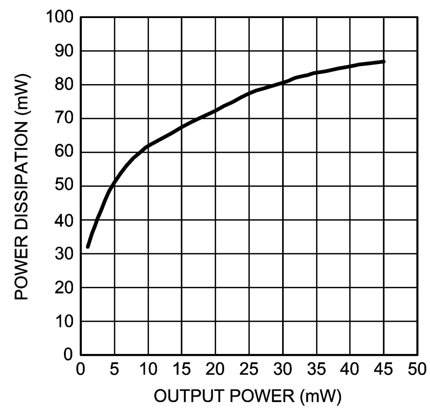
201735B5

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 7, OCL



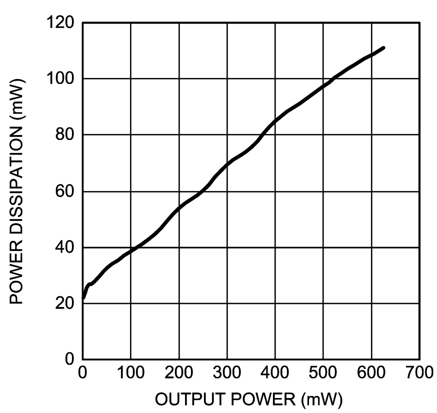
201735C9

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 7, SE



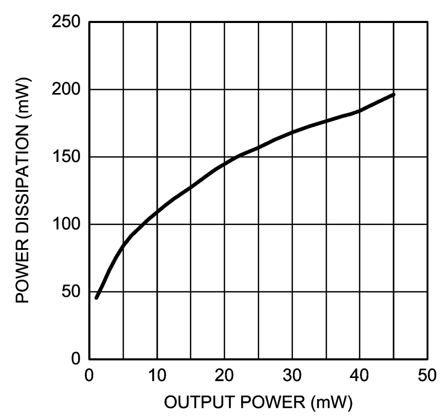
201735D0

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 1, 3, 5, MONO



201735C8

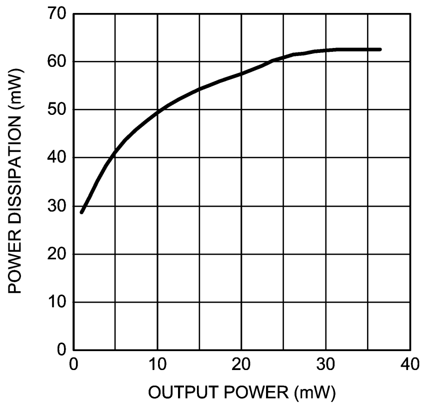
Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, OCL



201735B6

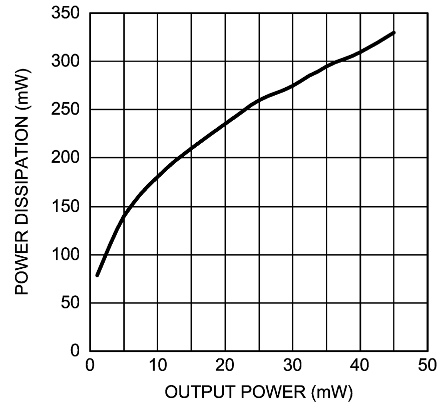
Typical Performance Characteristics (Continued)

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, SE



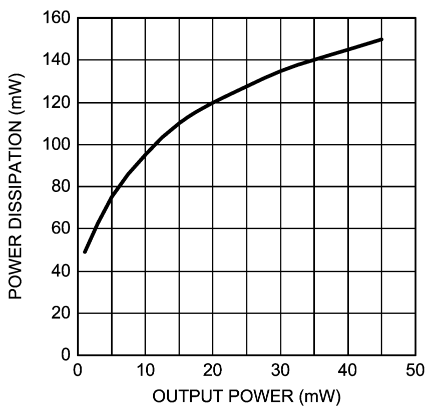
20173598

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 7, OCL



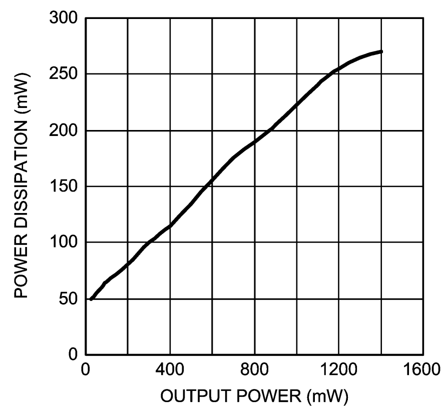
201735C0

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 7, SE



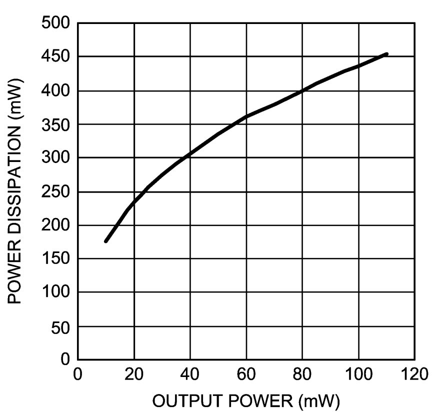
201735C1

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 1, 3, 5, MONO



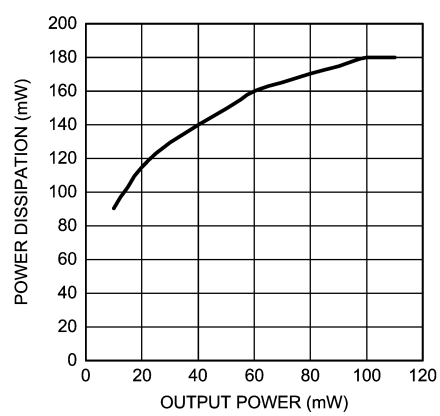
201735B7

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, OCL



201735B8

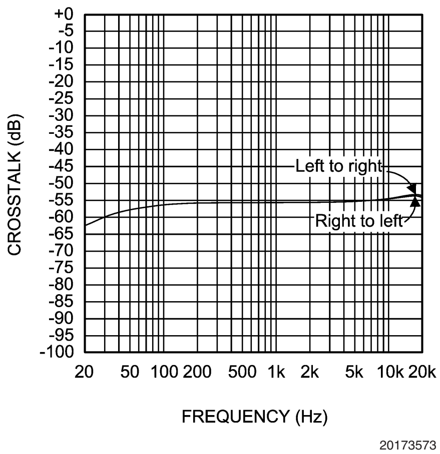
Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 2, 4, 6, SE



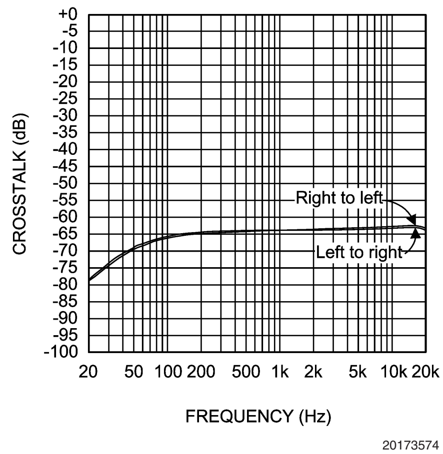
201735B9

Typical Performance Characteristics (Continued)

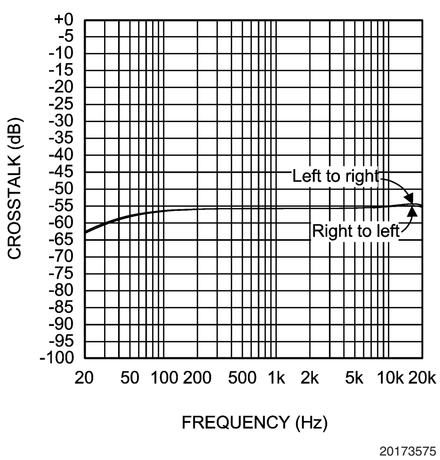
Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4, OCL



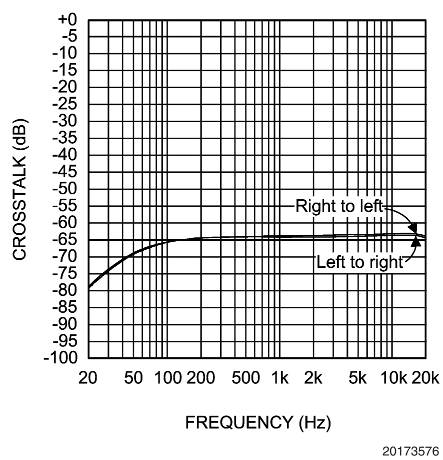
Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4, SE



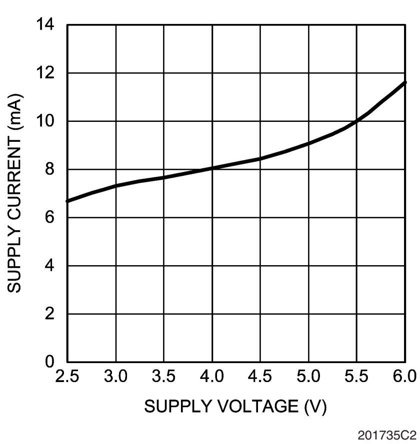
Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 4, OCL



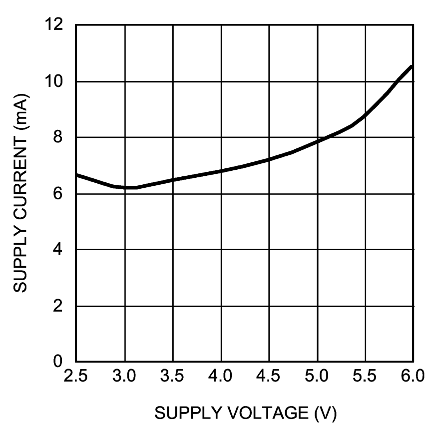
Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 4, SE



Supply Current vs Supply Voltage
No Load, Mode 7, OCL

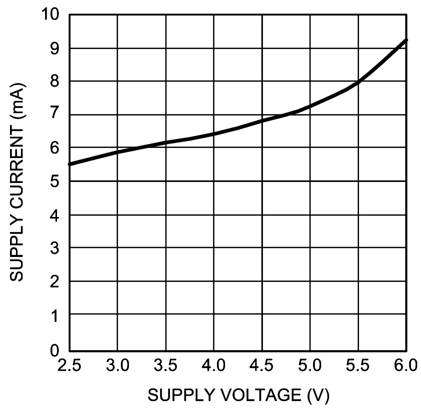


Supply Current vs Supply Voltage
No Load, Mode 7, SE



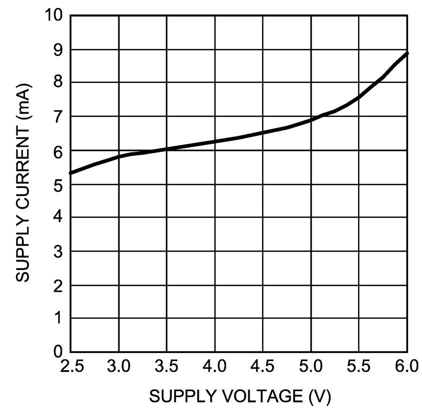
Typical Performance Characteristics (Continued)

Supply Current vs Supply Voltage
No Load, Mode 1, 3, 5, MONO



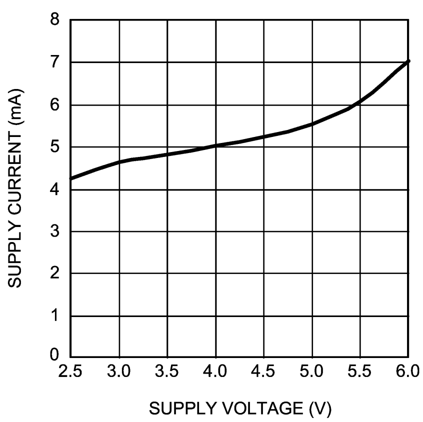
201735D1

Supply Current vs Supply Voltage
No Load, Mode 2, 4, 6, OCL



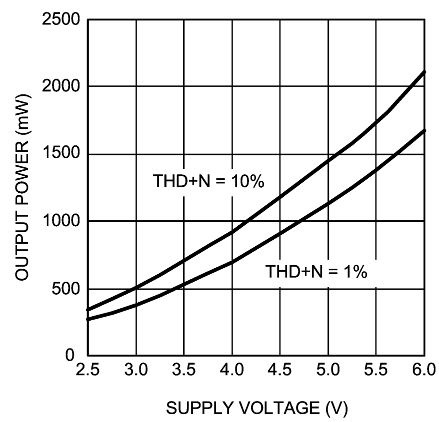
201735C4

Supply Current vs Supply Voltage
No Load, Mode 2, 4, 6, Headphone SE



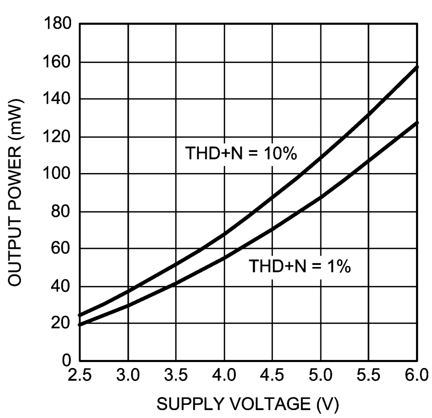
20173581

Output Power vs Supply Voltage
R_L = 8Ω, Mode 1, 3, 5, MONO



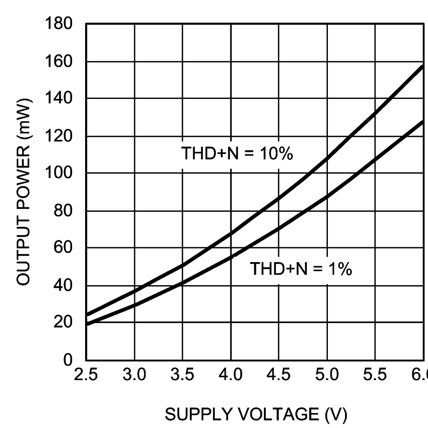
20173587

Output Power vs Supply Voltage
R_L = 32Ω, Mode 2, 4, 6, OCL



201735C7

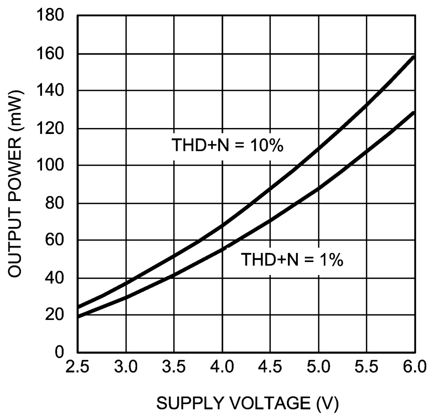
Output Power vs Supply Voltage
R_L = 32Ω, Mode 2, 4, 6, SE



20173589

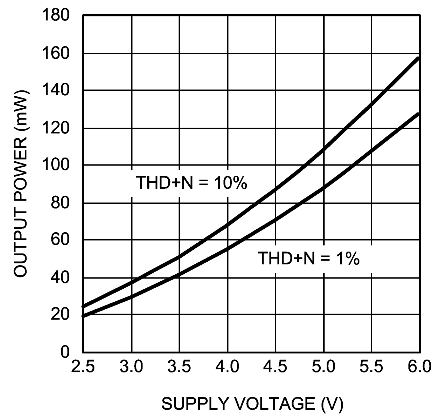
Typical Performance Characteristics (Continued)

Output Power vs Supply Voltage
R_L = 32Ω, Mode 7, OCL



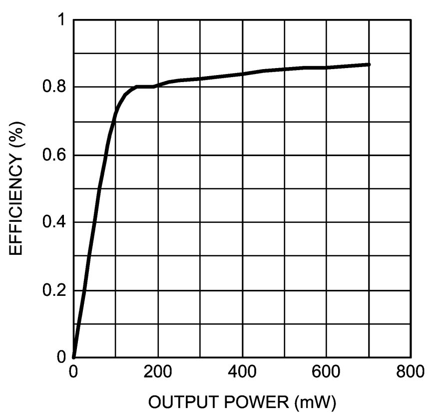
20173590

Output Power vs Supply Voltage
R_L = 32Ω, Mode 7, SE



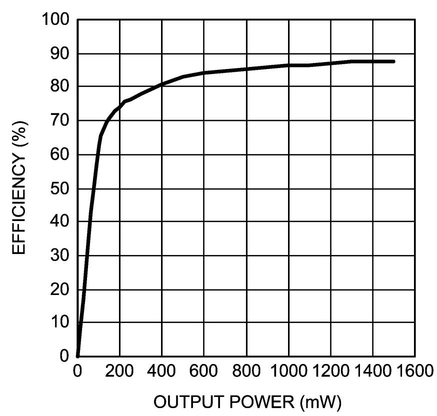
20173591

Efficiency vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, Mode 1, 3, 5, BTL



20173513

Efficiency vs Output Power
V_{DD} = 5V, R_L = 8Ω, Mode 1, 3, 5, BTL



201735C6

Application Information

I^2C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ID_ENB: This is the address select input pin.

I^2C COMPATIBLE INTERFACE

The LM4947 uses a serial bus which conforms to the I^2C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I^2C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4947.

The I^2C address for the LM4947 is determined using the ID_ENB pin. The LM4947's two possible I^2C chip addresses are of the form $111110X_10$ (binary), where X_1 = 0, if ID_ADDR is logic LOW; and X_1 = 1, if ID_ENB is logic HIGH. If the I^2C interface is used to address a number of chips in a system, the LM4947's chip address can be changed to avoid any possible address conflicts.

The bus format for the I^2C interface is shown in Figure 3. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH.

After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4947 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4947.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH.

After the data byte is sent, the master must check for another acknowledge to see if the LM4947 received the data.

The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

I^2C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

The LM4947's I^2C interface is powered up through the I^2CV_{DD} pin. The LM4947's I^2C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I^2C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

TABLE 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	EC	0
ID_ADDR = 0	1	1	1	1	1	0	0	0
ID_ADDR = 1	1	1	1	1	1	0	1	0

TABLE 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Mode Control	0	0	SE/Diff (select)	0	OCL (select)	MC2	MC1	MC0
Programmable 3D	0	1	L2R2 (select)	L1R1 (select)	N3D3	N3D2	N3D1	N3D0
Mono Volume Control	1	0	0	MVC4	MVC3	MVC2	MVC1	MVC0
Left Volume Control	1	1	0	LVC4	LVC3	LVC2	LVC1	LVC0
Right Volume Control	1	1	1	RVC4	RVC3	RVC2	RVC1	RVC0

1. Bits MVC0 — MVC4 control 32 step volume control for MONO input
2. Bits LVC0 — LVC4 control 32 step volume control for LEFT input
3. Bits RVC0 — RVC4 control 32 step volume control for RIGHT input
4. Bits MC0 — MC2 control 8 distinct modes
5. Bits N3D3, N3D2, N3D1, N3D0 control programmable 3D function
6. N3D0 turns the 3D function ON (N3D0 = 1) or OFF (N3D0 = 0)
7. Bit OCL selects between SE with output capacitor (OCL = 0) or SE without output capacitors (OCL = 1). **Default is OCL = 0**
8. N3D1 selects between two different 3D configurations
9. SE/Diff-SE/Diff = 0 for SE mode; SE/Diff = 1 for Diff mode

Application Information (Continued)

TABLE 3. Programmable National 3D Audio

	N3D3	N3D2
Low	0	0
Medium	0	1
High	1	0
Maximum	1	1

TABLE 4. Input/Output Control

	L1R1	L2R2	SE/DIFF
Select L_{IN1} and R_{IN1} Stereo Pair	1	0	0
Select L_{IN2} and R_{IN2} Stereo Pair	0	1	0
Select L_{IN1}+L_{IN2} and R_{IN1}+R_{IN2} Stereo Pair	1	1	0
Sets Stereo Inputs to Differential	x	x	1

X = Don't Care

Application Information (Continued)

TABLE 5. Output Volume Control Table

Volume Step	xVC4	xVC3	xVC2	xVC1	xVC0	Gain, dB
1	0	0	0	0	0	–59.50
2	0	0	0	0	1	–48.00
3	0	0	0	1	0	–40.50
4	0	0	0	1	1	–34.50
5	0	0	1	0	0	–30.00
6	0	0	1	0	1	–27.00
7	0	0	1	1	0	–24.00
8	0	0	1	1	1	–21.00
9	0	1	0	0	0	–18.00
10	0	1	0	0	1	–15.00
11	0	1	0	1	0	–13.50
12	0	1	0	1	1	–12.00
13	0	1	1	0	0	–10.50
14	0	1	1	0	1	–9.00
15	0	1	1	1	0	–7.50
16	0	1	1	1	1	–6.00
17	1	0	0	0	0	–4.50
18	1	0	0	0	1	–3.00
19	1	0	0	1	0	–1.50
20	1	0	0	1	1	0.00
21	1	0	1	0	0	1.50
22	1	0	1	0	1	3.00
23	1	0	1	1	0	4.50
24	1	0	1	1	1	6.00
25	1	1	0	0	0	7.50
26	1	1	0	0	1	9.00
27	1	1	0	1	0	10.50
28	1	1	0	1	1	12.00
29	1	1	1	0	0	13.50
30	1	1	1	0	1	15.00
31	1	1	1	1	0	16.50
32	1	1	1	1	1	18.00

1. x = M, L, or R

Application Information (Continued)

TABLE 6. Output Mode Selection

Output Mode Number	MC2	MC1	MC0	Handsfree Mono Output	Right HP Output	Left HP Output
0	0	0	0	SD	SD	SD
1	0	0	1	$2 \times G_M \times M$	MUTE	MUTE
2	0	1	0	SD	$G_M \times M$	$G_M \times M$
3	0	1	1	$G_L \times L + G_R \times R$	MUTE	MUTE
4	1	0	0	SD	$G_R \times R$	$G_L \times L$
5	1	0	1	$G_L \times L + G_R \times R + 2(G_M \times M)$	MUTE	MUTE
6	1	1	0	SD	$G_R \times R + G_M \times M$	$G_L \times L + G_M \times M$
7	1	1	1	$G_R \times R + G_L \times L$	$G_R \times R$	$G_L \times L$

Note: L and R are selected by modes from Table 4.
On initial POWER ON, the default mode is 000
M = Mono
R = R_{IN}
L = L_{IN}
SD = Shutdown
MUTE = Mute Mode
G_M = Mono volume control gain
G_R = Right stereo volume control gain
G_L = Left stereo volume control gain

NATIONAL 3D ENHANCEMENT

The LM4947 features a stereo headphone, 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement creates a perceived spatial effect optimized for stereo headphone listening. The LM4947 can be programmed for a “narrow” or “wide” soundstage perception. The narrow soundstage has a more focused approaching sound direction, while the wide soundstage has a spatial, theater-like effect. Within each of these two modes, four discrete levels of 3D effect that can be programmed: low, medium, high, and maximum (Table 2), each level with an ever increasing aural effect, respectively. The difference between each level is 3dB.

The external capacitors, shown in Figure 6, are required to enable the 3D effect. The value of the capacitors set the cutoff frequency of the 3D effect, as shown by Equations 1 and 2. Note that the internal 20kΩ resistor is nominal (±25%).

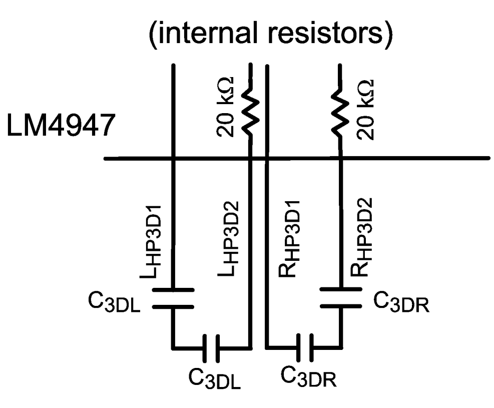


FIGURE 5. External 3D Effect Capacitors

$$f_{3DL(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DL} \quad (1)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DR} \quad (2)$$

Optional resistors R_{3DL} and R_{3DR} can also be added (Figure 7) to affect the -3dB frequency and 3D magnitude.

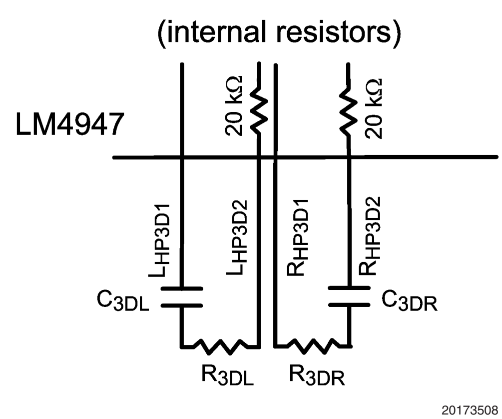


FIGURE 6. External RC Network with Optional R_{3DL} and R_{3DR} Resistors

$$f_{3DL(-3dB)} = 1 / 2\pi * (20k\Omega + R_{3DL}) * C_{3DL} \quad (3)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega + R_{3DR}) * C_{3DR} \quad (4)$$

Application Information (Continued)

ΔAV (change in AC gain) = 1 / 1 + M, where M represents some ratio of the nominal internal resistor, 20kΩ (see example below).

$$f_{3dB}\ (3D) = 1 / 2\pi\ (1 + M)(20k\Omega * C_{3D}) \quad (5)$$

$$C_{Equivalent}\ (new) = C_{3D} / 1 + M \quad (6)$$

TABLE 7. Pole Locations

R_{3D} (kΩ) (optional)	C_{3D} (nF)	M	ΔAV (dB)	f-3dB (3D) (Hz)	Value of C_{3D} to keep same pole location (nF)	new Pole Location (Hz)
0	68	0	0	117		
1	68	0.05	–0.4	111	64.8	117
5	68	0.25	–1.9	94	54.4	117
10	68	0.50	–3.5	78	45.3	117
20	68	1.00	–6.0	59	34.0	117

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 8Ω LOAD

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by an 8Ω load from 158.3mW to 156.4mW. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

POWER DISSIPATION AND EFFICIENCY

In general terms, efficiency is considered to be the ratio of useful work output divided by the total energy required to produce it with the difference being the power dissipated, typically, in the IC. The key here is "useful" work. For audio systems, the energy delivered in the audible bands is considered useful including the distortion products of the input signal. Sub-sonic (DC) and super-sonic components (>22kHz) are not useful. The difference between the power flowing from the power supply and the audio band power being transduced is dissipated in the LM4947 and in the transducer load. The amount of power dissipation in the LM4947 is very low. This is because the ON resistance of the switches used to form the output waveforms is typically less than 0.25Ω. This leaves only the transducer load as a potential "sink" for the small excess of input power over audio band output power. The LM4947 dissipates only a fraction of the excess power requiring no additional PCB area or copper plane to act as a heat sink.

The LM4947 also has a pair of single-ended amplifiers driving stereo headphones, R_{HP} and L_{HP}. The maximum internal power dissipation for R_{HP} and L_{HP} is given by equation (9) and (10). From Equations (9) and (10), assuming a 5V power supply and a 32Ω load, the maximum power dissipation for L_{HP} and R_{HP} is 40mW, or 80mW total.

$$P_{DMAX\text{-}LHP} = (V_{DD})^2 / (2\pi^2\ R_L)\text{: Single-ended Mode} \quad (7)$$

$$P_{DMAX\text{-}RHP} = (V_{DD})^2 / (2\pi^2\ R_L)\text{: Single-ended Mode} \quad (8)$$

The maximum internal power dissipation of the LM4947 occurs when all 3 amplifiers pairs are simultaneously on; and is given by Equation (11).

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}SPKROUT} + P_{DMAX\text{-}LHP} + P_{DMAX\text{-}RHP} \quad (9)$$

The maximum power dissipation point given by Equation (11) must not exceed the power dissipation given by Equation (12):

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (10)$$

The LM4947's T_{JMAX} = 150˚C. In the ITL package, the LM4947's θ_{JA} is 65˚C/W. At any given ambient temperature T_A, use Equation (12) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (12) and substituting $P_{DMAX\text{-}TOTAL}$ for P_{DMAX}' results in Equation (13). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4947's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX\text{-}TOTAL}\ \theta_{JA} \quad (11)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 104˚C for the ITL package.

$$T_{JMAX} = P_{DMAX\text{-}TOTAL}\ \theta_{JA} + T_A \quad (12)$$

Equation (14) gives the maximum junction temperature $T_{J\text{-}MAX}$. If the result violates the LM4947's 150˚C, reduce the

Application Information (Continued)

maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (11) is greater than that of Equation (12), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance). Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 1µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.1µF tantalum bypass capacitance connected between the LM4947's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4947's power supply pin and ground as short as possible. Connecting a 2.2µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figures 1 & 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor (R_i), nominal 20kΩ, and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation (15).

$$f_c = 1 / (2\pi R_i C_i) \qquad (13)$$

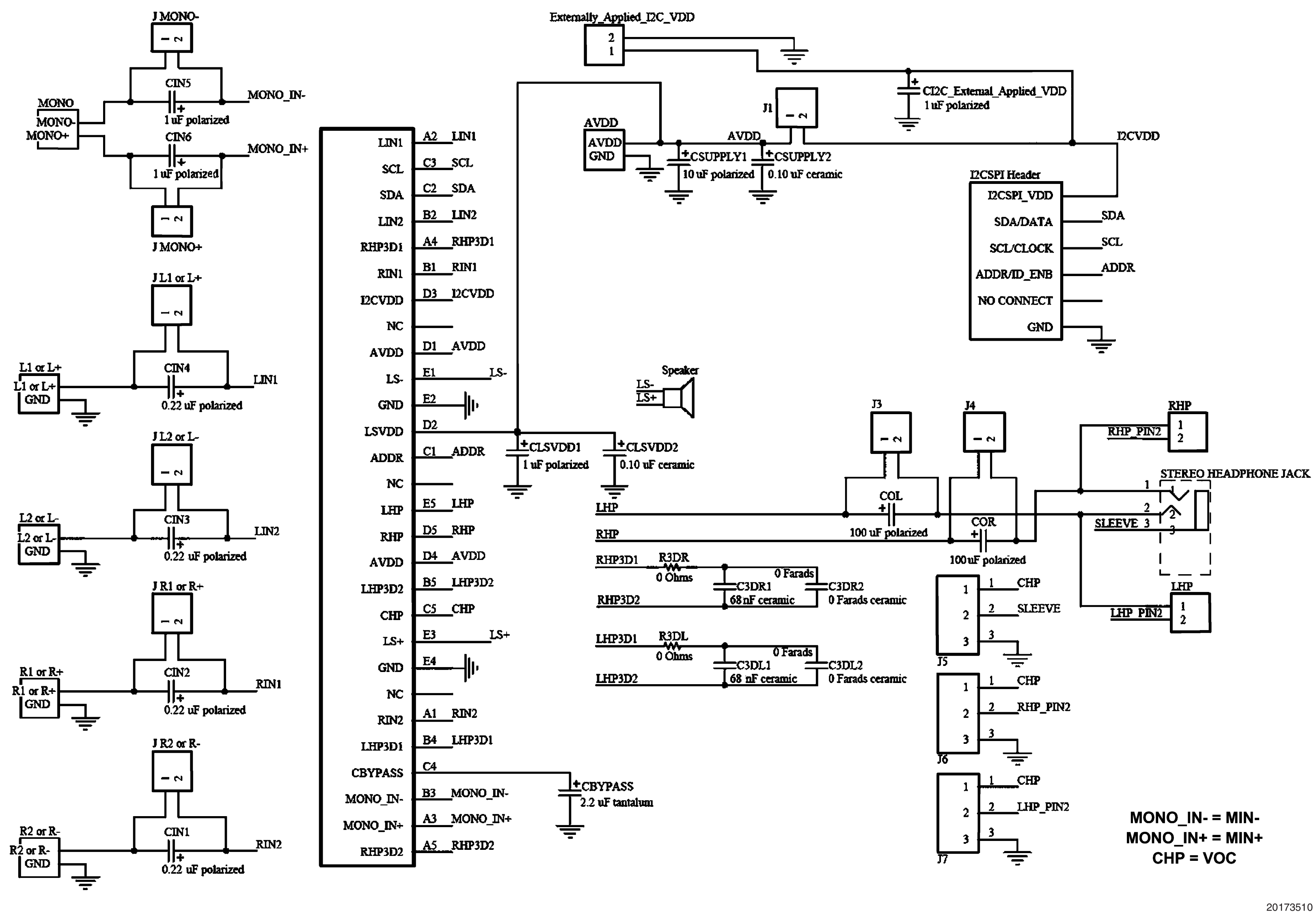
As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation (15) is 0.053µF. The 0.22µF C_i shown in *Figure 1* allows the LM4947 to drive high efficiency, full range speaker whose response extends below 40Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS bump. Since C_B determines how fast the LM4947 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4947's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 5 times to 7 times the value of C_i. This ensures that output transients are eliminated when power is first applied or the LM4947 resumes operation after shutdown.

Application Information (Continued)

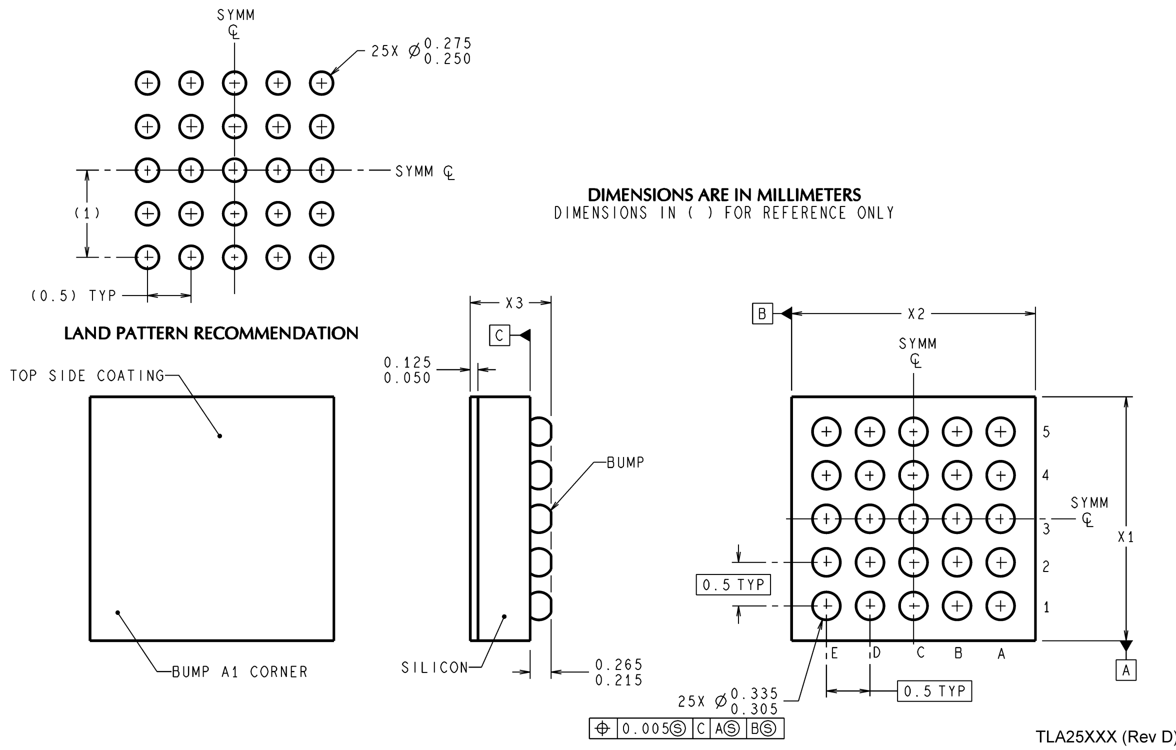
DEMO BOARD SCHEMATIC



Revision History

Rev	Date	Description
1.0	06/16/06	Initial release.
1.1	06/19/06	Changed the Class D Efficiency (n) on Typical limit (from 79 to 86) on the 5V specification table.
1.2	06/22/06	Added more Typ Perf curves.
1.3	07/18/06	Replaced some of the curves.
1.4	08/29/06	Text edits.
1.5	10/18/06	Edited micro SMD pkg drawing, Figure 1, and Figure 2. Changed I_{DDQ} typical and limit values on the 3.3V and 5.0V specification table. Removed CMRR SE condition and changed typical values for CMRR BTL on 3.3V and 5.0V specification table. Changed Mute Attenuation typical value on 5.0V specification table.

Physical Dimensions inches (millimeters) unless otherwise noted



TLA25XXX (Rev D)

25 – Bump micro SMD
Order Number LM4947TL
NS Package Number TLA25BBA
Dimensions are in millimeters
X_1 = 2.517 ± 0.01 X_2 = 2.517 ± 0.01 X_3 = 0.600 ± 0.10

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