October 2001

National Semiconductor

LM9833 48-Bit Color, 1200dpi USB Image Scanner

General Description

The LM9833 is a complete USB image scanner system on a single IC. The LM9833 provides all the functions (image sensor control, illumination control, analog front end, pixel processing function image data buffer/DRAM controller, microstepping motor controller, and USB interface) necessary to create a high performance color scanner. The LM9833 scans images in 48 bit color/16 bit gray, and has output data formats for 48 and 24bit color/16 and 8 bit gray. The LM9833 supports sensors with pixel counts of up to 16384 pixels x 3 colors (1200 dpi x 13.6 inches).

The LM9833's low operating and suspend mode supply currents allow design of USB bus-powered scanners. The only additional active components required are an external 4Mbit or 16Mbit DRAM for data buffering and power transistors for the stepper motor.

Applications

- Color Flatbed Document Scanners
- Color Sheetfed Document Scanners

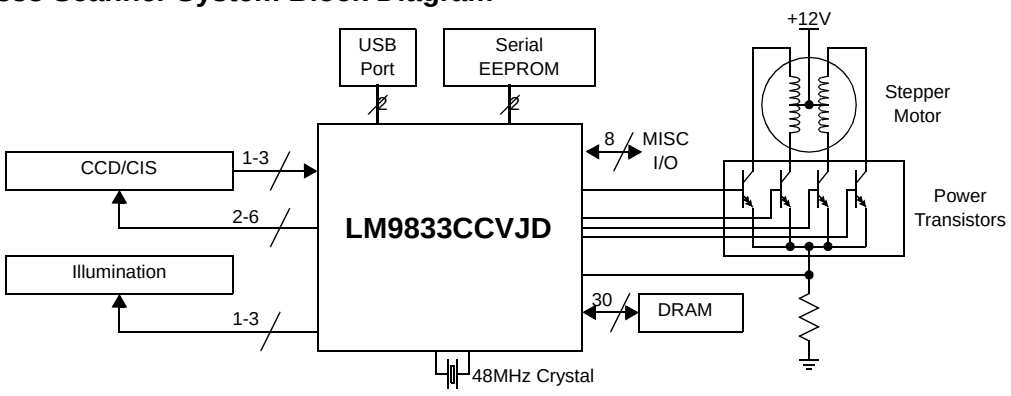
Key Specifications

• Analog to Digital Converter Resolution	16 Bits
• Maximum Pixel Conversion Rate	6MHz
• A4 Color 150dpi scan time	<10 seconds
• A4 Color 300dpi scan time	<40 seconds
• A4 Color 600dpi scan time	<160 seconds
• Supply Voltage	
- LM9833	+4.75V to +5.25V
- LM9833 DRAM I/O	+2.85 to +5.25V
• Maximum Operating Current Consumption	136mA
• Maximum Suspend Current Consumption	175µA

Features

- 16 bit ADC digitizes at up to 6Mpixels/s (2M RGB pixels/sec).
- Digital Pixel Processing provides 1200, 800, 600, 400, 300, 200, 150, and 100dpi horizontal resolution from a 1200dpi sensor and 600, 400, 300, 200, 150, 100, 75, and 50dpi horizontal resolution from a 600dpi sensor.
- Provides 50-2400dpi vertical resolution in 1 dpi increments.
- Pixel rate error correction for gain (shading) and offset errors.
- Supports 4 or 16Mbit external DRAMs.
- Multiple CCD clocking rates allows matching of CCD clock to scan resolution and pixel depth for maximum scan speed.
- Stepper motor control tightly coupled with image data buffer management to maximize data transfer efficiency.
- PWM stepper motor current control allows microstepping for the price of fullstepping.
- USB interface for Plug and Play operation on USB-equipped computers.
- Serial EEPROM option for custom Vendor and Product IDs.
- Support for USB bus-powered operation.
- Pixel depths of 1, 2, or 4 bits are packed into bytes for faster scans of line art and low pixel depth images.
- Supports 3 channel CCDs and 1 channel CIS sensors.
- 3 (R, G, and B) 12-bit, user-programmable gamma correction tables.
- Compatible with a wide range of color linear CCDs and Contact Image Sensors (CIS).
- Operates with 48MHz external crystal.
- Internal bandgap voltage reference.
- 100 pin TQFP package

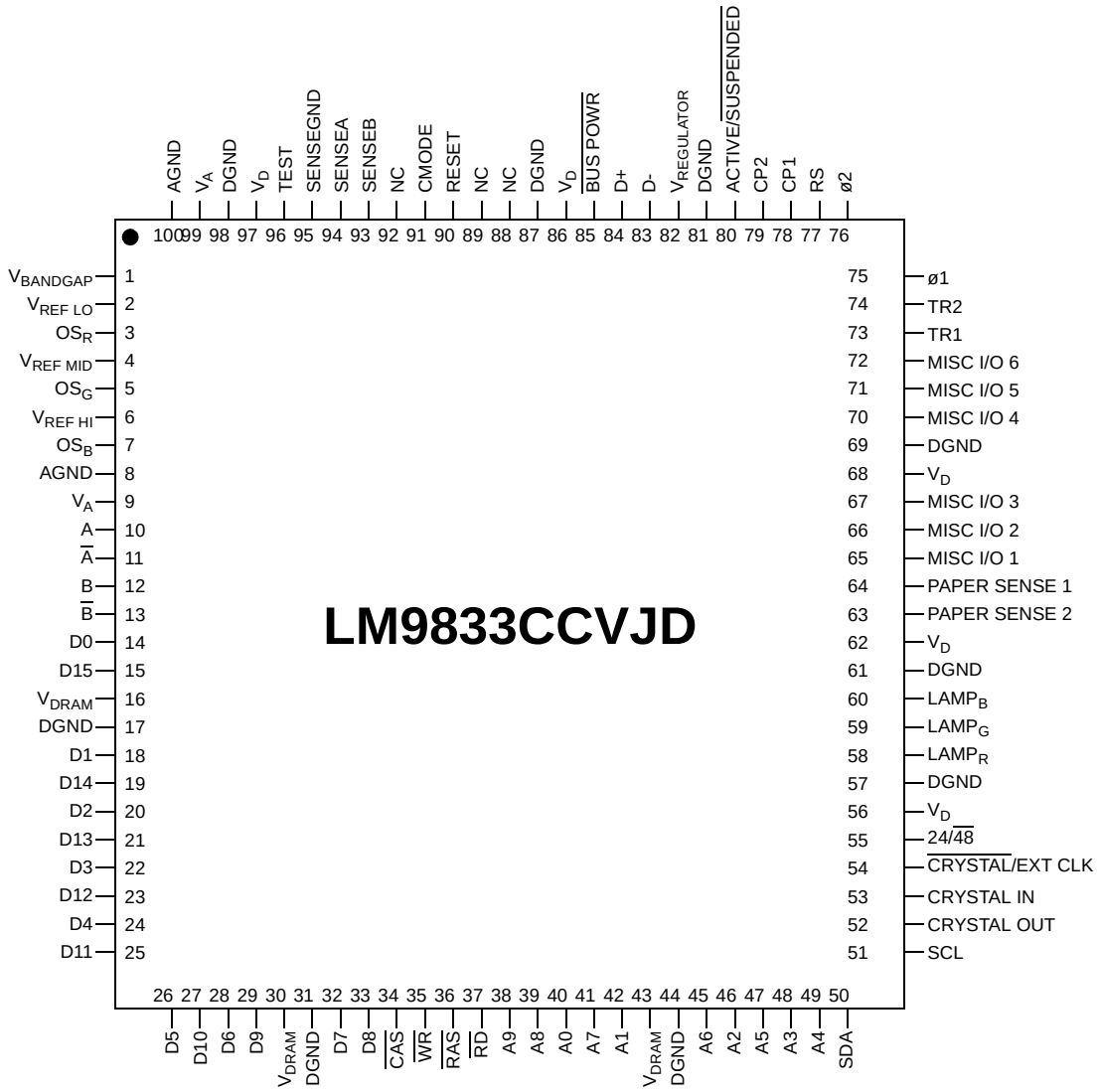
LM9833 Scanner System Block Diagram



Ordering Information

Commercial (0°C ≤ T_A ≤ +70°C)	Package
LM9833CCVJD	VJD100A 100 Pin Thin Quad Flatpac

Connection Diagram



Ordering Information

Commercial ($0°C \leq T_A \leq +70°C$)	Package
LM9833CCVJD	VJD100A 100 Pin Thin Quad Flatpac

Pin Descriptions

USB Interface	
D+, D-	Digital I/O. USB Interface signals
$\overline{\text{BUS POWER}}$	Digital Input. Tie low for bus powered systems, tie high for external power.
ACTIVE/ $\overline{\text{SUSPENDED}}$	Digital Output. Low in Suspend mode. High in operational mode. Used to control external regulators, other components.
SDA	Digital I/O. Serial Data to/from external EEPROM.
SCL	Digital Output. Serial Clock Output to external EEPROM.
Analog	
OS_R, OS_G, OS_B	Analog Inputs. These inputs (for Red, Green, and Blue) should be tied to the sensor's output signal through DC blocking capacitors. If unused, tie to ground through DC blocking capacitors.
$V_{REF\ LO}$	Analog Output/Input. Bypass to AGND with a 0.047µF monolithic capacitor. Do not put a DC load on this pin.
$V_{REF\ MID}$	Analog Output/Input. Bypass to AGND with a 0.047µF monolithic capacitor. Do not put a DC load on this pin.
$V_{REF\ HI}$	Analog Output/Input. Bypass to AGND with a 0.047µF monolithic capacitor. Do not put a DC load on this pin.
$V_{BANDGAP}$	Analog Output. Bypass to AGND with a 0.047µF monolithic capacitor. Do not put a DC load on this pin.
DRAM	
D0 (LSB) -D15 (MSB)	Digital Inputs/Outputs. This is the 16 bit data path between the external DRAM and the LM9833.
$\overline{\text{RD}}$	Digital Output. Read signal to external DRAM.
$\overline{\text{WR}}$	Digital Output. Write signal to external DRAM.
A0-A9	Digital Outputs. Address pins for up to 1M x 16 external DRAM.
$\overline{\text{RAS}}$	Digital Output. Row Address Strobe signal.
$\overline{\text{CAS}}$	Digital Output. Column Address Strobe signal.
Scanner Support I/O	
PAPER SENSE 1-2	Digital Inputs. Programmable, used for sensing home position, paper, front panel switches, etc.
MISC I/O 1-6	Digital Inputs/Outputs. Programmable, used for front panel switches, status LEDs, etc. At power-on and in Suspend Mode, MISC I/Os 1-3 are inputs and MISC I/Os 4-6 are outputs.

Stepper Motor	
A, B, $\overline{\text{A}}$, $\overline{\text{B}}$	Digital Outputs. Pulses to stepper motor drive circuitry.
$SENSE_A$, $SENSE_B$	Analog Inputs. Current sensing for stepper motor's PWM current control.
$SENSE_{GND}$	Analog Input. Ground sense input for stepper motor's PWM current control.
Sensor Control	
ø1	Digital Output. CCD/CIS clock signal phase 1.
ø2	Digital Output. CCD/CIS clock signal phase 2.
RS	Digital Output. Reset pulse for the CCD/CIS.
CP1	Digital Output. Clamp pulse for the CCD/CIS.
CP2	Digital Output. Clamp pulse for the CCD/CIS.
TR1, TR2	Digital Outputs. Transfer pulses for the CCD/CIS.
$LAMP_R$, $LAMP_G$, $LAMP_B$	Digital Outputs. Used to control R, G, and B LEDs of single output CIS, as well as brightness of CCFL. The CDS signal can be seen on $LAMP_B$ in a test mode (see register 5E, bit 7).
Master Clock Generation	
CRYSTAL IN	Digital Input. Used with CRYSTAL OUT and an external 48MHz crystal to form a crystal oscillator.
CRYSTAL OUT	Digital Output. Used with CRYSTAL IN and an external 48MHz crystal to form a crystal oscillator.
$\overline{\text{CRYSTAL}}$/ EXT CLOCK	Digital Input. Tie to DGND for operation with an external crystal. Pull up to V_D to drive CRYSTAL OUT with an external TTL or CMOS clock source.
24/$\overline{48}$	Digital Input. Tie to DGND for operation with a 48MHz crystal or external clock. Pull up to V_D for operation with a 24MHz crystal or external clock. NOTE: Operation at 24MHz is not guaranteed - always use a 48MHz crystal.
Miscellaneous	
$V_{REGULATOR}$	Digital Output. This is the regulated 3.3V supply (generated from V_D) that powers the USB transceiver. It should be used as the terminal voltage for the 1.5k D+ pullup resistor, and bypassed to DGND with a 0.047µF monolithic capacitor.
RESET	Digital input. Take high to force device into Power On Reset state, low to exit reset state.
TEST	Analog Output.
CMODE	Digital Input. Test mode, always tie high.

Pin Descriptions (Continued)

Analog Power Supplies (4 pins)	
V_A (2)	This is the positive supply pin for the analog supply. It should be connected to a voltage source of +5V and bypassed to AGND with a 0.1µF monolithic capacitor in parallel with a 10µF tantalum capacitor.
AGND (2)	This is the ground return for the analog supply.
Digital Power Supplies (17 pins)	
V_D (5)	This is the positive supply pin for the digital supply. It should be connected to a voltage source of +5V and bypassed to DGND with a 0.1µF monolithic capacitor.
V_{DRAM}(3)	This is the positive supply pin for the digital supply for the LM9833's external DRAM I/O. It also powers the A, B, $\overline{A}$, and $\overline{B}$ stepper motor outputs. It should be connected to a 3 or 5V supply and bypassed to the closest DGND pin with a 0.1µF monolithic capacitor.
DGND (9)	This is the ground return for V_D and V_{DRAM}.

Absolute Maximum Ratings (Notes 1 & 2)

Positive Supply Voltage (V^+=V_A=V_D=V_{DRAM})	
With Respect to GND=AGND=DGND	6.5V
Voltage On Any Input or Output Pin	-0.3V to V^++0.3V
Input Current at any pin (Note 3)	±25mA
Package Input Current (Note 3)	±50mA
Package Dissipation at T_A = 25°C	(Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2000 V
Machine Model	250 V
Soldering Information	
Infrared, 10 seconds (Note 6)	235°C
Storage Temperature	-65°C to +150°

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM9833CCVJD	0°C≤T_A≤+70°C
V_A Supply Voltage	+4.75V to +5.25V
V_D Supply Voltage	+4.75V to +5.25V
V_{DRAM} Supply Voltage	+2.85V ≤ V_{DRAM} ≤ V_D+100mV
$\lvert V_A - V_D \rvert$	≤ 100mV
Input Voltage Range	-0.05V to V^+ + 0.05V

Electrical Characteristics

The following specifications apply for AGND=DGND=0V, V_A=V_D=V_{DRAM}=+5.0V_{DC}, $f_{CRYSTAL\ IN}$= 48MHz, Analog Bias Current = 100%, unless otherwise noted. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 8, 9, & 10)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Full Channel Characteristics (in units of 12 bit LSBs unless otherwise noted)					
	Resolution with No Missing Codes		16	12	bits (min)
DNL	Differential Non-Linearity (Note 14)	Bias Current = 80%, V_{DRAM}=3.3V	-0.45 +0.75	**-0.9** **+2.4**	LSB (min) LSB (max)
INL	Integral Non-Linearity Error (Notes 11 & 14)	Bias Current = 80%, V_{DRAM}=3.3V	-2.3 +1.7	**-8.5** **+7.5**	LSB (min) LSB (max)
C	Analog Channel Gain Constant (ADC Codes/V), referred to 16 bits.	Includes voltage reference variation, gain setting = 1	32768	**29648** **37200**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error		26	**-34** **+76**	mV (min) mV (max)
V_{OS2}	Pre-PGA Analog Channel Offset Error		-30	**-80** **+31**	mV (min) mV (max)
V_{OS3}	Post-PGA Analog Channel Offset Error		-26	**-75** **+26**	mV (min) mV (max)
Coarse Color Balance PGA Characteristics (Configuration Registers 3B, 3C, and 3D)					
	Monotonicity			**5**	bits (min)
	G_0 (Minimum PGA Gain)	PGA Setting = 0	0.93	**0.90** **0.96**	V/V (min) V/V (max)
	G_{31} (Maximum PGA Gain)	PGA Setting = 31	3.00	**2.95** **3.10**	V/V (min) V/V (max)
	x3 Boost Gain	x3 Boost Setting On (bit B5 of Gain Register is set)	2.94	**2.85** **3.04**	V/V (min) V/V (max)
	Gain Error at any gain (Note 13)		0.3	**-0.6** **+0.9**	% (min) % (max)
Static Offset DAC Characteristics (Configuration Registers 38, 39, and 3A)					
	Monotonicity			**6**	bits (min)
	Offset DAC LSB size	PGA gain = 1	9	**6** **12**	mV (min) mV (max)
	Offset DAC Adjustment Range	PGA gain = 1	±278	**±256**	mV (min)

Electrical Characteristics (Continued)

The following specifications apply for AGND=DGND=0V, V_A=V_D=V_{DRAM}=+5.0V_{DC}, $f_{CRYSTAL\ IN}$= 48MHz, Analog Bias Current = 100%, unless otherwise noted. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 8, 9, & 10)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CCD/CIS Source Requirements for Full Specified Accuracy and Dynamic Range (Note 12)					
$V_{CCDPEAK}$	Sensor's Maximum Output Signal Amplitude before LM9833 Analog Front End Saturation	Gain = 0.933 Gain = 3.0 Gain = 9.0	1.9 0.6 0.19		V V V
Analog Input Characteristics					
	Average OS_R, OS_G, OS_B Input Current	CDS Enabled, OS = 3.5V_{DC}	±3		nA
	OS_R, OS_G, OS_B Input Current	CDS Disabled, OS = 3.5V_{DC}	±26	**±30**	µA (max)
Internal Voltage Reference Characteristics					
$V_{BANDGAP}$	Voltage Reference Output Voltage		1.23		V
$V_{REF\ LO}$	Negative Reference Output Voltage		$V_{REF\ MID}$-1.0		V
$V_{REF\ MID}$	Midpoint Reference Output Voltage		V_A/2.0		V
$V_{REF\ HI}$	Positive Reference Output Voltage		$V_{REF\ MID}$+1.0		V
$V_{REGULA-TOR}$	USB I/O Voltage Regulator		3.3		V

DC and Logic Electrical Characteristics

The following specifications apply for AGND=DGND=0V, V_A=V_D=V_{DRAM}=+5.0V_{DC} unless otherwise noted, $f_{CRYSTAL\ IN}$= 48MHz. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 8, 9, & 10)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Digital Input Characteristics for D0-D15 (DRAM Interface)					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{DRAM}=5.25V V_{DRAM}=3.6V		**2.0** **2.0**	V (min) V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_{DRAM}=4.75V V_{DRAM}=2.85V		**0.8** **0.8**	V (max) V (max)
I_{IN}	Input Leakage Current		±0.1		µA
C_{IN}	Input Capacitance		5		pF
Digital Input Characteristics for PAPER SENSE 1-2, MISC I/O 1-6, SDA, $\overline{\text{BUS POWER}}$, $\overline{\text{CRYSTAL/EXT CLOCK}}$, 24/$\overline{48}$, RESET, CMODE					
$V_{IN(1)}$	Logical "1" Input Voltage	V_D=5.25V		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_D=4.75V		**0.8**	V (max)
I_{IN}	Input Leakage Current		±0.1		µA
C_{IN}	Input Capacitance		5		pF
Digital Input Characteristics for D+, D-					
$V_{IN(1)}$	Logical "1" Input Voltage	V_D=5.25V		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_D=4.75V		**0.8**	V (max)
I_{IN}	Input Leakage Current		±0.1		µA
C_{IN}	Input Capacitance		5		pF

DC and Logic Electrical Characteristics (Continued)

The following specifications apply for AGND=DGND=0V, $V_A=V_D=V_{DRAM}=+5.0V_{DC}$ unless otherwise noted, $f_{CRYSTAL\ IN}$= 48MHz. **Boldface limits apply for $T_A=T_J=T_{MIN}$ to T_{MAX}**; all other limits $T_A=T_J=25°C$. (Notes 8, 9, & 10)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Digital Output Characteristics for D0-D15, A0-A9, $\overline{RD}$, $\overline{WR}$, $\overline{RAS}$, $\overline{CAS}$ (DRAM Interface)					
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{DRAM}=4.75V, I_{OUT}=-4mA V_{DRAM}=2.85V, I_{OUT}=-4mA		**2.4** **2.4**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{DRAM}=4.75V, I_{OUT}=4mA V_{DRAM}=2.85V, I_{OUT}=4mA		**0.4** **0.4**	V (max) V (max)
Digital Output Characteristics for A, B, $\overline{A}$, $\overline{B}$					
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{DRAM}=4.75V, I_{OUT}=-10mA V_{DRAM}=2.85V, I_{OUT}=-10mA		**2.4** **2.4**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{DRAM}=4.75V, I_{OUT}=4mA V_{DRAM}=2.85V, I_{OUT}=4mA		**0.4** **0.4**	V (max) V (max)
Digital Output Characteristics for MISC I/O 1-6, TR1, TR2, ø1, ø2, RS, CP1, CP2, $LAMP_R$, $LAMP_G$, $LAMP_B$					
$V_{OUT(1)}$	Logical "1" Output Voltage	V_D=4.75V, I_{OUT}=-4mA		**2.4**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_D=4.75V, I_{OUT}=4mA		**0.4**	V (max)
Digital Output Characteristics for D+, D-					
$V_{OUT(1)}$	Logical "1" Output Voltage	V_D=4.75V, I_{OUT}=-1mA		**2.4**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_D=4.75V, I_{OUT}=3mA		**0.4**	V (max)
CRYSTAL IN, CRYSTAL OUT Characteristics					
$XTAL_{OUT\ DC}$	CRYSTAL OUT Bias Level (Offset)		0.8		V
$XTAL_{OUT\ AC}$	CRYSTAL OUT Amplitude	$f_{CRYSTAL}$ = 48MHz	0.8		V_{P-P}
Power Supply Characteristics (Note 14)					
I_A	Analog Supply Current (V_A pins)	Operating (Bias Current = 80%)	65	**91**	mA (max)
I_D	Digital Supply Current (V_D pins)	Operating (Bias Current = 80%)	35	**41**	mA (max)
I_{DRAM}	DRAM Supply Current (V_{DRAM} pins)	Operating, V_{DRAM} = 5V Operating, V_{DRAM} = 3V	2 1	**8** **5**	mA (max) mA (max)
$I_{SUSPEND}$	Total Suspend Current ($I_A+I_D+I_{DRAM}$)		19	**175**	µA (max)

AC Electrical Characteristics

The following specifications apply for AGND=DGND=0V, V_A=V_D=V_{DRAM}=+5.0V_{DC} unless otherwise noted, $f_{CRYSTAL\ IN}$= 48MHz, MCLK DIVIDER = 1.0 (unless otherwise noted), f_{MCLK} = $f_{CRYSTAL\ IN}$/MCLK DIVIDER, $f_{ADC\ CLK}$ = f_{MCLK}/8, C_L (databus loading) = 20pF/pin. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 8, 9, & 10)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
DRAM Timing (Figure 1)					
$t_{\overline{RD}\ SETUP}$	Data valid to $\overline{RD}$ rising edge	V_{DRAM}=5.0V V_{DRAM}=3.3V		**26** **35**	ns (min) ns (min)
$t_{\overline{RD}\ HOLD}$	Data valid after $\overline{RD}$ rising edge			**0**	ns (min)
$t_{\overline{WR}\ SETUP}$	Data valid before $\overline{WR}$ falling edge			**5**	ns (min)
$t_{\overline{WR}\ HOLD}$	Data valid after $\overline{WR}$ rising edge			**10**	ns (min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND=AGND=DGND=0V, unless otherwise specified.

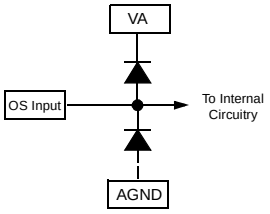
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN}<GND or V_{IN}>V_A or V_D), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is P_D = ($T_J$max - T_A) / Θ_{JA}. $T_J$max = 150°C for this device. The typical thermal resistance (Θ_{JA}) of this part when board mounted is 53°C/W.

Note 5: Human body model, 100pF capacitor discharged through a 1.5kΩ resistor. Machine model, 200pF capacitor discharged through a 0Ω resistor.

Note 6: See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Two diodes clamp the OS analog inputs to AGND and VA as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the sensor, prevents damage to the LM9833 from transients during power-up.



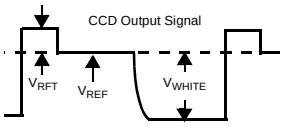
Note 8: For best performance, it is required that all supply pins be powered from the same power supply with separate bypass capacitors at each supply pin.

Note 9: Typicals are at T_J=T_A=25°C, $f_{CRYSTAL\ IN}$ = 48MHz, and represent most likely parametric norm.

Note 10: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the ADC.

Note 12: V_{REF} is defined as the CCD OS voltage for the reference period following the reset feedthrough pulse. V_{WHITE} is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to the reference level, V_{REF} . V_{RFT} is defined as the peak positive deviation above V_{REF} of the reset feedthrough pulse. The maximum correctable range of pixel-to-pixel V_{WHITE} variation is defined as the maximum variation in V_{WHITE} (due to PRNU, light source intensity variation, optics, etc.) that the LM9833 can correct for using its internal PGA.



Note 13: PGA Gain Error is the maximum difference between the measured gain for any PGA code and the ideal gain calculated by using the formula $Gain_{PGA}\left(\frac{V}{V}\right) = G_0 + X\frac{PGA\ code}{32}$ where $X = (G_{31} - G_0)\frac{32}{31}$.

Note 14: DNL, INL, and Power Supply Current are specified at the 80% Bias Current Setting (Register 9). This is the maximum recommended Bias Current setting, and gives the best analog performance as well as lower power consumption for USB-bus powered applications.

Timing Diagrams

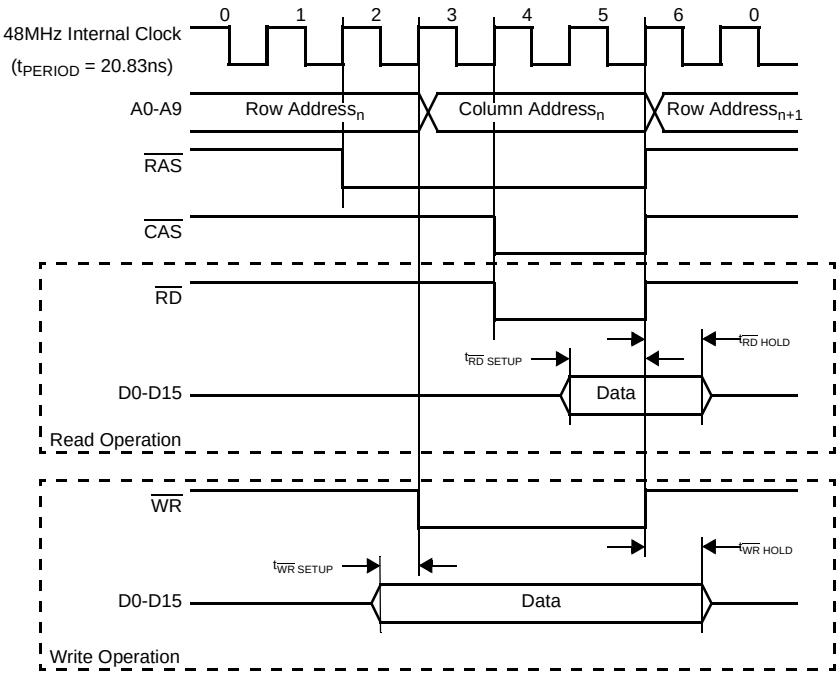


Figure 1: DRAM Read and Write

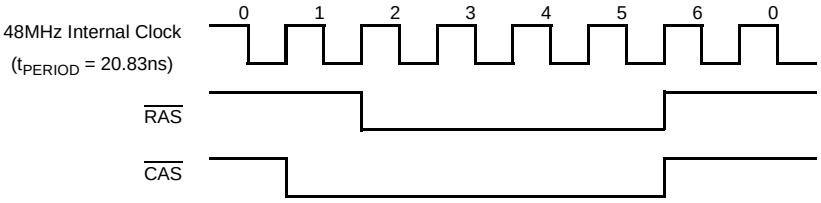


Figure 2: DRAM Refresh ($\overline{CAS}$ before $\overline{RAS}$)

Register Listing

Registers in bold boxes are reset to that value on power-up. All register addresses are in hexadecimal. All other numbers are decimal unless otherwise noted.

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
IMAGE BUFFER (READ ONLY)										
00	**Pixel (Image) Data**	n	n	n	n	n	n	n	n	One byte of image data.
STATUS REGISTERS (READ ONLY)										
01	**Image Data Available In Buffer**	n	n	n	n	n	n	n	n	n*2 (256k x 16 DRAM) or n*8 (1M x 16 DRAM) kilobytes of image data is available
02	**PAPER SENSE 1 State**								0	False
	read clears bit if edge sensitive input.								1	True
	PAPER SENSE 2 State							0		False
	read clears bit if edge sensitive input.							1		True
	MISC I/O 1 State						0			False
	read clears bit if edge sensitive input.						1			True
	MISC I/O 2 State					0				False
	read clears bit if edge sensitive input.					1				True
	MISC I/O 3 State				0					False
	read clears bit if edge sensitive input.				1					True
	MISC I/O 4 State			0						False
	read clears bit if edge sensitive input.			1						True
	MISC I/O 5 State		0							False
	read clears bit if edge sensitive input.		1							True
	MISC I/O 6 State	0								False
	read clears bit if edge sensitive input.	1								True
DATAPORT REGISTERS										
03	**DataPort Target**							0	0	Offset Coefficient Data
								0	1	Gain Coefficient Data
								1	0	Gamma Lookup Table
								1	1	N/A
	DataPort Target Color					0	0			Red
						0	1			Green
						1	0			Blue
						1	1			N/A
	Pause (Read Only) This bit indicates whether or not the scanner is currently paused due to a buffer full condition.				0					Normal State
					1					The scanner is currently in the pause/reverse cycle.
	DRAM Test		0							Normal Operation
			1							DRAM Test mode
04	**DataPort Address - MSB**		R/W	a	a	a	a	a	a	Address of location to be read/written to. a = 0 to 4095 for gamma tables, 0 to 16383 for Offset and Gain Coefficient Data Addresses greater than these are illegal. Bit D6 of register 4 indicates whether next operation will be a Read (D6=1) or a Write (D6=0).
05	**DataPort Address - LSB**	a	a	a	a	a	a	a	a	
06	**DataPort**	n	n	n	n	n	n	n	n	Data to be read from or written to the address of the currently selected Dataport Target. The DataPort Address is automatically incremented whenever one (gamma data) or two (Gain/Offset Data) bytes are read from or written to this register.

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
COMMAND REGISTER										
07	**Command Register** This register is used to start and end a scan. It is also used to home the sensor in a flatbed scanner or eject the image in a sheetfed scanner. **Note: Always make sure the Command Register is in the idle state (=0) before issuing a new command.**						0	0	0	Idle - Stops motor (A, B, $\overline{A}$, $\overline{B}$ = 0), completes current line of data (if scanning). Note: CCD/CIS clocks continue clocking.
							0	0	1	High Speed Forward - Moves motor forward at a speed determined by the Fast Feed Step Size (registers 48 and 49).
							0	1	0	High Speed Reverse - Moves motor backward at a speed determined by the Fast Feed Step Size (registers 48 and 49).
							0	1	1	Start Scan - Resets the LM9833's data pointers and starts an image scan.
							1	0	1	Programmed High Speed Forward - Moves motor forward at a speed determined by the Fast Feed Step Size (registers 48 and 49) for the number of lines programmed in registers 4A and 4B.
							1	1	0	Programmed High Speed Reverse - Moves motor backward at a speed determined by the Fast Feed Step Size (registers 48 and 49) for the number of lines programmed in registers 4A and 4B.
	Standby When this bit is set the entire chip enters a low power state. *Warning: A Standby command will stop DRAM refresh.*				0					Normal Operation.
					1					Low Power Standby Mode.
	Soft Reset Write a 1 then a 0 to reset the LM9833's state machines. *Warning: A Reset will stop DRAM refresh.*			0						Normal Operation.
				1						Resets the LM9833. See section **10.2 Soft Reset** for instructions on using this bit.
MASTER CLOCK DIVIDER										
08	**MCLK Divider** This register sets the master clock frequency for the entire scanner. f_{MCLK} = 48MHz/MCLK_Divider $f_{ADC} = f_{MCLK}/8$			0	0	0	0	0	0	÷1.0
				0	0	0	0	0	1	÷1.5
				0	0	0	1	1	0	÷4
				a	a	a	a	a	a	÷ ((aaaaaa/2)+1)
				1	1	1	1	1	0	÷32.0
				1	1	1	1	1	1	÷32.5

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
HORIZONTAL RESOLUTION AND DATAMODE SETTINGS										
09	**Horizontal DPI Divider** This register determines the horizontal resolution of the scan. Scan resolution = Optical resolution divided by the Horizontal_DPI_Divider.						0	0	0	÷1
							0	0	1	÷1.5
							0	1	0	÷2
							0	1	1	÷3
							1	0	0	÷4
							1	0	1	÷6
							1	1	0	÷8
							1	1	1	÷12
	Pixel Packing This register determines how many bits in each byte of data are transmitted to the host when DataMode = 0				0	0				1 bit/pixel (1 bit grayscale/3 bit color)
					0	1				2 bits/pixel (2 bit grayscale/6 bit color)
					1	0				4 bits/pixel (4 bit grayscale/12 bit color)
					1	1				8 bits/pixel (8 bit grayscale/24 bit color)
	DataMode When DataMode = 0, the pixel data is fully processed, going through the Offset, Shading, Horizontal DPI Adjust, Gamma, and Pixel Packing blocks. When DataMode = 1, 16 bit data is extracted following the Shading Multiplier stage. Gamma and any other post processing must be done by the host.			0						1, 2, 4, or 8 bit image data, as determined by the Pixel Size setting.
				1						16 bit image data - sent in 2 bytes, MSB first: 15 14 13 12 11 10 09 08 - 07 06 05 04 03 02 01 00
	Analog Bias Current (Percent of Nominal) The recommended setting is 80% for best performance. Lower settings will reduce power consumption further but may degrade ADC INL and DNL performance.	0	0							100% (analog supply current = ~81mA)
		0	1							80% (analog supply current = ~65mA)
		1	0							70% (analog supply current = ~57mA)
		1	1							50% (analog supply current = ~41mA)
TURBO AND PREVIEW MODE SETTINGS										
0A	Turbo/Preview Mode Select							0	0	Normal Operation
								0	1	Preview Mode (for CCD Sensors)
								1	0	Turbo Mode (for CIS Sensors)
								1	1	N/A
	Turbo/Preview Mode Speed					0	0			x2
						0	1			x3 (3 Channel Pixel Rate Mode Only)
						1	0			x4 (3 Channel Pixel Rate Mode Only)
						1	1			x6 (3 Channel Pixel Rate Mode Only)
SENSOR CONFIGURATION										
0B	**Input Signal Polarity**								0	Negative (Most CCD Sensors and Toshiba CIS)
									1	Positive (Most CIS Sensors)
	CDS On/Off							0		CDS Off
								1		CDS On
	Standard/Even-Odd Sensor						0			Standard (1 pixels per Ø period)
							1			Even/Odd (2 pixels per Ø period)
	CIS TR1 Timing Mode				0	0				Off - use standard CCD Timing
					0	1				CIS TR1 Timing Mode 1: TR1 pulse = exactly one Ø clock, starting at rising edge of Ø1
					1	0				CIS TR1 Timing Mode 2: TR1 pulse = exactly one Ø clock, TR1 centered around Ø1 high.
					1	1				N/A
	Fake Optical Black Pixels (for Dyna-type CIS sensors)			0						Off: Normal operation
				1						On: RS pulse held high for entire Optical Black period

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
SENSOR CONTROL SETTINGS										
0C	**Ø1 Polarity**								0	Positive
									1	Negative
	Ø2 Polarity							0		Positive
								1		Negative
	RS Polarity						0			Positive
							1			Negative
	CP1 Polarity					0				Positive
						1				Negative
	CP2 Polarity				0					Positive
					1					Negative
	TR1 Polarity			0						Positive
				1						Negative
	TR2 Polarity		0							Positive
			1							Negative
0D	**Ø1 Active/Off**								0	Off
									1	Active
	Ø2 Active/Off							0		Off
								1		Active
	RS Active/Off						0			Off
							1			Active
	CP1 Active/Off					0				Off
						1				Active
	CP2 Active/Off				0					Off
					1					Active
	TR1 Active/Off			0						Off
				1						Active
	TR2 Active/Off		0							Off
			1							Active
	Number of TR Pulses	0								1 TR Pulse
		1								2 TR Pulses
0E	**TR Pulse Duration**					n	n	n	n	n+1 pixel periods (1-16)
	TR-Ø1 Guardband Duration	n	n	n	n					n pixel periods (0-15)
0F	**Optical Black Clamp Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
10	**Optical Black Clamp End**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
11	**Reset Pulse Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
12	**Reset Pulse Stop**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
13	**CP1 Pulse Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
14	**CP1 Pulse Stop**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
15	**CP2 Pulse Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
16	**CP2 Pulse Stop**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
17	**Reference Sample Position**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
18	**Signal Sample Position**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
INTEGRATION TIME ADJUST										
19	**Integration Time Adjustment Function**		n	n	n	n	n	n	n	$t_{READOUT} = n*t_{INT}$, n = 1 to 127. n=0 turns off function.
STEPPER PHASE CORRECTION										
1A	**TR to Stepper Phase Correction - MSB**			n	n	n	n	n	n	First step of scan occurs n pixels (1 - 16383) after first TR pulse. This register can be used to set the phase between the TR pulses and the stepper motor pulses. NOTE: a setting of n = 0 creates the maximum delay (16384) pixels, which will increase scan time. If this function is not used, this register should be set to 1.
1B	**TR to Stepper Phase Correction - LSB**	n	n	n	n	n	n	n	n	

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
SENSOR PIXEL CONFIGURATION										
1C	**Optical Black Pixels Start**	n	n	n	n	n	n	n	n	n pixels (0 - 255)
1D	**Optical Black Pixels End**	n	n	n	n	n	n	n	n	n pixels (0 - 255)
1E	**Active Pixels Start - MSB**			n	n	n	n	n	n	n pixels (0 - 16383) Set to the same value as register **Data Pixels Start**.
1F	**Active Pixels Start - LSB**	n	n	n	n	n	n	n	n	
20	**Line End - MSB**			n	n	n	n	n	n	n pixels (0 - 16383) This selects the pixel count at which the current line is ended and the next line begins. This determines the integration time of one line.
21	**Line End - LSB**	n	n	n	n	n	n	n	n	
PIXEL DATA RANGE TO PROCESS										
22	**Data Pixels Start - MSB**			n	n	n	n	n	n	n pixels (**Active Pixels Start** - 16383) This selects the start of the range of pixels transmitted to the PC and determines the pixel location where offset and shading correction begins (pixel 0 in the DataPort). This value must be >= **Active Pixels Start**
23	**Data Pixels Start - LSB**	n	n	n	n	n	n	n	n	
24	**Data Pixels End - MSB**			n	n	n	n	n	n	n pixels (**Data Pixels Start** - [**Line End** - 20])
25	**Data Pixels End - LSB**	n	n	n	n	n	n	n	n	This selects the end of the range of pixels transmitted to the PC. This value must be <= [**Line End** - 20]
COLOR MODE SETTINGS										
26	**AFE Operation** 3 Channel or 1 Channel						0	0	0	3 Channel Pixel Rate Color
							0	0	1	3 Channel Line Rate Color
							1	0	0	1 Channel Grayscale
							1	0	1	1 Channel Color
	1 Channel Grayscale Input Source (1 Channel Color always uses the Blue Channel as the input)				0	0				Red Channel
					0	1				Green Channel
					1	0				Blue Channel
					1	1				N/A
	TR_{RED} (=TR1) position (3 Channel Line Rate Mode only)			0						1st TR pulse position (inside Ø1 high)
				1						2nd TR pulse position (inside Ø1 low)
	TR_{GREEN} (=TR2) position (3 Channel Line Rate Mode only)		0							1st TR pulse position (inside Ø1 high)
			1							2nd TR pulse position (inside Ø1 low)
	TR_{BLUE} (=CP2) position (3 Channel Line Rate Mode only)	0								1st TR pulse position (inside Ø1 high)
		1								2nd TR pulse position (inside Ø1 low)
27	**3 Channel Line Rate TR_{RED} drop** (3 Channel Line Rate Mode only)							0	0	Do not drop any TR_{RED} pulses
								0	1	Drop 1 TR_{RED} pulse (double integration time)
								1	0	Drop 2 TR_{RED} pulses (triple integration time)
								1	1	N/A
	3 Channel Line Rate TR_{GREEN} drop (3 Channel Line Rate Mode only)					0	0			Do not drop any TR_{GREEN} pulses
						0	1			Drop 1 TR_{GREEN} pulse (double integration time)
						1	0			Drop 2 TR_{GREEN} pulses (triple integration time)
						1	1			N/A
	3 Channel Line Rate TR_{BLUE} drop (3 Channel Line Rate Mode only)			0	0					Do not drop any TR_{BLUE} pulses
				0	1					Drop 1 TR_{BLUE} pulse (double integration time)
				1	0					Drop 2 TR_{BLUE} pulses (triple integration time)
				1	1					N/A
	Triple TR output		0							Normal operation
			1							Outputs single TR pulse on TR1, TR2, and CP2 pins
RESERVED										
28	Reserved	0	0	0	0	0	0	0	0	Write 00 to this register

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
ILLUMINATION SETTINGS										
29	**Illumination Mode** Controls the function of the 3 LAMP outputs: $LAMP_R$, $LAMP_G$, and $LAMP_B$ Mode 0 is the Off/Reset state. Mode 1 is typically used for CCFL lamps. Mode 2 is for color scanning with tri-color LEDs. Mode 3 is for grayscale scanning with tri-color LEDs.							0	0	$LAMP_R$ = $LAMP_G$ = $LAMP_B$ = 0V (Power-On/Reset Default)
								0	1	Illumination Mode 1 - $LAMP_R$ and $LAMP_B$ turn on every line, with their on and off points controlled by the Pixel Counter settings. $LAMP_G$ Output is continuous PWM pulse stream. (Figure 20) $LAMP_R$ and/or $LAMP_B$ may be set to stay on or off at all times by setting the LAMP Off or LAMP On settings (registers 2C-37) greater than the Line End value (registers 20 and 21).
								1	0	Illumination Mode 2 - $LAMP_R$, $LAMP_G$, $LAMP_B$ turn on sequentially at the line rate, with their on and off points controlled by Pixel Counter settings. (Figure 21)
								1	1	Illumination Mode 3 - $LAMP_R$, $LAMP_G$, $LAMP_B$ turn on every line, with their on and off points controlled by the Pixel Counter settings. (Figures 22 and 23)
	$LAMP_B$ for INT IME ADJ						0			$LAMP_B$ operates normally
							1			$LAMP_B$ output is enabled during short integration time, low during long integration time.
2A	**$LAMP_G$ PWM - MSB** (Illumination Mode 1)					n	n	n	n	$LAMP_G$ output is a PWM pulse stream. Duty cycle is n/4095. Frequency = 48Mhz/4096 = 11.7kHz
2B	**$LAMP_G$ PWM - LSB** (Illumination Mode 1)	n	n	n	n	n	n	n	n	
2C	**$LAMP_R$ On - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the $LAMP_R$ output goes high (if programmed)
2D	**$LAMP_R$ On - LSB**	n	n	n	n	n	n	n	n	
2E	**$LAMP_R$ Off - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the $LAMP_R$ output goes low (if programmed)
2F	**$LAMP_R$ Off - LSB**	n	n	n	n	n	n	n	n	
30	**$LAMP_G$ On - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the $LAMP_G$ output goes high (if programmed)
31	**$LAMP_G$ On - LSB**	n	n	n	n	n	n	n	n	
32	**$LAMP_G$ Off - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the $LAMP_G$ output goes low (if programmed)
33	**$LAMP_G$ Off - LSB**	n	n	n	n	n	n	n	n	
34	**$LAMP_B$ On - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the $LAMP_B$ output goes high (if programmed)
35	**$LAMP_B$ On - LSB**	n	n	n	n	n	n	n	n	
36	**$LAMP_B$ Off - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the $LAMP_B$ output goes low (if programmed)
37	**$LAMP_B$ Off - LSB**	n	n	n	n	n	n	n	n	
STATIC OFFSET AND GAIN SETTINGS FOR ANALOG FRONT END										
38	**Static Offset (Red)**			0	n	n	n	n	n	Offset = +n*9.3mV, n = 0 to 31
				1	n	n	n	n	n	Offset = -n*9.3mV, n = 0 to 31
39	**Static Offset (Green)**			0	n	n	n	n	n	Offset = +n*9.3mV, n = 0 to 31
				1	n	n	n	n	n	Offset = -n*9.3mV, n = 0 to 31
3A	**Static Offset (Blue)**			0	n	n	n	n	n	Offset = +n*9.3mV, n = 0 to 31
				1	n	n	n	n	n	Offset = -n*9.3mV, n = 0 to 31
3B	**Static Gain (Red)**			0	n	n	n	n	n	Gain = 0.93 + 0.067*n (V/V), n = 0 to 31
				1	n	n	n	n	n	Gain = 3(0.93 + 0.067*n) (V/V), n = 0 to 31
3C	**Static Gain (Green)**			0	n	n	n	n	n	Gain = 0.93 + 0.067*n (V/V), n = 0 to 31
				1	n	n	n	n	n	Gain = 3(0.93 + 0.067*n) (V/V), n = 0 to 31
3D	**Static Gain (Blue)**			0	n	n	n	n	n	Gain = 0.93 + 0.067*n (V/V), n = 0 to 31
				1	n	n	n	n	n	Gain = 3(0.93 + 0.067*n) (V/V), n = 0 to 31

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
DIGITAL PIXEL RATE OFFSET AND GAIN SETTINGS										
3E	**Fixed Offset Coefficient - MSB**	n	n	n	n	n	n	n	n	Fixed Offset to use for calibration
3F	**Fixed Offset Coefficient - LSB**	n	n	n	n	n	n	n	n	
40	**Fixed Multiplier Coefficient - MSB**	n	n	n	n	n	n	n	n	Fixed Gain to use for calibration
41	**Fixed Multiplier Coefficient - LSB**	n	n	n	n	n	n	n	n	
DIGITAL PIXEL RATE OFFSET AND GAIN/DRAM SETTINGS										
42	**Shading Multiplier**								0	Gain = [Multiplier Coefficent]/16384
									1	Bypass Multiplier
	Multiplier Coefficient Source							0		Configuration Register 40 and 41 (Fixed)
								1		External DRAM
	Offset Coefficient Source						0			Configuration Register 3E and 3F (Fixed)
							1			External DRAM
	Reserved			1	0					Set to 10
	DRAM Size		0							256k x 16
			1							1M x 16

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
STEPPER MOTOR CONTROL SETTINGS										
43	**n (Line Skipping)** Part of the "n out of m" function, consisting of registers 43, 44, and 54 (bits 3-7).	t	t	t	t	t	t	t	t	n lines saved in DRAM for every m lines (register 44) scanned, function bypassed if register value = 0. n (lines saved per m lines scanned) = 256 - t t = 256 - n If t = 0 then function is bypassed.
44	**m (Line Skipping)** Part of the "n out of m" function, consisting of registers 43, 44, and 54 (bits 3-7).	m	m	m	m	m	m	m	m	n lines (register 43) saved in DRAM for every m lines scanned. m = 1 to 255. If m = 0 then function is bypassed.
45	**Full/Microstepping**								0	Full Step Mode
									1	Microstepping Mode
	Current Sensing Phases = 0 for fullstepping							0		1 Phase - No microstepping, just kickstart/stop functions
	= 1 for microstepping							1		2 Phases - necessary for microstepping
	Stepper Motor Phase A Polarity						0			Positive (A/B/$\overline{A}$/$\overline{B}$ Output high = winding energized)
							1			Negative (A/B/$\overline{A}$/$\overline{B}$ output low = winding energized) WARNING: When idle, this setting leaves the motor energized for unipolar motors, and will destroy bipolar motor drivers. Keep this bit set to a 0.
	Stepper Motor Phase B Polarity					0				Positive (A/B/$\overline{A}$/$\overline{B}$ Output high = winding energized)
						1				Negative (A/B/$\overline{A}$/$\overline{B}$ output low = winding energized) WARNING: When idle, this setting leaves the motor energized for unipolar motors, and will destroy bipolar motor drivers. Keep this bit set to a 0.
	A, B, $\overline{A}$, and $\overline{B}$ stepper motor status				**0**					A, B, $\overline{A}$, and $\overline{B}$ output pins in Tri-State
					1					A, B, $\overline{A}$, and $\overline{B}$ output pins active
	Swap A/$\overline{A}$ with B/$\overline{B}$ (Reverses motor direction)			0						Default polarity
				1						Reverse Polarity
	Fullstep During FastFeed at Start of Scan		0							Traditional Operation
			1							Fullstep during fastfeed at start of scan
46	**Scanning Step Size - MSB**	n	n	n	n	n	n	n	n	The step size of one microstep while scanning, in units of pixel periods (minimum 2)
47	**Scanning Step Size - LSB**	n	n	n	n	n	n	n	n	
48	**Fast Feed Step Size - MSB**			n	n	n	n	n	n	The step size of one microstep while fast feeding, in units of pixel periods (minimum 2)
49	**Fast Feed Step Size - LSB**	n	n	n	n	n	n	n	n	
4A	**Fullsteps to Skip at Start of Scan - MSB**		n	n	n	n	n	n	n	When scan starts, paper is fed forward n full steps (0 - 32767) at highest speed. For "zooming" in flatbeds
4B	**Fullsteps to Skip at Start of Scan - LSB**	n	n	n	n	n	n	n	n	
4C	**Step Counter - MSB**			n	n	n	n	n	n	Counts n (0-16383) full steps. See register 58, bit 5 for more information.
4D	**Step Counter - LSB**	n	n	n	n	n	n	n	n	
4E	**Pause scanning, stop/reverse motor**	n	n	n	n	n	n	n	n	Pause scan when buffer is n*2 (16 x 256k) or n*8 (16x1M) kbytes full
4F	**Resume scanning, start motor**	n	n	n	n	n	n	n	n	Resume scan when buffer is n*2 (16 x 256k) or n*8 (16x1M) kbytes full
50	**Full steps to reverse when buffer is full**	n	n	n	n	n	n	n	n	n (0-255) full steps (0 = do not reverse)
51	**Acceleration Profile (stopped)**					n	n			n (0,1, 2, or 8) full step time units pause while stopped
	Acceleration Profile (25%)			n	n					n (0,1, 2, or 8) full steps at 25% speed
	Acceleration Profile (50%)	n	n							n (0,1, 2, or 8) full steps at 50% speed
	Default Phase Difference - High Byte							n	n	18 bit word used to calculate when motor resumes after reversing and stopping. 1 < n < 262143. 2 bits in register 51 are the most significant bits of 18 bit word.
52	**Default Phase Difference - Mid Byte**	n	n	n	n	n	n	n	n	
53	**Default Phase Difference - Low Byte**	n	n	n	n	n	n	n	n	
54	**Lines to Process After Pause/ Lines to Discard after Resume**						n	n	n	n (0-7) lines. This only applies if the motor doesn't reverse (reverse steps = 0)
	Line Skipping Phase Part of the "n out of m" function, consisting of registers 43, 44, and 54 (bits 3-7).					0				Red sensor data arrives before Green sensor
						1				Blue sensor data arrives before Green sensor
	Line Skipping Color Phase Delay Part of the "n out of m" function, consisting of registers 43, 44, and 54 (bits 3-7).	n	n	n	n					n lines, n = 0-15

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
55	**Kickstart steps** (fullstepping mode)						n	n	n	Motor gets maximum current for first n (0-7) full steps
	Hold Current Timeout	n	n	n	n	n				Full step time units (1-31) (do not set to 0)
56	**Stepper Motor PWM Frequency**	n	n	n	n	n	n	n	n	=CRYSTAL OUT/(256*n) (0 < n < 256) =CRYSTAL OUT/(256*256) (n = 0)
57	**Stepper Motor PWM Set Duty Cycle**			n	n	n	n	n	n	= minimum of n/64 (default = 0)
PAPER SENSE SETTINGS										
58	**PAPER SENSE 1: Polarity**								0	A low input on PAPER SENSE 1 is True
									1	A high input on PAPER SENSE 1 is True
	PAPER SENSE 1: Level/Edge sensitive							0		Level sensitive: PAPER SENSE 1 State bit (in Status Register) is set to a 1 if PAPER SENSE 1 is currently True.
								1		Edge sensitive: PAPER SENSE 1 State bit (in Status Register) is set to a 1 if PAPER SENSE 1 has been True since the last time the Status Register was read.
	PAPER SENSE 1: Stop Scan, High Speed Forward, and High Speed Reverse Use this input for the home sensor in flatbed scanners.						0			Transitions on PAPER SENSE 1 will not clear the command register.
							1			A False-to-True transition on PAPER SENSE 1 will clear the Command Register and stop the scan.
	PAPER SENSE 2: Polarity					0				A low input on PAPER SENSE 2 is True
						1				A high input on PAPER SENSE 2 is True
	PAPER SENSE 2: Level/Edge sensitive				0					Level sensitive: PAPER SENSE 2 State bit (in Status Register) is set to a 1 if PAPER SENSE 2 is currently True.
					1					Edge sensitive: PAPER SENSE 2 State bit (in Status Register) is set to a 1 if PAPER SENSE 2 has been True since the last time the Status Register was read.
	PAPER SENSE 2: Stop Scan and High Speed Forward			0						The scan will automatically stop after scanning for the number of fullsteps specified in the **Step Counter** (registers 4C and 4D). (The fullsteps moved during the "FastFeed At Start of scan period are not counted.) If the value in the **Step Counter** is 0, the scan can only be stopped by writing a 0 to register 07.
				1						A False-to-True transition on PAPER SENSE 2 will stop a scan or a High Speed Forward command after the number of fullsteps specified in the **Step Counter** (registers 4C and 4D). It will not stop a High Speed Reverse, and therefore should not be used as a home position sensor input.

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
MISC I/O PIN SETTINGS										
59	**MISC I/O 1: Input or Output**								0	The MISC I/O 1 pin is configured as an input.
									1	The MISC I/O 1 pin is configured as an output.
	MISC I/O 1: Polarity (if configured as an input)							0		A low input on MISC I/O 1 is True
								1		A high input on MISC I/O 1 is True
	MISC I/O 1: Level/Edge sensitive (if configured as an input)						0			Level sensitive: MISC I/O 1 State bit (in Status Register) is set to a 1 if MISC I/O 1 is currently True.
							1			Edge sensitive: MISC I/O 1 State bit (in Status Register) is set to a 1 if MISC I/O 1 has been True since the last time the Status Register was read.
	MISC I/O 1: Output State (if configured as an output) ***Power On/USB Suspend Default: Input***					0				The output of the MISC I/O 1 pin will be a logic low (0V).
						1				The output of the MISC I/O 1 pin will be a logic high (5V).
	MISC I/O 2: Input or Output				0					The MISC I/O 2 pin is configured as an input.
					1					The MISC I/O 2 pin is configured as an output.
	MISC I/O 2: Polarity (if configured as an input)			0						A low input on MISC I/O 2 is True
				1						A high input on MISC I/O 2 is True
	MISC I/O 2: Level/Edge sensitive (if configured as an input)		0							Level sensitive: MISC I/O 2 State bit (in Status Register) is set to a 1 if MISC I/O 2 is currently True.
			1							Edge sensitive: MISC I/O 2 State bit (in Status Register) is set to a 1 if MISC I/O 2 has been True since the last time the Status Register was read.
	MISC I/O 2: Output State (if configured as an output) ***Power On/USB Suspend Default: Input***	0								The output of the MISC I/O 2 pin will be a logic low (0V).
		1								The output of the MISC I/O 2 pin will be a logic high (5V).
5A ***(NEW)***	MISC I/O 3: Input or Output								0	The MISC I/O 3 pin is configured as an input.
									1	The MISC I/O 3 pin is configured as an output.
	MISC I/O 3: Polarity (if configured as an input)							0		A low input on MISC I/O 3 is True
								1		A high input on MISC I/O 3 is True
	MISC I/O 3: Level/Edge sensitive (if configured as an input)						0			Level sensitive: MISC I/O 3 State bit (in Status Register) is set to a 1 if MISC I/O 3 is currently True.
							1			Edge sensitive: MISC I/O 3 State bit (in Status Register) is set to a 1 if MISC I/O 3 has been True since the last time the Status Register was read.
	MISC I/O 3: Output State (if configured as an output) ***Power On/USB Suspend Default: Input***					0				The output of the MISC I/O 3 pin will be a logic low (0V).
						1				The output of the MISC I/O 3 pin will be a logic high (5V).
	MISC I/O 4: Input or Output				0					The MISC I/O 4 pin is configured as an input.
					1					The MISC I/O 4 pin is configured as an output.
	MISC I/O 4: Polarity (if configured as an input)			0						A low input on MISC I/O 4 is True
				1						A high input on MISC I/O 4 is True
	MISC I/O 4: Level/Edge sensitive (if configured as an input)		0							Level sensitive: MISC I/O 4 State bit (in Status Register) is set to a 1 if MISC I/O 4 is currently True.
			1							Edge sensitive: MISC I/O 4 State bit (in Status Register) is set to a 1 if MISC I/O 4 has been True since the last time the Status Register was read.
	MISC I/O 4: Output State (if configured as an output) ***Power On/USB Suspend Default: Output, Logic High***	0								The output of the MISC I/O 4 pin will be a logic low (0V).
		1								The output of the MISC I/O 4 pin will be a logic high (5V).

Register Listing (Continued)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
5B *(NEW)*	MISC I/O 5: Input or Output								0	The MISC I/O 5 pin is configured as an input.
									1	The MISC I/O 5 pin is configured as an output.
	MISC I/O 5: Polarity (if configured as an input)							0		A low input on MISC I/O 5 is True
								1		A high input on MISC I/O 5 is True
	MISC I/O 5: Level/Edge sensitive (if configured as an input)						0			Level sensitive: MISC I/O 5 State bit (in Status Register) is set to a 1 if MISC I/O 5 is currently True.
							1			Edge sensitive: MISC I/O 5 State bit (in Status Register) is set to a 1 if MISC I/O 5 has been True since the last time the Status Register was read.
	MISC I/O 5: Output State (if configured as an output)					0				The output of the MISC I/O 5 pin will be a logic low (0V).
	Power On/USB Suspend Default: Output, Logic High					1				The output of the MISC I/O 5 pin will be a logic high (5V).
	MISC I/O 6: Input or Output				0					The MISC I/O 6 pin is configured as an input.
					1					The MISC I/O 6 pin is configured as an output.
	MISC I/O 6: Polarity (if configured as an input)			0						A low input on MISC I/O 6 is True
				1						A high input on MISC I/O 6 is True
	MISC I/O 6: Level/Edge sensitive (if configured as an input)		0							Level sensitive: MISC I/O 6 State bit (in Status Register) is set to a 1 if MISC I/O 6 is currently True.
			1							Edge sensitive: MISC I/O 6 State bit (in Status Register) is set to a 1 if MISC I/O 6 has been True since the last time the Status Register was read.
	MISC I/O 6: Output State (if configured as an output)	0								The output of the MISC I/O 6 pin will be a logic low (0V).
	Power On/USB Suspend Default: Output, Logic Low	1								The output of the MISC I/O 6 pin will be a logic high (5V).
TEST MODE SETTINGS										
5C	**ADC Output Code - MSB**	n	n	n	n	n	n	n	n	Used to force the input to the HDPI Divider to a known value for digital tests
5D	**ADC Output Code - LSB**	n	n	n	n	n	n	n	n	
5E	**ADC Test Mode**							0	0	Normal Operation
								0	1	Bypass AFE, Normal ADC Operation
								1	0	Bypass AFE, bypass ADC digital correction, output uncorrected ADC MSB
								1	1	Bypass AFE, bypass ADC digital correction, output uncorrected ADC LSB
	Pixel Processing Input Select					0	0			Normal Operation - ADC Output
						0	1			Registers 5C and 5D
						1	0			16 bit counter, reset at the start of every scan
						1	1			16 bit counter, reset at the start of every line
	16 bit Counter Increment Select (16 bit counter starts at 0, increments every datapixel)			0	0					Increments by 1
				0	1					Increments by 4
				1	0					Increments by 16
				1	1					N/A
	MCLK edge for AFE (Set this bit to 0)		0							Rising
			1							Falling
	CDS Signal	0								Normal Operation
		1								CDS signal is output on $LAMP_B$ pin
5F-68	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to these registers
69	**Version Number**						1	0	0	100 = LM9832 or LM9833 (011 = LM9831, 010 = LM9830)
6A-7F	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to these registers

Applications Information

1.0 OVERVIEW

The LM9833 is a USB, 1200dpi, 16 bit (48 bit color) scanner-on-a-chip. The LM9833 is an improved, 16 bit version of the LM9831, providing all of the LM9831's functionality while improving performance and adding several new features. See **12.0 CHANGES FROM THE LM9831** for a complete list of additions and enhancements.

2.0 ANALOG SIGNAL PROCESSING

One channel of the LM9833's analog front end is shown in Figure 3. The gain through each channel can be set between 0.93V/V and 9.0V/V using registers 3B, 3C, and 3D. The offset DAC provides up to ±278mV of offset correction using registers 38, 39, and 3A. The offset DAC and gain stages should be adjusted during coarse calibration so that the input signal is a maximum of 1.9Vp-p at the ADC input.

3.0 DIGITAL SIGNAL PROCESSING

3.1 ADC

The digital pixel data comes from a 6MHz 16 bit pipelined ADC.

3.2 Pixel Processing Block

The Pixel Processing stage is used to digitally reduce the optical resolution of the sensor. The optical resolution can be reduced by a factor of 1, 1.5, 2, 3, 4, 6, 8, or 12. For a 1200 dpi (optical) system, this would produce resolutions of 1200, 800, 600, 400, 300, 200, 150, and 100. A 600 dpi (optical) system would be capable of 600, 400, 300, 200, 150, 100, 75, and 50 dpi. (Resolution in the vertical direction is controlled by the stepper motor speed.)

Horizontal resolution reduction is accomplished by averaging adjacent pixels. Averaging produces better image quality and reduces aliasing versus the traditional technique of simply discarding pixels to reduce resolution. For example, to get 100 dpi from a 300dpi optical sensor, you would average 3 300dpi pixels:

$$pixel_{100dpi} = \frac{p_{n-2} + p_{n-1} + p_n}{3}$$

The number of pixels coming out of the Pixel Processing block is equal to the integer portion of the number of pixels going in to the Pixel Processing block divided by the "Divide By" setting, from the table shown in Figure 4.

$$Pixels_{OUT} = INT\left(\frac{Pixels_{IN}}{Divide\ By}\right)$$

This equation also applies to the divide by 1.5 function.

Divide By	DPI (1200 DPI system)	DPI (800 DPI system)	DPI (600 DPI system)	DPI (300 DPI system)
1	1200	800	600	300
1.5	800	533	400	200
2	600	400	300	150
3	400	267	200	100
4	300	200	150	75
6	200	133	100	50
8	150	100	75	37.5
12	100	67	50	25

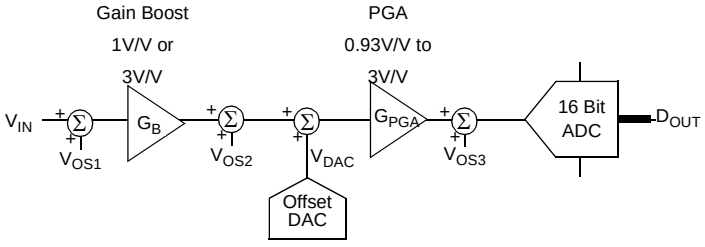
Figure 4: Decreasing Horizontal Resolution

If there are not enough pixels at the end of a line to form a complete pixel, the last pixel will be eliminated. For example, if a line is 35 pixels wide and the Horizontal DPI setting is set to divide by 6, then the output of the Pixel Processing block will be 5 pixels (the integer portion of 35/6). The last 5 pixels will be discarded, since 6 pixels would be required to form a new pixel in this mode.

The output of this stage is sent to the Pixel Rate Offset Correction Block.

3.3 Pixel Rate Offset Correction Block

Offset correction words for every pixel of the CCD are stored in



$$D_{OUT} = (((V_{IN} + V_{OS1})G_B + V_{DAC} + V_{OS2})G_{PGA} + V_{OS3})C$$

simplified, with all offsets = 0, this is:

$$D_{OUT} = (V_{IN}G_B + V_{DAC})G_{PGA}C$$

C is a constant that combines the gain error through the AFE, reference voltage variance, and analog voltage to digital code conversion into one constant. Ideally, C = 32768 codes/V.

Manufacturing tolerances widen the range of C. See Electrical Specifications.

Figure 3: Analog Front End (AFE) Model

Applications Information (Continued)

the external DRAM and accessed at the pixel rate. A digital subtractor subtracts the 16 bit offset word (corresponding to that pixel's offset error) from each pixel.

The subtractor saturates at 0, i.e. if the coefficient to be subtracted is greater than the ADC output code, the result is an output of 0.

The offset words stored in DRAM are typically calculated by scanning a black calibration strip at 16 bits, and storing the results in the DRAM using the DataPort.

The offset correction equation is:

$$Pixel_{OUT} = Pixel_{IN} - coefficient$$

3.4 Pixel Rate Gain Correction Block

This is a digital multiplier that multiplies the output word from the subtractor by a 16 bit digital correction coefficient corresponding to that pixel's gain error. The coefficients are stored in the external RAM and accessed at the pixel rate.

The multiplier saturates at 65535, i.e. if the result of the multiplication is greater than 65535, the multiplier output is 65535.

The gain equation is:

$$Pixel_{OUT} = Pixel_{IN} \cdot \frac{coefficient}{16384}$$

Note that a coefficient of 0 represents a gain of 0. On the LM9830 and previous parts, a coefficient of 0 represented a gain of 1. To achieve a gain of 1, the coefficient should be set to 16384.

3.5 Gamma Correction Tables

There are 3 gamma lookup tables for R, G, and B. The input to the table is the 12 MSBs (most significant bits) of the 16 bit pixel data coming from the previous stage (**3.4 Pixel Rate Gain Correction Block**). The output is the 8 bit gamma corrected pixel data. The tables consume 12k words (4K bytes x 16 bits, only the 8 LSBs of each word is used) of the external DRAM. Each gamma table (red, green, and blue) can be loaded with any arbitrary user-defined transfer curve.

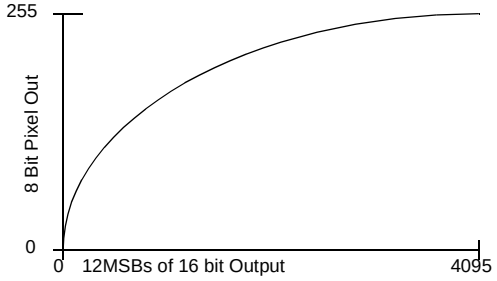


Figure 5: Gamma Table

The gamma tables are loaded through the dataport (see **6.1 The DataPort: Reading and Writing to Gamma, Offset, and Gain Memory**). The DataPort selects which color (Red, Green or Blue) gamma table will be read from or written to.

3.6 Pixel Packing/Thresholding Block

Some scans require only one bit per pixel ("line art" mode), others may need only 2 or 4 bits/pixel. To increase scanning speed for lower pixel depths, the LM9833 packs the desired MSBs of multiple pixels together into 1 16 bit word, increasing the transmission speed to the host by a factor of 2, 4, 8, or 16. Figure 6 shows how the pixels are packed together for 8, 4, 2, and 1 bit pixel depths. In Figure 6, "b" indicates the bit position (b7 = the most significant and b0 = the least significant bit) of the original 8 bit pixel data, and p_n indicates the original pixel sequence, i.e p_0, p_1, p_2, p_3...

If there are not enough unpacked pixels at the end of a line to complete the packed word for transmission, that final word is not sent. For example, doing an 8 bit pixel rate scan with a HDPI divider of 1 and an odd number of pixels will truncate the blue component of the last pixel.

Pixel Depth	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
8	b7 p_0	b6 p_0	b5 p_0	b4 p_0	b3 p_0	b2 p_0	b1 p_0	b0 p_0
4	b7 p_0	b6 p_0	b5 p_0	b4 p_0	b7 p_1	b6 p_1	b5 p_1	b4 p_1
2	b7 p_0	b6 p_0	b7 p_1	b6 p_1	b7 p_2	b6 p_2	b7 p_3	b6 p_3
1	b7 p_0	b7 p_1	b7 p_2	b7 p_3	b7 p_4	b7 p_5	b7 p_6	b7 p_7
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
8	b7 p_1	b6 p_1	b5 p_1	b4 p_1	b3 p_1	b2 p_1	b1 p_1	b0 p_1
4	b7 p_2	b6 p_2	b5 p_2	b4 p_2	b7 p_3	b6 p_3	b5 p_3	b4 p_3
2	b7 p_4	b6 p_4	b7 p_5	b6 p_5	b7 p_6	b6 p_6	b7 p_7	b6 p_7
1	b7 p_8	b7 p_9	b7 p_{10}	b7 p_{11}	b7 p_{12}	b7 p_{13}	b7 p_{14}	b7 p_{15}

Figure 6: Packing Multiple Pixels Into One Word

The gamma table in **3.5 Gamma Correction Tables** allows the user to set the threshold of each transition for various line art or reduced pixel depth modes.

3.7 16 Bit Output Mode

The LM9833 also supports a 16 bit out mode. This can be used to get very accurate data for calibration or to scan a 16 gray/48 bit color image. This mode is set through register 9, bit 5. In the 16 bit output mode, the gamma and pixel packing stages are bypassed, and the 16 bit data from the ADC is stored in DRAM, formatted as shown in Figure 7.

MSB	15	14	13	12	11	10	9	8
	b15	b14	b13	b12	b11	b10	b9	b8
LSB	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	b7	b6	b5	b4	b3	b2	b1	b0

Figure 7: 16 Bit Output Mode Data Format

The memory reserved for the gamma table is used to store image data in the 16 bit mode. After scanning in 16 bit mode, the gamma table must be reloaded for operation in 8, 4, 2, or 1 bit mode.

3.8 Line Buffer

The line buffer uses the external DRAM as a FIFO line buffer to store the pixel data (which is generated at a fixed rate, synchronous to the CCD clocks) and send it back to the PC at an asynchronous, unpredictable, and non-constant rate.

The LM9833 supports 2 sizes of DRAM, 256k x 16bit and 1M x 16bit. 216kbytes (108kwords) of the capacity of the DRAM is con-

Applications Information (Continued)

sumed by the offset and shading coefficients and the gamma tables. That leaves 296kbytes of memory available for line buffer when using a 256k x 16 bit DRAM, or 1832kbytes of memory when using a 1M x 16 bit DRAM.

The line buffer is tightly coupled to the stepper motor (**4.0 Stepper Motor Controller**), and is responsible for stopping the motor before the buffer overflows and starting the motor again as the buffer nears empty.

If the scanner is generating pixel data faster than the PC can acquire it, the line buffer will start to fill up. As the buffer nears 100% of its capacity, the scan must be paused before it starts acquiring a line which will overflow the buffer. This Pause Threshold limit (register 4E) is programmable in 2 kbyte (256k x 16 bit DRAM) or 8kbyte (1M x 16 bit DRAM) increments between 0 and 255.

To maximize scanner performance and minimize pausing due to buffer full conditions, the pause threshold should be set using this formula:

Pause Threshold (kB) = Available_Memory - (Line_Length + 1)

where Available_Memory = 296kbytes (256k x 16b DRAM) or 1832kbytes (1M x 16 bit DRAM),

Line_Length = (Bytes/Line)/1024

$$\text{Bytes/Line} = 2 \cdot \text{INT}\left(\frac{\text{INT}\left(\frac{\text{Data Pixels}}{\text{HDPI\_Divider}}\right) \cdot C \cdot B}{16}\right)$$

Where C = 1 for “1 Channel Grayscale”, 3 for all other modes,

Data_Pixels = Data Pixels End (registers 24, 25) - Data Pixels Start (registers 22, 23)

HDPI_Divider = Horizontal DPI divider = 1, 1.5, 2, 3, 4, 6, 8, or 12

B = Bits per Pixel = 16 (16 bit mode), 8, 4, 2, or 1

Register 4E value = Pause Threshold (kB)/2 (256k x 16 DRAM) or Pause Threshold (kB)/8 (1M x 16 DRAM)

When the Pause Threshold is reached the buffer sends a command to the stepper motor controller to stop scanning. The remainder of the line being processed will continue being processed and be sent to the buffer. If the Lines To Process After Pause Scan Signal register (register 54) is greater than 0, then room for these additional lines needs to be added into the Pause Threshold value calculation.

Note that the scanner software on the host PC must set a Pause Threshold value low enough to ensure that any data that comes after a pause request (the rest of the current line and any subsequent lines if register 54 bits 0-2 are greater than 0) will fit into the DRAM buffer. If the Pause Threshold is set too high, the Line Buffer may overflow, creating discontinuities in the scanned image.

After a pause, the buffer will continue to transmit data to the PC until it hits the Resume Threshold limit (register 4F), which is also programmable in 2 kbyte (256k x 16 bit DRAM) or 8kbyte (1M x 16 bit DRAM) increments between 0 and 255. When the Resume Threshold is reached, the Line Buffer sends the motor controller a command to resume.

4.0 Stepper Motor Controller

The stepper motor controller sends a series of pulses to the stepper motor to move the paper past the sensor (sheetfed) or the sensor past the paper (flatbed). The speed at which the paper moves relative to the sensor, combined with the integration time of the image sensor, determines the effective vertical resolution (Lines Per Inch, or LPI).

The stepper motor is moved forwards and backwards by two signals, A and B, 90° out of phase with each other. The phase for the forward direction is set in Configuration Register 45.

The A and B signals are either squarewaves (in Full Step Mode, Figure 8), or a staircase approximation of a sine wave (in Microstep mode, Figures 10 and 11).

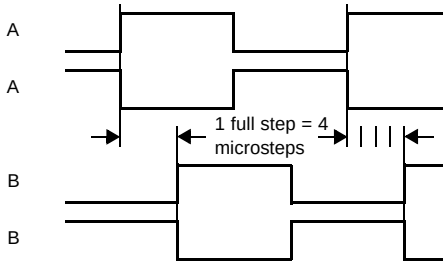


Figure 8: Stepper Motor Waveform - Full Stepping

The LM9833 always counts stepper motor steps in units of microsteps. A full step is equal to four microsteps. Even when the LM9833 is in Full Step Mode, it is counting in microsteps, and will increment the stepper motor (generating a full step) every four microsteps.

The microstep Step Size is defined in units of time. These units of time are pixel periods, as defined in the horizontal pixel counter. In the 3 Channel Pixel Rate input mode, the pixel period is the $f_{ADC}/3$ (= $f_{MCLK}/24$). In the 3 Channel Line Rate and 1 channel modes, the pixel period is equal to f_{ADC} (= $f_{MCLK}/8$). The Step Size is stored in the **Scanning Step Size** configuration register as a 14 bit value. During normal operation, the stepper motor is advanced 1 microstep every Step Size pixel periods. The LPI can be calculated as follows:

$$\text{LPI} = 4\text{FSPI}\frac{\text{StepSize}}{\text{pixels/line} \cdot X}$$

Where FSPI = the number of full steps required to move the image one inch, pixels/line is the number of pixel periods it takes to scan one horizontal line (equivalent to the value stored in the **Line End** registers), StepSize is the number of pixel periods/microstep, and X = 3 for line rate and 1 for pixel rate modes.

Whenever the stepper motor has been moving and then comes to a stop, the LM9833 waits for the time specified in the Hold Current Timeout register and then de-asserts the A, B, $\overline{A}$, and $\overline{B}$ outputs to cut power to the motor. When the stepper motor is not scanning or fast-feeding (Command = 00), A, B, $\overline{A}$, and $\overline{B}$ are de-asserted in all stepper modes.

There are two modes of stepper motor operation: fullstepping and microstepping.

4.1 Full Step Mode

In Full Step Mode the output is a pulse stream, as shown in Figure 8. The amplitude of the pulses is controlled by the output of

Applications Information (Continued)

the 2 bit DAC, shown in Figure 9.

Scan Mode	DAC Voltage
Starting from a dead stop	0.484V for number of steps specified in Kickstart Steps register (0-7). If register is 0 there is no Kickstart current-movement begins at 0.347V.
Scanning	0.347V
Stopped	0.133V for number of steps specified in Hold Current Timeout register (1 - 31), 0V after time out.

Figure 9: Full Step Current Control

4.2 Microstep Mode

Microstepping is a technique of driving the stepper motor with a staircase approximation of a sine wave, as shown in Figure 10. This technique maximizes the torque of a given motor, resulting in a higher maximum speed. In addition, it increases the resolution of the stepper motor. If a stepper motor moves 3.6° per full step, microstepping can create positions inside the 3.6°: 1.8°, 0.9°, or 0.45°, for example. This increases the maximum vertical resolution of the scanner. Microstepping also results in quieter motor movement.

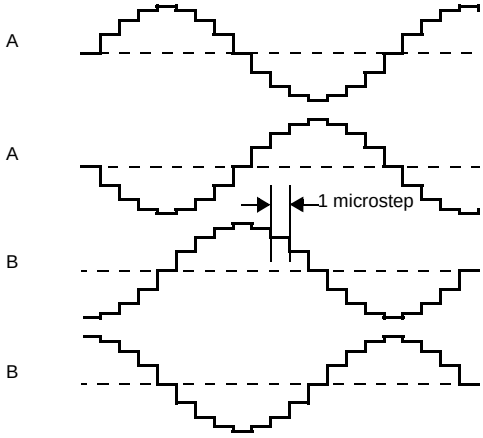


Figure 10: Bipolar Microstepping Waveform

The amplitude of the microstepped sine wave is controlled by the output of the stepper motor DAC (Figure 11). The current in the stepper motor winding is measured as a voltage across the sense resistor, and the transistor drive signals are pulse width modulated (PWM) to force the average current through the winding equal to V_{DAC}/R_{SENSE}. Register 56 controls the frequency of the PWM, and Register 57 controls the minimum time the driver is on every period. Register 57 should be set as short as possible, the driver only needs to be on long enough to mask any transient noise generated by the driver transistor turning on.

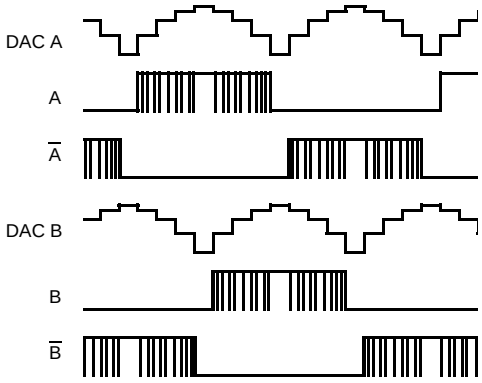


Figure 11: Stepper Motor Waveform - LM9833 Signals

Figure 12 shows the LM9833's DAC voltages. The peak current through the stepper motor winding will be $0.484V/R_{SENSE}$. The table index is incremented every microstep (StepSize pixel periods).

Table Index	A (B)	$\overline{A}$ ($\overline{B}$)	DAC Voltage
0	0	0	N/A
1	1	0	0.195V
2	1	0	0.347V
3	1	0	0.448V
4	1	0	0.484V
-0	0	0	N/A
-1	0	1	0.195V
-2	0	1	0.347V
-3	0	1	0.448V
-4	0	1	0.484V

Figure 12: Microstepping Current Control

4.3 Pause Behavior - Non-Reversing Mode

When the **Full Steps to Reverse When Buffer is Full** register is 0, the stepper motor simply stops moving when the Pause signal is received, as shown in Figure 13. The line of data currently being processed (section "a" in Figure 13) will continue to be processed and stored in DRAM. Additional lines may be digitized and stored as well, depending on the number programmed in the **Lines to Process After Pause Scan Signal** register (Figure 14). This value is different for different scanner designs and should be empirically set to the value that minimizes the spatial distortion created by the motor slowing down and stopping.

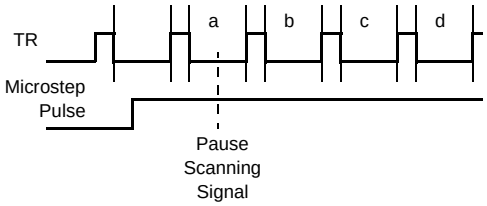


Figure 13: Stepper Motor Stopping

Applications Information (Continued)

Value	Additional Lines to Store in DRAM
0	0(a only)
1	1 (a and b)
2	2 (a, b and c)
...	...
7	7

Figure 14: Lines to Process after Pause Scan Signal Register

When the Resume Scan signal is received, the stepper motor controller waits the appropriate number of pixel periods after the next TR pulse and then starts stepping again at the normal rate. The first new line transmitted is determined by the **Lines to Discard After Resume Scan Signal** register. The discard value must be the same as the value in the **Lines to Process After Pause Scan Signal** register.

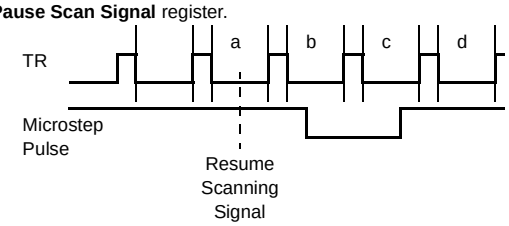


Figure 16: Stepper Motor Resuming

Value	First Line to Transmit After Pause
0	b
1	c
2	d
...	...
7	i

Figure 15: Lines to Discard After Resume Scan Signal Register

4.4 Pause Behavior - Reversing Mode

If the **Full Steps to Reverse When Buffer is Full** register is >0, then the Reversing Mode is enabled.

The Reversing Mode eliminates spatial distortion due to the pausing of a scan. When the Pause Scan signal is received, the line currently being processed is completed and stored in RAM (line “b” in Figure 17). When the scan resumes, ideally the LM9833 would send out lines “c” and after under the exact same speed and positional conditions the scanner was in before the scan paused (as indicated by the dotted line in Figure 17).

When the Pause Scan signal is received, the LM9833 processes the remainder of the line currently being read from the CCD (line b), and stores the offset (in pixel periods) between the last TR pulse and the last step. It then stops, reverses, stops, and waits for the Resume Scan signal. Once Resume Scan is asserted, the motor controller waits for the previously stored number of pixels periods, then starts moving forward again, maintaining the same phase relationship between the TR pulse and the stepper motor control signals. The result is as if the stepper motor had never paused.

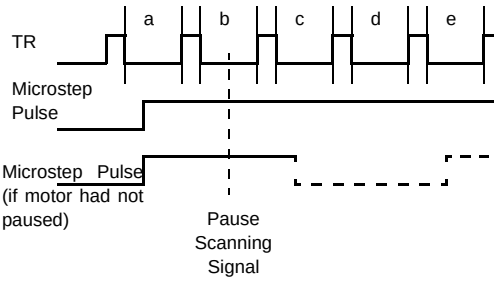


Figure 17: Reversing - The Goal

Stopping, reversing, and resuming forward motion all follow the curve programmed in the **Acceleration Profile** configuration register. There are 3 segments (Stopped, 25%, and 50%), and the number in each register indicates the number of full steps to stay at that acceleration. A value of 0 indicates that that segment is to be skipped. For example, a value of 0 in all three registers would mean that the motor would instantly reverse when the buffer is full, then instantly stop after going back the specified number of lines.

Speed Register	DAC output
Stopped (x = 0 to 3)	x = number of full step clocks to wait before reversing motor.
25% (y = 0 to 3)	y = number of full steps at 25% of final speed. Full step period = 4 full step clocks.
50% (z = 0 to 3)	z = number of full steps at 50% of final speed. Full step period = 2 full step clocks.

Figure 18: Acceleration Profile Settings

This acceleration profile is used any time the motor is started, stopped, or reversed.

The acceleration profile for stopping, reversing, stopping, and going forward again is this:

- Full speed forward (1 microstep = #pixels in **Scanning Step Size** register) until the Pause Scanning signal is received.
- 50% speed forward for z full steps (1 microstep = 2* #pixels in **Fast Feed Step Size** register)
- 25% speed forward for y full steps (1 microstep = 4*#pixels in **Fast Feed Step Size** register)
- Stopped for x full steps (1 microstep = #pixels in **Fast Feed Step Size** register).
- 25% speed backward for y full steps (1 microstep = 4*#pixels in **Fast Feed Step Size** register)
- 50% speed backward for z full steps (1 microstep = 2* #pixels in **Fast Feed Step Size** register)
- Full speed backward (1 microstep = #pixels in **Fast Feed Step Size** register) for number of microsteps in the **Steps to Reverse** register
- 50% speed backward for z full steps (1 microstep = 2* #pixels in **Fast Feed Step Size** register)
- 25% speed backward for y full steps (1 microstep = 4*#pixels in

Applications Information (Continued)

Fast Feed Step Size register)

- Paused until a Resume Scan signal is received, whichever event happens first. During the hold current timeout period, the DAC output is held at 0.133V (the hold current) for FullStep mode, or the DAC outputs are held as they were prior to stopping for the microstep mode. After the hold current timeout period, output drivers A, B, $\overline{A}$, and $\overline{B}$ will be deasserted.
- Wait for Resume Scan signal
- Wait for correct number of pixel periods to resynchronize stepper motor with sensor timing.
- 25% speed forward for y full steps (1 microstep = 4*#pixels in **Fast Feed Step Size** register)
- 50% speed forward for z full steps (1 microstep = 2* #pixels in **Fast Feed Step Size** register).
- Full speed forward (1 microstep = #pixels in **Scanning Step Size** register), with TR pulses synchronized to same the position on image that they would have been had scanner not stopped.

The **Lines to Process After Pause Scan Signal/Lines to Discard After Resume Scan Signal** register is not used in reversing mode.

4.5 Fast Feed Step Size Register

When the motor is being moved quickly (High Speed Forward or Reverse command or Steps to Skip at Start of Scan register), the microstep period comes from this register.

For all other motor movement, the microstep size is given in the **Scanning Step Size** register.

4.6 Stepper Motor Current Control Using PWM

There is an option to use Pulse Width Modulation of the current in the stepper motor to increase high speed torque, optimize efficiency, and allow use of a lower current, less expensive motor. Precisely controlling the current in the motor provides several benefits. In Full Step Mode, the motor can start moving faster and overcome inertia by increasing the current to the motor to 100% when it is starting from a dead stop. After a programmable number of steps, the inertia is overcome and the current can be reduced to 70% to reduce heat in the stepper motor (allowing a less expensive motor to be used). When stopping the stepper motor, the current is increased to 100% for a short time to overcome the forward momentum, then the motor is held in position with a low-level standby current of 25%. If the motor is motionless for more than the Hold Current Timeout period, the current goes to 0%.

In microstepping mode, the PWM is used to approximate a sine wave as shown in Figure 10.

The current control is accomplished by measuring the average motor winding current through a sense resistor to ground, comparing it to a reference voltage, and PWMing the motor driver transistor(s) to force the current to be equal to the reference current. See the **Stepper Motor Current Controller Block Diagram** at the end of this document.

5.0 Scanner Support Functions

5.1 Illumination Control Block

Scanner systems require an illumination source to supply the light to the image being scanned. This source may be white (typically a fluorescent lamp), or red, green, and/or blue LEDs. There are four illumination modes in the LM9833:

Illumination Mode	Description
0	$LAMP_R$, $LAMP_G$, $LAMP_B$ outputs = 0. This is the power-on default.
1	Scanning with white light: $LAMP_R$ and $LAMP_B$ controlled by LAMP On/Off pointers in horizontal pixel counter (as in Mode 3), $LAMP_G$ is a PWM pulse stream
2	Scanning with 3 LEDs in color: $LAMP_R$ turns on for Red lines $LAMP_G$ turns on for Green lines $LAMP_B$ turns on for Blue lines
3	Scanning with 3 LEDs in gray: $LAMP_R$ turns on for all lines $LAMP_G$ turns on for all lines $LAMP_B$ turns on for all lines

Figure 19: Illumination Modes

In Illumination Mode 1, the lamp connected to the $LAMP_R$ pin is controlled by the $LAMP_R$ On/Off settings in the configuration register. The $LAMP_B$ output (if used) is controlled the same way. If the lamp is supposed to be on all the time, then the On setting should be set to a number between 0 and the value in the Line End register, and the Off register should be set to a number greater than the value in the Line End register. Conversely, if the lamp is supposed to be off all the time, then the On setting should be set to a number greater than the value in the Line End register, and the Off register should be set to a number between 0 and the value in the Line End register. The $LAMP_G$ output is a Pulse-Width-Modulated pulse stream whose duty cycle is controlled by the value in the PWM register (0-4095). The duty cycle is therefore equal to the register value/4096. The PWM counter is clocked with the 48MHz clock so the output frequency is 48MHz/4096 = 11.7kHz. This PWM output can be used to control the brightness of a fluorescent lamp.

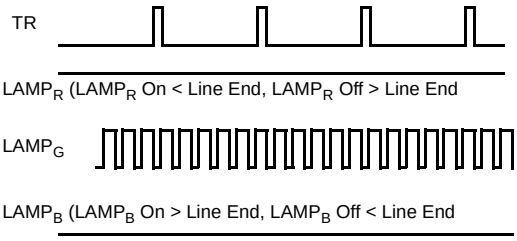


Figure 20: Illumination Mode 1

In Illumination Mode 2 (which is typically used in conjunction with **1 Channel Color**), the $LAMP_R$, $LAMP_G$, and $LAMP_B$ outputs are cycled through sequentially, one line at a time. An internal color counter keeps track of the color of the line to be integrated, and takes that color's LAMP output high when the pixel counter

Applications Information (Continued)

reaches the value stored in that color's LAMP On register (Configuration Registers 2C-37). If the On value is greater than the value in the Line End register, then that lamp never turns on. That color's LAMP output goes low when the pixel counter reaches that color's Off value. If the Off value is greater than the value in the Line End register, then the pixel counter will never reach the Off value and the lamp will always stay on. Illumination Mode 2 timing is shown in Figure 21, and in slightly more detail in Figure 33.

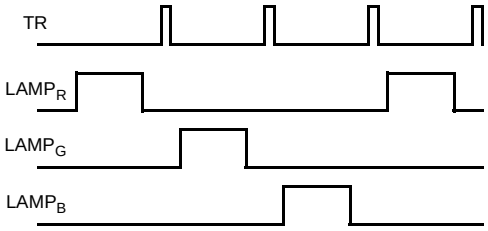


Figure 21: Illumination Mode 2

Illumination Mode 3 is similar to Illumination Mode 2, except that the LAMP outputs for all three colors are turned on and off every line. Illumination Mode 3 timing is shown in Figures 22 and 23. The Lamp On and Lamp Off settings work the same as in Mode 2 to control the on and off points for the different lamp signals. In systems with a limited power budget, care should be taken to prevent turning multiple lamps on at the same time. This can also be important for CIS sensors that limit the maximum combined current of the three lamps.

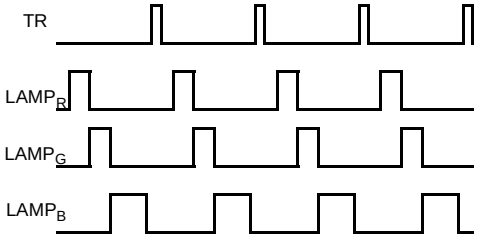


Figure 22: Illumination Mode 3 (grayscale)

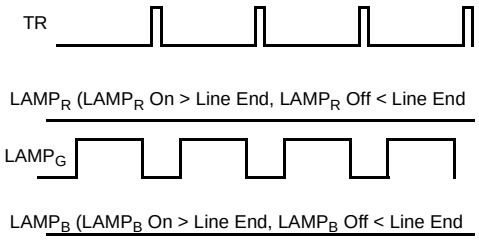


Figure 23: Illumination Mode 3 (green only)

These modes are in operation whenever the chip is powered on and not in standby mode. For example, the LAMP outputs in Figures 21 and 22 keep pulsing whether the LM9833 is in the Idle, High Speed Forward or Reverse, or Scanning states. This eliminates light amplitude variations due to the lamp/LEDs warm-up characteristics. Since the LAMP pulses are synchronized to the TR pulse, which is determined by the horizontal pixel counter, this means that the pixel counter is constantly running, and any new scans can only be started by waiting for the next new line (the next Red line in the case of Illumination Mode 2).

5.2 CCD/CIS Control Block

This function generates the clock signals necessary to control a CCD or CIS sensor. Refer to the descriptions for registers 0B to 18 for more details on the timing of specific signals. The LM9833 features:

- Independent control over the polarity (inverting or noninverting) of the input stage to accommodate CIS or CDS signals.
- Full timing control of the CIS and CDS sample points. Reference and signal sample points can be independently adjusted. Note that the absolute time between reference sample and signal sample must be 2 MCLKs or greater, whether CDS is on or off.
- Ability to turn off CDS. When CDS is on, traditional CDS is performed. When CDS is off, the signal is sampled at the Sample Signal point, but the internal reference is used for the Sample Reference voltage (not a point on the input signal itself).
- The CP1 output supplies the CP pulse needed on some popular Toshiba CCDs. This looks and acts just like another, independent RS pulse.
- A CP2 output is another independent pixel rate pulse that (if needed) can be programmed to supply an additional clock.
- CCD clock signals RS, CP1, CP2 are reset when Line Ends
- The internal Clamp signal is reset with Optical Black Pixels End.
- TR1 and TR2 pulse widths are always the same width, as determined by Register 0E.
- The TR-Ø1 guardband may be equal to 0, causing TR and Ø1 to go high simultaneously and low simultaneously (Figure 24). This is a requirement of some Canon CIS sensors.

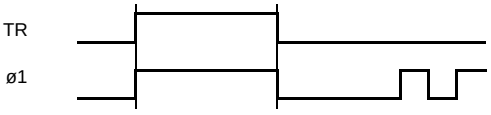


Figure 24: TR-Ø1Guardband Can Be Equal To 0

- CIS TR1 Timing Mode 1. In this mode the TR1 pulse is exactly one Ø clock long, occurring on the rising edge of Ø1. The TR1 pulse width and guardband settings are ignored. For Dyna CIS.

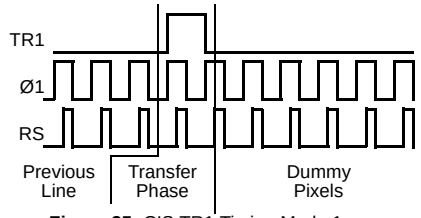


Figure 25: CIS TR1 Timing Mode 1

- CIS TR1 Timing Mode 2. In this mode the TR pulse is again equal to 1 Ø period, but now it is centered around Ø1. The TR pulse width and guardband settings are ignored. For Canon CIS.

Applications Information (Continued)

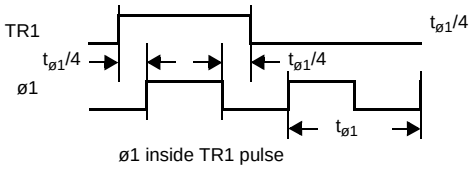


Figure 26: CIS TR1 Timing Mode 2

- To prevent sensor saturation, the LM9833 is always clocking the CCD/CIS, except when it is in Reset or Standby (Register 7 bit 2 or 3 = 1).
- There is a bit for **Fake Optical Black Pixels** (register 19, bit 2). This is used with Dyna CIS sensors. In this mode, the RS output pulses once inside the TR1 pulse, then is held high until the end of the optical black pixels. The TR1 pulse is extended until the trailing edge of the first RS pulse. This mode works for TR1 only, under all TR1 settings (normal and CIS TR1 Timing modes 1 and 2).

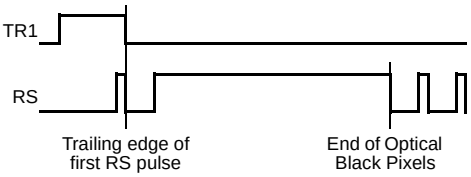
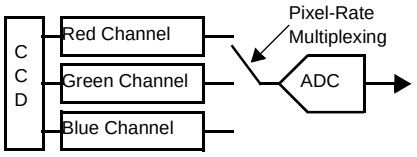


Figure 27: Fake Optical Black Pixels

5.3 AFE Operation

The LM9833 supports the following operation modes, controlled by registers 26 and 27:

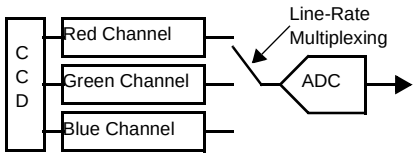
- 3 Channel Pixel Rate Mode. In this mode all three channels are converted with the multiplexer in front of the ADC switching at the ADC conversion rate, producing interleaved RGB data that is transferred to RAM. The ADC runs at MCLK/8, each channel's pixel rate is MCLK/24. Each color has its own offset and gain coefficients. This mode typically uses Illumination Mode 1.



ADC Out LIne 1: RGBRGBRGBRGBRGB...
ADC Out LIne 2: RGBRGBRGBRGBRGB...
ADC Out LIne 3: RGBRGBRGBRGBRGB...

Figure 28: 3 Channel Pixel Rate Mode

- 3 Channel Line Rate Mode. In this mode all three channels are converted with the multiplexer in front of the ADC switching at the line rate, producing a line of Red data, followed by a line of Green data, followed by a line of Blue data, etc. that is transferred to RAM. The selected channel and the ADC both run at MCLK/8. Each color has its own offset and gain coefficients. This mode typically uses Illumination Mode 1.



ADC Out LIne 1: RRRRRRRRRRRRRRR...
ADC Out LIne 2: GGGGGGGGGGGGGG...
ADC Out LIne 3: BBBBBBBBBBBBBBB...

Figure 29: 3 Channel Line Rate Mode

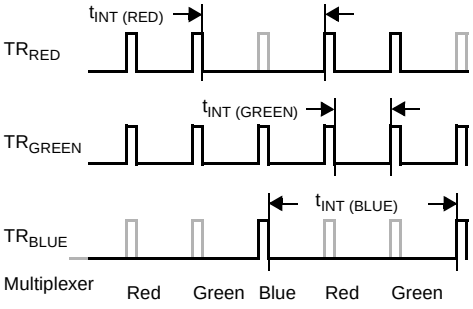


Figure 30: 3 Channel Line Rate TR Pulse Timing

In the 3 Channel Line Rate Mode three TR pulses are generated. TR_{RED} is the TR1 output, TR_{GREEN} is the TR2 output, and TR_{BLUE} is the CP2 output. In this mode TR pulses for a particular color can be "skipped", increasing the integration time for that color. In the example shown in Figure 30, the red channel sees 2 times the integration time of the green channel, and the blue channel sees 3 times the integration time of the green channel. Each channel can be independently programmed to drop 0, 1, or 2 TR pulses.

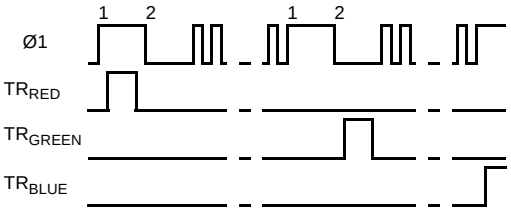
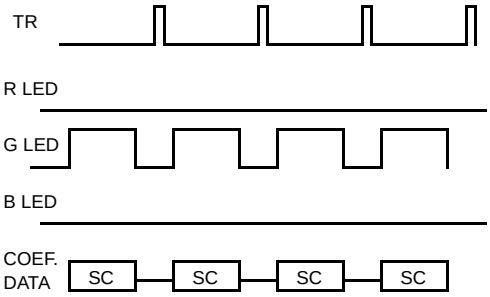


Figure 31: 3 Channel Line Rate Mode with 2 TR Pulse Positions

Each color's TR pulse can be programmed to occur in position 1 (inside Ø1 high) or position 2 (inside Ø1 low), as shown in Figure 31.

- 1 Channel Grayscale: Uses the selected channel's offset and gain coefficients for all lines. 1 Channel Grayscale is used to scan a grayscale images. This mode typically uses Illumination Mode 1 when used with a 3 Channel Color sensor, or Illumination Mode 3 when used with a 1 Channel sensor.

Applications Information (Continued)



SC = selected channel (=green in this example)

Figure 32: 1 Channel Grayscale

- 1 Channel Color: This mode uses a sensor tied to the Blue OS input only. Illumination is switched in RGBRGB pattern at the line rate. Each color has own digital offset and gain coefficients as well as static Gain and Offset data. Note that there is a one line delay between when a line is exposed to a color and when pixels of that color are clocked out of the sensor. For example, the Green LEDs should be on while you are clocking out Red pixels. This mode uses Illumination Mode 2.

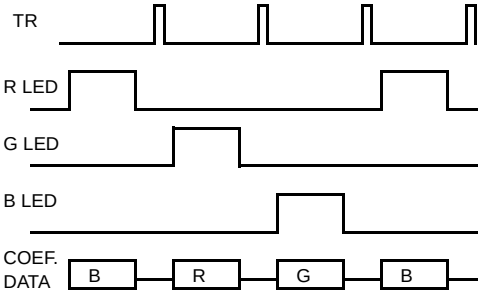


Figure 33: 1 Channel Color

5.4 External DRAM Interface

The LM9833 supports two external DRAM sizes: 256k x 16 and 1M x 16. The DRAM is used for line buffering, gain (shading) coefficient data, offset coefficient data, and gamma correction. 48kwords (16k pixels * 3 colors) are used for gain coefficients, and another 48kwords (16k pixels * 3 colors) for the offset coefficients. Gamma correction consumes 12kwords (4k x 3 colors). The remaining RAM (148kwords = 296kB for 256k DRAM, or 916kwords = 1,832kB for 1M DRAM) is used for the circular image data buffer. The 1M size does not necessarily provide a performance advantage (except perhaps when the USB bus is heavily loaded and I/O is very slow) - the option is there to provide an alternative to the 256k in case of a supply shortage of 256k DRAMs.

Because the LM9833 does not use any EDO or Fast Page Mode features, it can work with either EDO or Fast Page Mode DRAM. The LM9833 should work with most 50-60ns 256k x 16 or 1Mx16 DRAM. Examples:

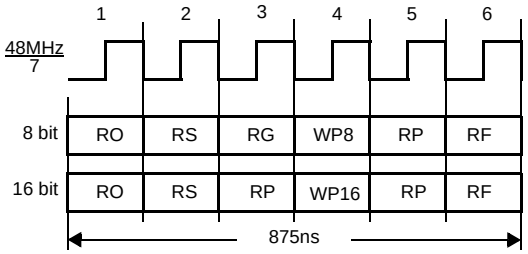
Samsung: KM416C1000C/C-L-5, KM416C1200C/C-L-5, KM416C1004C/C-L-5, KM416C1204C/C-L-5 (5V)

KM416V1000C/C-L-5, KM416V1200C/C-L-5, KM416V1004C/C-L-5, KM416V1204C/C-L-5 (3V)

Alliance: AS4C1M16E5-50 (5V), AS4LC1M16E5-50 (3V)

Micron: MT4LC1M16E5DJ-5, MT4LC1M16E5TG-5 (3V)

There are 2 scan modes: 8 bit and 16 bit. The 8 bit mode is used for normal scanning to application software to generate 8 bit gray or 24 bit color images. The 16 bit mode is used for calibration.



RO: Offset Coefficient read

RS: Shading (Gain) Coefficient read

RG: Gamma Table read

WP8: 8 bit pixel write (write 2 pixels as 16 bits every other cycle)

WP16: 16 bit pixel write

RP: read pixel

RF: refresh

Figure 34: DRAM Timing per Pixel

The ADC always converts at 1/8 of the MCLK frequency ($f_{ADC} = f_{MCLK}/8$). The datarate to the DRAM is the ADC rate divided by the HDPI divider setting ($f_{DRAM} = f_{ADC}$/HDPI_DIVIDER. The offset correction data and the gain correction coefficient data are provided at the DRAM datarate.

The DRAM timing is shown in Figure 34. All the read and write operations shown in Figure 34 must be done for every pixel written to DRAM. That limits the pixel datarate to the DRAM to 1/875ns = 1.14MHz. The following equation must be adhered to in order to limit the DRAM datarate to 1MHz or slower:

(MCLK div)(HDPI divider)(Int Time Adj) >= 6

Int Time Adj refers to the value in register 19, and will be discussed in a later section. If register 19 = 0, then the value of Int Time Adj = 1 (for the purpose of this equation).

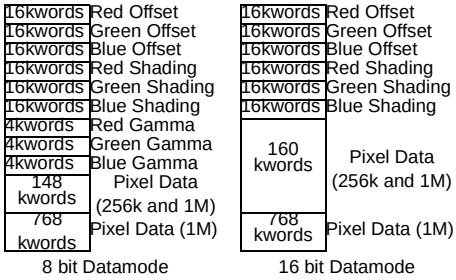


Figure 35: Memory Map of External DRAM

5.5 PAPER SENSE and MISC I/O

These 8 pins are used for home and paper sensing, LED displays, user start buttons, etc.

Two pins are dedicated inputs: PAPER SENSE 1 and PAPER SENSE 2. The other six pins, MISC I/O 1-6, can be configured as

Applications Information (Continued)

inputs or outputs.

The state of each pin, True or False (1 or 0), is reflected in the Status Register.

These are the configurable aspects of these I/O pins:

- Input or Output function. If this bit is set to a 0, the pin is configured as an input. If this bit is set to a 1 the pin is configured as an output.
- The polarity of the input. If this bit is set to a 1 (Active High), a high level on that input pin will produce a True reading (1) in the Status Register. If this bit is set to a 0 (Active Low), a low level on that input pin will produce a True reading (1) in the Status Register.
- Level or Edge Sensitive. If this bit is set to 0 (Level Sensitive), the Status Register will reflect the current state at that sensor input pin. If this bit is set to 1 (Edge Sensitive), the Status Register for that input will be True (1) if there were any False to True transitions at that sensor input pin since the last time the Status Register was read. Reading the status register clears the state of all the edge sensitive inputs to False (0).
- PAPER SENSE 1 can be programmed to stop a scan, high speed forward, or high speed reverse command (by clearing the Scanning bit) when its state (as reflected in the Status Register) changes from False to True. For flatbed scanners this sensor can be used to detect the home position. In sheetfed systems, PAPER SENSE 1 can be used to detect whether or not the user has inserted a document to be scanned.
- PAPER SENSE 2 can be programmed to stop the scan or high speed forward (by clearing the Scanning bit), and also set its bit in the Status Register to True a programmable number of lines after its input pin changes state from False to True. In sheetfed scanners this is useful if the PAPER SENSE is located *before* the scanner array, where the sensor will change states before all of the paper has been scanned. This can be used in flatbeds to prevent the motor from trying to step past the limits of travel of the system. This input should not be used as the home position sensor in flatbed scanners, since it will not stop a high speed reverse command.
- If they are configured as outputs, the MISC I/O 1-6 pins can have their outputs set to +5V or 0V by writing a 1 or a 0 to the appropriate bit.

The default state of the MISC I/O pins is described in detail in the Register Listing section. The Misc I/O pins revert to their default states on power-on, after entering USB Suspend, or when the RESET pin is pulsed high. A Soft Reset (register 07) does not reset the MISC I/O pins. The default states of the MISC I/O pins are:

- MISC I/O 1: Input, edge sensitive, high-to-low transition sets bit 2 of register 2.
- MISC I/O 2: Input, edge sensitive, high-to-low transition sets bit 3 of register 2.
- MISC I/O 3: Input, edge sensitive, high-to-low transition sets bit 4 of register 2.
- MISC I/O 4: Output, voltage on MISC I/O 4 pin = V_D.
- MISC I/O 5: Output, voltage on MISC I/O 5 pin = V_D.
- MISC I/O 6: Output, voltage on MISC I/O 6 pin = 0V.

5.5.1 Adding Function Buttons

Many scanners today feature multiple buttons to select scan, copy, fax, email, etc. functions. The LM9833's MISC I/O pins can be used for these functions. To free up MISC I/O inputs for other functions, or if more than 6 buttons are required, you can multiplex the buttons together. Figure 36 shows how 7 buttons can be multiplexed into only 3 MISC I/O lines. Figure 37 shows how to decode the data in register 2 to determine which button was pressed. This multiplexing technique can easily be scaled to allow for more or less buttons with the minimum number of MISC I/O lines.

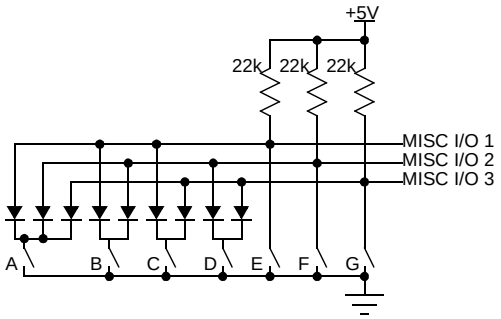


Figure 36: Remote Wakeup With Up To 7 Switches

Switch	MISC I/O 1	MISC I/O 2	MISC I/O 3
No Switch Pressed	1	1	1
A	0	0	0
B	0	0	1
C	0	1	0
D	1	0	0
E	0	1	1
F	1	0	1
G	1	1	0

Figure 37: Truth Table for Remote Wakeup With Up To 7 Switches

5.6 The Brains

This is the master control section that keeps track of the position of the CCD pixel going through the analog front end, the color of that line of CCDs (for single output CCD illumination control), the stepper motor, and all other system coordination.

6.0 Communicating with the LM9833

Everything on the LM9833 (configuration settings, image data, coefficient data, and gamma tables) is accessed through the Configuration Register. Configuration Register I/O is done through two steps. The first step is to write the address (0 through 7F) of the configuration register to be read from or written to. The second access is the data operation (a read or a write) for that address. The address only needs to be written once. After an address is written, any number of reads and/or writes may be made to that address.

Registers 0, 1, and 2 are read-only registers. Writing to these addresses may affect various counters inside the LM9833 and

Applications Information (Continued)

should therefore be avoided. Bits 4 of register 3 is also read only, however it is OK to write to register 3. All of the remaining configuration registers can be read from and written to using this protocol.

Registers 03-06 (the Dataport), 2A-27 (Illumination), 38-3D (Static Gain and Offset), 42 (Offset and Gain Source, bits 0-2), 45 (Stepper Motor Status), and 58-5B (Paper Sense and Misc. I/O) may be written to while the chip is in the Idle state. The LM9833 must be in Soft Reset mode to write all other configuration registers (see **10.2 Soft Reset**).

6.1 The DataPort: Reading and Writing to Gamma, Offset, and Gain Memory

Because the gamma table and the shading and offset correction blocks of RAM are very large, the LM9833 uses an indexed method of reading and writing them, called the DataPort. Four addresses in the Configuration Register are used to implement this feature, as shown in Figure 38.

Configuration Register Address	Name	Bits
3	DataPort Target/ Color	b3- b0
4	DataPort Address (MSB)	b13 - b8
5	DataPort Address (LSB)	b7 - b0
6	DataPort	b7 - b0

Figure 38: DataPort

The DataPort allows the user to select a memory block (gamma, gain coefficient, or offset coefficient) and color (red, green, or blue) to be read from or written to, by writing to Configuration Register Address 3.

The starting address of that block (usually 0) is written into the DataPort Address register (at Configuration Register Addresses 4 and 5). Bit D6 of register 4 should also be set to a 0 or a 1 to indicate whether the DataPort will be read from (D6 = 1) or written to (D6 = 0) in subsequent operations. This is required so the LM9833 can prefetch the data for faster access. The DataPort Address is automatically incremented after every word (2 bytes) of Offset, Shading, or Gamma data is read/written.

Once the memory block, color, and starting address are written, a series of reads or writes to the DataPort will read from or write to the selected memory block at maximum speed.

Registers 4 and 5 should always be written to after Register 3 has been changed.

Reading and writing the DataPort should only be done when the LM9833 is not scanning (Register 07 = 0).

6.1.1 DataPort Type and Color

These 3 bits determine which memory block (gamma, gain, or offset coefficients, Figure 39) and which color of that memory block

7	6	5	4	3	2	1	0	Type
-	-	-	-	-	-	0	0	Offset
-	-	-	-	-	-	0	1	Gain
-	-	-	-	-	-	1	0	Gamma
-	-	-	-	-	-	1	1	Undefined

Figure 39: DataPort Target Pointer

(red, green, or blue, Figure 40) is to be read from or written to.

7	6	5	4	3	2	1	0	Color
-	-	-	-	0	0	-	-	Red
-	-	-	-	0	1	-	-	Green
-	-	-	-	1	0	-	-	Blue
-	-	-	-	1	1	-	-	Undefined

Figure 40: DataPort Color Pointer

6.1.2 DataPort Address

This 14 bit register (at Configuration Register addresses 4 and 5) determines what the starting address is for the read/write operation. *This address is automatically incremented after every 2 byte word read/write operation to the actual DataPort.* For the gamma table the range is 0 to 4093. For the Gain and Offset Coefficients this range is 0 (corresponding the first valid pixel as programmed in the Valid Pixels Start register) to 16383 (the maximum number of image pixels). If reads or writes continue past 4093 or 16383, the DataPort address counter wraps back around to 0 and continues counting.

6.1.3 DataPort

The DataPort is the 8 bit register (Configuration Register address 06) where the data is sequentially read from or written to. The formats for Offset, Gain, and Gamma data are shown in Figures 41, 42, and 43.

7	6	5	4	3	2	1	0	Type
b15	b14	b13	b12	b11	b10	b9	b8	First Byte
b7	b6	b5	b4	b3	b2	b1	b0	Second Byte

Figure 41: DataPort Offset Format

7	6	5	4	3	2	1	0	Type
b15	b14	b13	b12	b11	b10	b9	b8	First Byte
b7	b6	b5	b4	b3	b2	b1	b0	Second Byte

Figure 42: DataPort Gain Format

7	6	5	4	3	2	1	0	Type
0	0	0	0	b11	b10	b9	b8	First Byte
b7	b6	b5	b4	b3	b2	b1	b0	Second Byte

Figure 43: DataPort Gamma Format

Applications Information (Continued)

7.0 The USB Interface

The LM9833 uses the USB (Universal Serial Bus) interface. Refer to the LM9833 software package for details on USB communication.

7.1 The USB Pins

Data is received and transmitted through the D+ and D- pins. These are 3V differential signals. Figure 44 shows the recommended circuitry between the LM9833's D+ and D- pins and the scanner's USB connector.

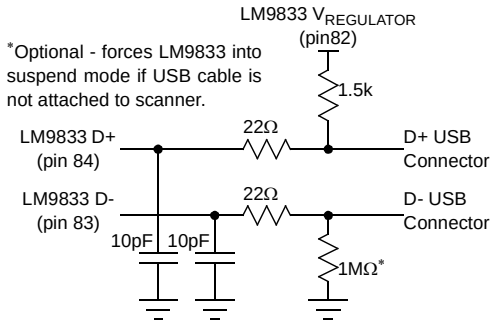


Figure 44: Recommended USB Component Values

8.0 Scanning

The following sections describe the typical steps taken to scan an image.

8.1 Start Scanning - Initiating an Image Scan

An image scan is initiated by writing a Scan command to Register 07. The LM9833 will move the sensor forward the number of full-steps specified in registers 4A/4B and begin scanning. Scanning ends when the host writes a new command to the command register (Idle, High Speed Forward or High Speed Reverse) or when PAPER SENSE 1 or PAPER SENSE 2 changes state (if programmed to do so).

The line buffer is reset when the Scanning bit is SET, not when it is cleared. The host can continue to read stored data out of the line buffer after a scan has stopped.

Pixel data is read from configuration register address 00. Registers at other addresses can be read during a scan (to read the LM9833's status registers, abort the scan, etc.).

If for some reason you want to pause the scan for some length of time and resume later, do NOT stop the scan (return to Idle). Simply stop reading pixel data. When the buffer fills up, the LM9833 will automatically stop scanning and turn off power to the stepper motor (when the delay goes beyond the time specified in the Hold Current Timeout register).

The last 2 bytes of every line is a status word indicating how much data is in the image buffer at the time the status word was written. This information is in the 8 LSBs of the status word, and has the same format as Register 01.

8.2 Reconstructing 8 bit Image Data Received By the PC

When reconstructing an image from the stream of data received from the LM9833, it is useful to know the format of the data. The LM9833 does not perform deinterleaving on the pixel data, it comes out exactly as the sensor sends it. Deinterleaving must be performed on the host PC.

For a single output CCD/CIS that outputs one line of data with colors alternating at the line rate, the output format is:

$R_1, R_2, R_3, R_4,..., R_{n-2}, R_{n-1}, R_n$ (line m)

$G_1, G_2, G_3, G_4,..., G_{n-2}, G_{n-1}, G_n$ (line m + 1)

$B_1, B_2, B_3, B_4,..., B_{n-2}, B_{n-1}, B_n$ (line m + 2)

For a triple output CCD/CIS that outputs 3 lines of data (each x pixels apart in the vertical direction) with colors alternating at the pixel rate, the output would be:

$R_1, G_1, B_1, R_2, G_2, B_2,..., R_{n-1}, G_{n-1}, B_{n-1}, R_n, G_n, B_n$

with the Red data representing line m+x, the Green data representing line m, and the Blue data representing line m-x. "x" is the separation between lines, which depends on the physical distance between the R, G, and B sensors and the rate at which the sensor is moving over the image.

The length of a line of image data sent to the PC depends on several factors:

- The range of pixels to be scanned (Data Pixels): Data Pixels = (Data Pixels End - Data Pixels Start),
- The horizontal resolution set in the configuration register (HDPI_Divider)
- The number of bits per pixel (1, 2, 4, or 8, called B), and
- The color mode: pixel rate (C=3) or line rate (C=1).

$$\text{Bytes/Line} = 2 \cdot \text{INT}\left(\frac{\text{INT}\left(\frac{\text{Data Pixels}}{\text{HDPI\_Divider}}\right) \cdot C \cdot B}{16}\right)$$

The scanner software on the host must strip the 2 byte status word from the end of each line before reconstructing the image.

8.2.1 Reconstructing 16 bit Image Data Received By the PC

In the 16 bit Data Mode the Gamma Correction and Pixel Packing stages are bypassed. Each pixel comes out as 2 bytes instead of 1, doubling the amount of memory needed to store one line. The data format is shown in Figure 45. This mode is otherwise identical to the 8 bit mode. The number of bytes per line in 16 bit mode is given in this equation:

$$\text{Bytes/Line} = 2 \cdot \text{INT}\left(\frac{\text{Data Pixels}}{\text{HDPI\_Divider}}\right) \cdot C$$

The 16 bit mode is used to acquire 16 bit data for accurate gain and offset calibration.

7	6	5	4	3	2	1	0	Type
b15	b14	b13	b12	b11	b10	b9	b8	First Byte
b7	b6	b5	b4	b3	b2	b1	b0	Second Byte

Figure 45: 16 bit Data Format

8.3 High Speed Forward

When register 07 is set to a 1, the LM9833 moves the motor forward at maximum speed (determined by the fast feed stepsize, registers 48 and 49) until a 0 is written to register 07 or either one

Applications Information (Continued)

of the PAPER SENSE inputs becomes True (if that sensor has been properly programmed to interrupt scanner movement). PAPER SENSE 2 can be used to cause a delayed stop. If the **FullSteps to Scan after PAPER SENSE 2 trips** register is greater than 0, motor movement will continue for the programmed number of full steps. This can be used to eject paper in sheetfed scanners.

The LM9833 also features a Programmed High Speed Forward command. This is identical to the High Speed Forward function, except that it will automatically stop moving once the motor has moved the number of lines specified in registers 4A and 4B.

8.4 High Speed Reverse

When register 07 is set to a 2, the LM9833 moves the motor backwards at maximum speed (determined by the fast feed step-size, registers 48 and 49) until a 0 is written to register 07 or either one of the PAPER SENSE inputs becomes True (if that sensor has been properly programmed to interrupt scanner movement). The **FullSteps to Scan after PAPER SENSE 2 trips** register is not used in the High Speed Reverse mode. This function is generally used to home the sensor in flatbed scanning applications.

The LM9833 also features a Programmed High Speed Reverse command. This is identical to the High Speed Reverse function, except that it will automatically stop moving once the motor has moved the number of lines specified in registers 4A and 4B.

8.5 Short Example of a Scan

- PC configures the LM9833 by writing to the configuration registers.
- PC has the LM9833 scan a calibration image, then calculates the calibration coefficients for the scanner.
- PC transmits the calibration information to the LM9833.
- If a sheetfed, the PC now polls the LM9833 status registers to see if there is any paper inserted. If a flatbed, it moves the scan head to the home position.
- PC sets the Scanning bit in the Configuration Register.
- PC calculates the size of the image to be scanned in bytes, then reads bulk data from register 00 of the LM9833 until it has read the entire image. If for some reason the scan needs to be aborted, the PC writes a 0 to register 07.
- After all image data is read, PC writes a 0 to register 07 to stop scan.
- If this is a flatbed scanner, the PC should now send a High Speed Reverse command to send the sensor back to the home position. For a sheetfeeder, it can send a High Speed Forward command to eject the remainder of the image.
- The scanner is now in the idle state.

9.0 Master Clock Source

The timing for the entire chip comes from the CRYSTAL OUT pin. Typically this pin is used (with the CRYSTAL IN pin) as a crystal oscillator. The clock frequency should be 48MHz. This 48MHz clock is divided by the MCLK divider (register 08), and the divided output is MCLK (Master CLocK). The MCLK divider range is from 1.0 to 32.5 in steps of 0.5. A configuration register code of 0 divides the clock by 1.0, while a code of 63 divides the clock by 32.5. AT 48MHz, this provides an MCLK range of 1.48MHz to 48MHz and a corresponding ADC conversion rate of 184kHz to 6.00MHz. This divider can be used to closely match the output data rate to the PC's input data rate, minimizing scan time.

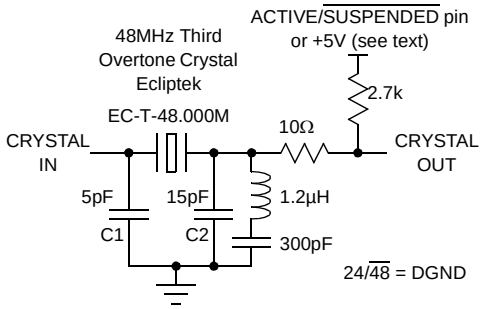


Figure 46: 48 MHz Crystal Oscillator Circuit

MCLK is used to clock the vast majority of the LM9833's circuits. CRYSTAL OUT is directly used in the USB I/O section, DRAM timing, and a few subsections where the highest possible clock speed is required (such as the PWM pulse generator for the light source and the stepper motors).

To use the LM9833's crystal oscillator feature, tie the CRYSTAL/EXT CLK pin to DGND. Figure 46 shows the recommended loading circuit and values for a 48MHz oscillator. These component values assume 10pF of stray capacitance between CRYSTAL IN and ground, and 10pF between CRYSTAL OUT and ground, for a total CRYSTAL IN and CRYSTAL OUT loading of 15pF and 25pF.

A 2.7k pullup to a 5V source is necessary to ensure oscillator start-up. For self-powered systems, any clean source of +5V can be used. For bus-powered systems, this pin must be connected to the ACTIVE/SUSPENDED pin in order to meet USB suspend power consumption requirements.

When laying out the crystal oscillator components, always keep the traces as short as possible, to minimize stray capacitance and inductive noise coupling, particularly on the CRYSTAL IN pin.

Operation at 24MHz ($24/\overline{48} = V_D$) is not reliable and should not be used.

To drive the LM9833 with an external 48MHz clock, tie CRYSTAL/EXT CLK (pin 54) to V_D, tie CRYSTAL_IN to DGND, and drive the TTL or CMOS-level clock signal into CRYSTAL_OUT (pin 52).

10.0 INITIALIZATION

10.1 Power On Reset (POR)

POR is generated by the ramp of the V_A supply pins from 0V to +5V. A low to high to low signal on the external RESET pin will also generate a POR. A POR event:

- Resets the USB transceiver. All enumeration and configuration data will be reset to its default setting.
- The oscillator will start (or continue) oscillating.
- Forces all configuration registers that have defaults (shown as black boxes in the configuration register tables) to their default settings (including the Reset and Standby bits). See the Reset and Standby mode descriptions for more information.
- MISC I/O 1-3 will be configured as inputs and could generate

Applications Information (Continued)

remote wakeup signals (after the device is initialized).
- MISC I/O 4-6 are configured as outputs.

10.2 Soft Reset

A Soft Reset is generated by setting bit 5 of register 07. A Soft Reset:
- Stops most of the internal clocks inside the system to save power.
- Does NOT stop 48MHz oscillator.
- Resets internal state machines for correct operation after register changes.
- Stops DRAM refresh. This will corrupt all the gamma, offset, gain values, as well as any image data, stored in the external DRAM.
- Does NOT prevent configuration register read/writes.

The following procedure should be followed to produce a Soft Reset:
- Set register 0x07 to 0x00 (Idle)
- Set register 0x18 to 0x18 (disabling sampling)
- Set register 0x07 to 0x20 (Reset)
- Write original value back into register 0x18, write additional configuration registers (if desired)
- Set register 0x07 to 0x00 (Idle)

10.3 Standby

The LM9833 enters the Standby mode by setting bit 4 of register 07. Standby Mode:
- Powers down the analog section to conserve power.
- Tristates the stepper motor outputs (regardless of the state of register 45, bit4).
- Does NOT prevent configuration register read/writes.

10.4 Suspend Mode: Entering

Suspend Mode is entered when the USB bus has had no activity for 3ms. The Suspend state forces the LM9833 into a low current idle state. Suspend Mode:
- Stops the oscillator.
- Forces all black-box highlighted configuration registers to their default settings (including the Reset and Standby bits). See the Reset and Standby mode descriptions for more information.
- MISC I/O 1-3 will be configured as inputs and can be used as remote wakeup signals.

10.5 Suspend Mode: Exiting

When the LM9833 exits Suspend Mode:
- The oscillator is restarted.
- The Reset and Standby bits are still set. The driver software is responsible for clearing them and setting the configuration registers again to resume operation. All configuration registers and DRAM data should be re-written after a Suspend sequence.

11.0 USEFUL EQUATIONS

The integration time (t_{INT}) for 1 line is always:

$$t_{INT} = \text{pixel\_period} \cdot \text{line\_length}$$

where pixel_period is the time it takes to clock one pixel out of the sensor (C = 3 for Pixel Rate Color, and 1 for all other modes):

$$\text{pixel\_period} = \frac{\text{mclk\_div} \cdot C \cdot 8}{48\text{MHz}}$$

and line_length is the length of an entire line, measured in units of pixels. Note that this includes the transfer portion of the line:

$$\text{line\_length} = \text{line\_end} + \text{TR\_time}$$

These equations apply for any ITA (Integration Time Adjust, Register 19) setting.

To maximize scanner throughput, it is desirable to generate data at the same rate as the digital I/O to the host PC. Under some conditions (slow digital I/O, or very high resolution scans), the time to generate one line may be greater than the maximum integration time. In this case, the integration time may be set to an acceptable value using the previous equations, and the time to process a line extended using Register 19 (the ITA function).

Using the ITA function, the time to process 1 line can be extended to match the digital I/O rate required:

$$t_{LINE} = (1 + \text{ITA}) t_{INT}$$

The maximum DRAM write pixel rate allowed is 1MHz. If you configure the LM9833 to generate data any faster then 1Mpixel/s, the LM9833 will not function correctly. To ensure that the LM9833 is programmed to a legal datarate, ensure that this constraint is met:

$$\text{mclk\_divider} \cdot \text{HDPI\_divider} \geq 6$$

When using the ITA function (ITA > 0), use this version of the equation:

$$\text{mclk\_divider} \cdot \text{HDPI\_divider} \cdot \text{ITA} \geq 6$$

Use this equation to calculate the stepsize for a scan:

$$\text{scan\_stepsize} = \frac{\text{line\_length} \cdot \text{vertical\_resolution}}{\text{FSPI} \cdot 4}$$

where vertical_resolution = the desired vertical resolution of the scan, and FSPI = the number of full steps required to move the sensor one inch.

When using the ITA function (ITA > 0), use this version of the equation to compensate for the ITA function:

$$\text{scan\_stepsize} = \frac{\text{line\_length} \cdot \text{vert\_res}}{\text{FSPI} \cdot 4} \cdot \frac{(\text{ITA} + 1)}{\text{ITA}}$$

12.0 CHANGES FROM THE LM9831

12.1 FullStep Timeout Function

The LM9833 features a motor step counter that will automatically stop the scan after a certain number of motor steps. To enable this mode, set register 58, bit 5 = 0, then program the number of fullsteps to scan.

12.2 16 Bit Output Mode

The LM9833's 16 bit output mode is fully functional. It is capable of scanning any image that the LM9833 can scan at 8 bits, and does not require any polling of register 01.

Applications Information (Continued)

12.3 Steps to Reverse Register Increased

To improve performance with some mechanical designs, the number of bits in register 50 was increased from 6 to 8 bits. This allows the scanner to reverse up to 255 steps when pausing due to a buffer full condition.

12.4 - Acceleration Profile Modified

The highest setting of the Acceleration Profile (bits 2-7 of register 51) has been modified to give the motor more time during the acceleration/deceleration phases. In the LM9831, a setting of 3 for the "stopped" time, "25%" time, and "50%" time caused the state machine to spend 3 full steps in that state. In the LM9833, a setting of 3 will cause the state machine to spend 8 full steps in that state.

12.5 1 Channel Color Mode

When using the LM9831 in 1 Channel Color Mode with the hold current timeout set to 0, the LM9831 would sometimes skip a line during a pause/resume cycle. This problem has been fixed in the LM9833.

12.6 DRAM Control Signals

The $\overline{RD}$, $\overline{WR}$, $\overline{CAS}$, and $\overline{RAS}$ pins are now tri-stated when the LM9833 is in Suspend Mode. In a USB bus-powered application where the DRAM is powered down in suspend mode but the LM9833's VDRAM supply still has power, this change prevents the $\overline{RD}$, $\overline{WR}$, $\overline{CAS}$, and $\overline{RAS}$ pins from potentially forward biasing the input protection diodes of the external DRAM which could cause the current drawn from the USB's power source to exceed the 2.5mA maximum allowable current draw when in suspend mode.

12.7 Start of Scan Reset

In the LM9831, the value in register 01 is not reset (and therefore not accurate) until the first line of the image has been scanned. The LM9833 resets this counter as soon as a scan is initiated, so the value in register 01 is always valid.

12.8 Power-On Reset (POR)

The LM9831 has a power-on reset circuit that causes the chip to be reset during power-up when the analog power supply (V_A) passes 2V. If V_A ramped very slowly (2V/ms), this could cause the LM9831 to be reset and start trying to load data from the external EEPROM before the external was EEPROM became active, which could cause the LM9831 to think there was no external EEPROM attached.

The LM9833 has a power-on reset threshold to 3V, to reduce the chance of this occurring. Additionally, the input to the POR comes from V_D, not V_A. This allows the V_A supply to be switched off when in Suspend mode, allowing more flexibility in USB bus-powered designs.

12.9 Remote Wakeup

The LM9833 supports enabling and disabling remote wakeup through the LM9833 minidriver software.

12.10 Reduced Current Consumption

The LM9833 includes 4 current settings (100%, 80%, 70%, and 50%) to control the current consumed by the analog supply (V_A). The LM9833 is tested and guaranteed at the 100% setting, which is the same as the LM9831's analog section. For USB bus-powered settings, To reduce the current consumption (for bus-powered applications) set this register to one of the 3 other settings. The performance of the analog section (INL, DNL, and noise) will degrade at the lower settings, but this may not be noticeable in the final image, particularly with CIS sensors where the noise and non-linearities of the sensor may be far greater than that of the LM9833's analog front end.

12.11 Motor Phase Swap

Bit 5 has been added to register 45 to "swap" the A and B stepper motor phases. This will reverse the stepper motor's direction of movement. This can be used to make the scanner scan in the opposite (or both) directions, provides an alternative means of sensing the home position by scanning towards home until a pattern on the calibration strip (instead of an optical sensor) is detected, and also provides a software fix for a motor that happens to be wired backwards. Note that this only works in fullstep mode.

12.12 ITA Output on $LAMP_B$

The LM9833 adds 1 bit (register 29 bit 2) that, when set, will output the ITA (Integration Time Adjust) phase on the $LAMP_B$ output pin. This signal can potentially be used to turn off the illumination source during the ITA's long integration time period.

12.13 Faster Fullstep Movement

In Fullstep Mode, the LM9831 and LM9833 normally move the motor with the motor winding current set to $0.35V/R_{SENSE}$ ($0.5V/R_{SENSE}$ during the Kickstart period at the start of movement). The problem is that the ideal R_{SENSE} value for microstepping was too small for fullstepping, and vice-versa. So if the scanner needed to use both modes (fullstepping for high speed movement and low resolution scans, microstepping for high resolution scans), there wasn't a sense resistor value that worked well for both.

The LM9833 improves this situation by adding this function: if the Kickstart Steps value (register 55 bits 0-2) is set to 0, the LM9833 will set the winding current to $0.5V/R_{SENSE}$ for all fullstep movement. This provides more current to the stepper motor in fullstep mode, while allowing the sense resistor to be at a value optimized for microstepping.

12.14 Fullstepping Fastfeed, Microstepping Scan

The LM9833 adds 1 bit (register 45 bit 6) that, when set, makes the scanner automatically use fullstep mode for fastfeeding at the start of scan, then switch to microstepping when scan begins.

12.15 Device and Vendor IDs for USB Interface

The LM9833's internal (default) ROM is programmed for a Vendor ID of 0x0400 and Device ID of 0x1002. The Vendor String is "National Semiconductor" and the Device String is "LM9833 48 Bit Scanner".

Applications Information (Continued)

12.16 Paper Sensor #2 Doesn't Stop High Speed Reverse

In the LM9831, a false-to-true transition on Paper Sensor #2 would stop a high speed reverse (usually used for homing in flatbed scanners). Due to the changes made to accommodate the **FullStep Timeout Function** function, the ability to stop a high speed reverse function was removed.

12.17 Turbo and Preview Modes

These modes actually existed in the LM9831, but were not documented.

The Turbo and Preview modes allow additional pixel averaging (horizontal resolution reduction) to be done in the analog domain. This can be useful, for example, when you have a 1200 dpi scanner and wish to scan at 75 or 50dpi. The HDPI divider function's lowest resolution is divide-by-12. With the HDPI divider set to divide-by-8 and turbo or preview mode set to x2, the horizontal resolution will be 1200/16 = 75dpi. With the HDPI divider set to divide-by-12 and turbo or preview mode set to x2, the horizontal resolution will be 1200/24 = 50dpi. The HDPI divider and Turbo/Preview modes can be used in any combination.

For a Preview factor of xN, the Preview Mode operates by increasing the pixel clocks to the CCD by a factor of N, while suppressing (N-1) reset pulses out of every N pixels. This is only useful for CCDs (or CIS sensors made with CCD technology).

In the Turbo Mode, the entire analog front end is run N times faster, and every N pixels are averaged together before they are converted to digital by the ADC. When using Turbo Mode, the range of registers 0F to 18 is reduced by the Turbo Mode factor, according to the following table:

Mode	Pixel Rate	Registers 0F to 18 Range
3 Channel, Turbo off	MCLK/24	0 - 23
3 Channel, Turbo x2	MCLK/12	0 - 11
3 Channel, Turbo x3	MCLK/8	0 - 7
3 Channel, Turbo x4	MCLK/6	0 - 5
3 Channel, Turbo x6	MCLK/4	0 - 3
1 Channel, Turbo off	MCLK/8	0 - 7
1 Channel, Turbo x2	MCLK/4	0 - 3

13.0 PORTING SOFTWARE FOR LM9830 TO LM9833

The LM9833 is similar in architecture to the LM9830. Porting a TWAIN driver from the LM9830 to the LM9833 is relatively straightforward if consideration is given to the following issues. The LM9833 includes almost all the features of the LM9830, plus several new ones. The first step is to change the LM9830 Twain driver so that it works with the LM9833. The second step is to take advantage of the new features of the LM9833 that will allow you to obtain even better, faster scans than you obtained with the LM9830.

13.1 Porting Step 1

13.1.1 Adjust for Register Changes

While more than 50% of the registers in the LM9833 are in the same location and perform the same function as they did in the LM9830, many other registers have changed. Sometimes the address of a register changed, sometimes the location of the bits inside a register were moved, some register settings were combined or deleted, and the size of some registers was changed. Please compare the register listings for the LM9830 and LM9833 carefully. This is a list of registers that have changed:

Registers 1, 2, 3, 4, 7, 9, B, 19, 1A, 1B, 3E-41, 42, 43-44, 4E-4F, 51-53, 54, 5A, 5B, 5E.

13.1.2 Choosing the MCLK Divider (Register 0x08)

The datarate coming out of the Horizontal DPI Divider must be 1.1MHz or less. If it is faster than this, the LM9833 will not operate correctly. Since the maximum USB datarate is about 1MHz, this does not impact the performance of the scanner in any way.

This is the Clock Divider Rule:

(MCLK_divider)(HDPI_divider)(ITA) >= 6

The ITA (Integration Time Adjust) refers to register 19, and will be discussed in a later section. If register 19 = 0, then the value of ITA = 1 for the purposes of this formula.

If register 19 = 0, this formula means that if the HDPI_divider = 1, the MCLK_divider must be set to divide-by-6 (reg 08 = 10 [decimal]) or higher. If the HDPI_divider = 4, the MCLK_divider must be set to divide-by-2 (reg 08 = 2) or higher. If the HDPI_divider is 6 or larger, then the MCLK_divider can be set to divide-by-1 (reg08 = 0).

See **13.2.2 Integration Time Adjustment Function** for additional information.

13.1.3 Calibration

In the LM9830, calibration was always performed at the optical resolution of the scanner. For example, if the optical resolution of the scanner was 600dpi, then calibration was performed at 600dpi even if the scan was going to be at 300dpi or 150dpi.

To keep the speed of the LM9833 high while using slower DRAM (instead of SRAM), the architecture of the LM9833 was changed so that the Horizontal DPI adjust function is performed *before* the pixel rate offset and shading correction, instead of after (as in the LM9830).

This means that the calibration routine needs to be changed so that register 9 is set to the desired scan resolution before calibration.

13.1.4 Pixel Rate Offset Correction

The LM9833 uses 16 bits for the offset correction of each pixel.

Applications Information (Continued)

13.1.5 Pixel Rate Shading Multiplier

The shading multiplier uses all 16 bits of data.

There is an important difference between the pixel rate shading multiplier of the LM9830 and the LM9833. In the LM9830, if the value for the shading multiplier was 0, the gain through the multiplier was 1V/V. The LM9830 also had 3 multiplier gain ranges: 1 to 1.5, 1 to 2.0, and 1 to 3.0 V/V.

The LM9833 has a simpler multiplier with only one gain range: 0 to 4 V/V. The gain of the multiplier is

Gain = (gain code)/16384 V/V

Note that if the gain code = 0, then the pixel is multiplied by 0! In other words, if the gain coefficient is set to 0, the output of the multiplier will be all 0s. A gain code of 0 was not unusual for the LM9830, but will not work with the LM9833. To maintain a minimum gain of 1V/V, make sure the gain code is 16384 or higher.

If desired, gains between 0 and 1 V/V can be used, but they will usually result in less dynamic range and noisier images.

13.1.6 The Gamma Table

The LM9833's 3 gamma tables are 12 bits wide, instead of 10 bits (LM9830). This means each gamma curve has 4 times the number of datapoints and you can now get 4 times the accuracy available with the LM9830.

Since most consumer CCDs have a true SNR of less than 12 bits, the LM9833 does not support a 16 bit gamma table, freeing up an additional 180kwords of DRAM memory.

13.1.7 General DataPort Information

There have been several important changes to the dataport.

The read-only Pause bit is now in register 3. You can write this bit in order to write to the other bits in the register, but anything you write to the Pause bit will be ignored.

There are now 2 bits to select between Offset Coefficients, Gain Coefficients, and Gamma data.

In the LM9830, Offset and Gain coefficients were combined to make one 16 bit word, written to register 6 as 2 bytes.

In the LM9833, Offset is a 16 bit word, and Gain is a 16 bit word. Offset and Gain data each have a separate dataport address. Register 5 will auto increment after 2 bytes are written to register 6 in Offset mode or Gain mode (reg03b1 = 0).

Gamma data is 8 bits wide, as in the LM9830. Register 5 will auto increment after 1 gamma byte is written to register 6 in Gamma mode (reg03b1 = 1).

The bit locations for selecting color (R, G, or B), have been shifted left by 1 bit.

The DataPort address width is now 14 bits wide. This caused the R/W bit to be shifted left by 1 bit.

When using 1 Channel Grayscale, the LM9830 ignored the color bits in register 3. This has been fixed in the LM9833. Register 3 controls the gamma table color.

Make sure your software takes all of these changes into account.

13.2 Porting Step 2

Once your TWAIN driver is operating with the LM9833, you can start taking advantage of the LM9833's additional features.

13.2.1 1200 DPI

The LM9833 can support line widths up to 16384 pixels x 3 colors. This allows 1200dpi scanners with a maximum width of 13.6" (B-size).

13.2.2 Integration Time Adjustment Function

Due to DRAM speed limitations, the maximum speed at which the LM9833 can store pixels is 1MHz. The ADC can run at speeds up to 6MHz, but only when the HDPI divider is set to divide-by-6 or greater, which results in a pixel rate of 1MHz or less.

This can be a challenge when scanning at high resolutions. For example, a 600dpi 8.5" wide color CCD scanner digitizes 15,300 pixels/line. At a 1MHz rate, the resulting integration time is15.3ms. Integration times above 10ms may be problematic in some designs.

To allow shorter integration times without violating the 1MHz max pixel rate, the LM9833 has an Integration Time Adjust (ITA) function (Figure 47). ITA generates 2 alternating timebases for the CCD timing, a high frequency timebase, and a lower frequency timebase. During the high frequency timebase, the integration time (t_{INT1}) is short, as short as the total number of pixels in a line divided by 6MHz. (Using the previous example, that would be 2.5ms). During t_{INT1}, data is clocked out of the CCD but it is not digitized by the AFE. The CCD output signal (representing line "n-1") is discarded.

After the short integration time, the clock is slowed for the next integration time (t_{INT2}). Integration for line "n+1" is done during this period. Since t_{INT2} is longer, there is more time to read out pixel data for line "n". As long as t_{INT2} corresponds to a pixel rate of 1MHz or slower, the line can be digitized and written to the DRAM.

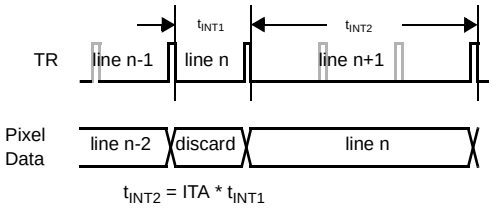


Figure 47: Integration Time Adjust Function

$t_{INT\ 1}$ is determined by the traditional calculations, primarily the MCLK divider and line end settings. $t_{INT2} = ITA * t_{INT1}$.

There are two more considerations when using the ITA. The first is CCD image lag. Image lag is a sensor phenomenon in which a percentage of the pixel voltage from the previous line appears in the pixel voltage for the current line. In the example above, some of the signal from line n-1 will leak into line n. Since the integration time for line n-1 (t_{INT2}) is 2 to 6 times longer than t_{INT1}, the leakage may be as much as 2 to 6 times the sensor specified image lag. This is usually not a problem. If it is, use a sensor with a low image lag specification, or reduce the brightness of the CCFL light source.

The second consideration is the stepsize calculation. Using the ITA's dual timebases affects the stepsize required to produce an image with the correct vertical resolution. The solution is to calculate the stepsize using the traditional formula, then multiply it by the factor (ITA+1)/ITA:

Applications Information (Continued)

$$stepsize\_ITA = stepsize \cdot \frac{ITA+1}{ITA}$$

14.0 QUESTIONS AND ANSWERS

Q Where is calibration done?
A Calibration is done on the host computer.

Q Does the LM9833 support 800dpi sensors? 400dpi? XXXdpi?
A Yes. The LM9833 will support any sensor up to a maximum of 16383 pixels x 3 colors. Available horizontal resolutions are calculated by the optical resolution of the scanner divided by the HDPI_divider.

15.0 GENERAL NOTES AND TROUBLESHOOTING TIPS

(mclk_divider)(HDPI_divider)(ITA) must be greater than or equal to 6. If this condition is not met, the LM9833 will not work.

Make sure the gamma tables are programmed with a valid gamma curve.

Make sure the multiplier gain coefficients are loaded and correct. (Remember, a gain coefficient of 0 means a GAIN of x0, not x1. If the gain coefficient = 0 the output code will always be 0.)

Remember that when the LM9833 is reset (reg08 = 0x20) or in suspend for longer than a few milliseconds (consult your DRAM datasheet), DRAM refresh will stop and the Gamma and Coefficient data may be corrupted.

Some of the CCD signals (RS, CP1, and CP2) can have a small pulse when line_end occurs. Line_end resets these signals and depending on how they are programmed to go on and off, line_end can chop off the signal before its programmed off time. This is not a problem because the truncation occurs at the end of every line, after all the image data for that line has been digitized.

Registers 4 and 5 only autowrap to 0 from their highest possible legal address. If an address higher than the highest legal address is written, it will continue to increment from the illegal address, not wrap to 0, and unknown operation may occur. This can not happen unless the host writes an illegal address to the dataport.

The absolute distance between reference sample and signal sample must be 2 MCLKs or greater, whether CDS is on or off.

The range of values for the Optical Black (registers 0F and 10), Reset Pulse (11 and 12), CP1 pulse (13 and 14), CP2 pulse (15 and 16), Reference Sample (17), and Signal Sample (18) settings depend on the rate of the pixel data coming from the sensor.

Mode	Pixel Rate	Registers 0F to 18 Range
Pixel Rate Modes	**MCLK/24**	**0 - 23**
Line Rate Modes	**MCLK/8**	**0 - 7**

Always make sure line length (data pixels end - data pixels start) is >= the horizontal divider. For example, if you are dividing by 12, the line length must be >=12.

The Line End (registers 20 and 21) setting must be programmed as follows relative to the Data Pixels End (registers 24 and 25) setting:

Line End must be >= Data Pixels End + 20

The Data Pixels Start (registers 22 and 23) setting must be >=the Active Pixels Start (registers 1E and 1F) setting.

The correct Default Phase Difference (registers 51, 52, and 53) must be set for a scan to restart properly following a pause in the scanning. See the LM9833 software for information on setting the DPD register.

The number of fullsteps skipped at the start of a scan may be one less than the Fullsteps to Skip at Start of Scan (registers 4A and 4B) setting.

The Scanning Step Size (registers 46 and 47) and Fast Feed Step Size (registers 48 and 49) settings must be > 2.

When reverse is enabled, the LM9833 always stops on Red (line rate color). When reverse is disabled, it will stop on any color.

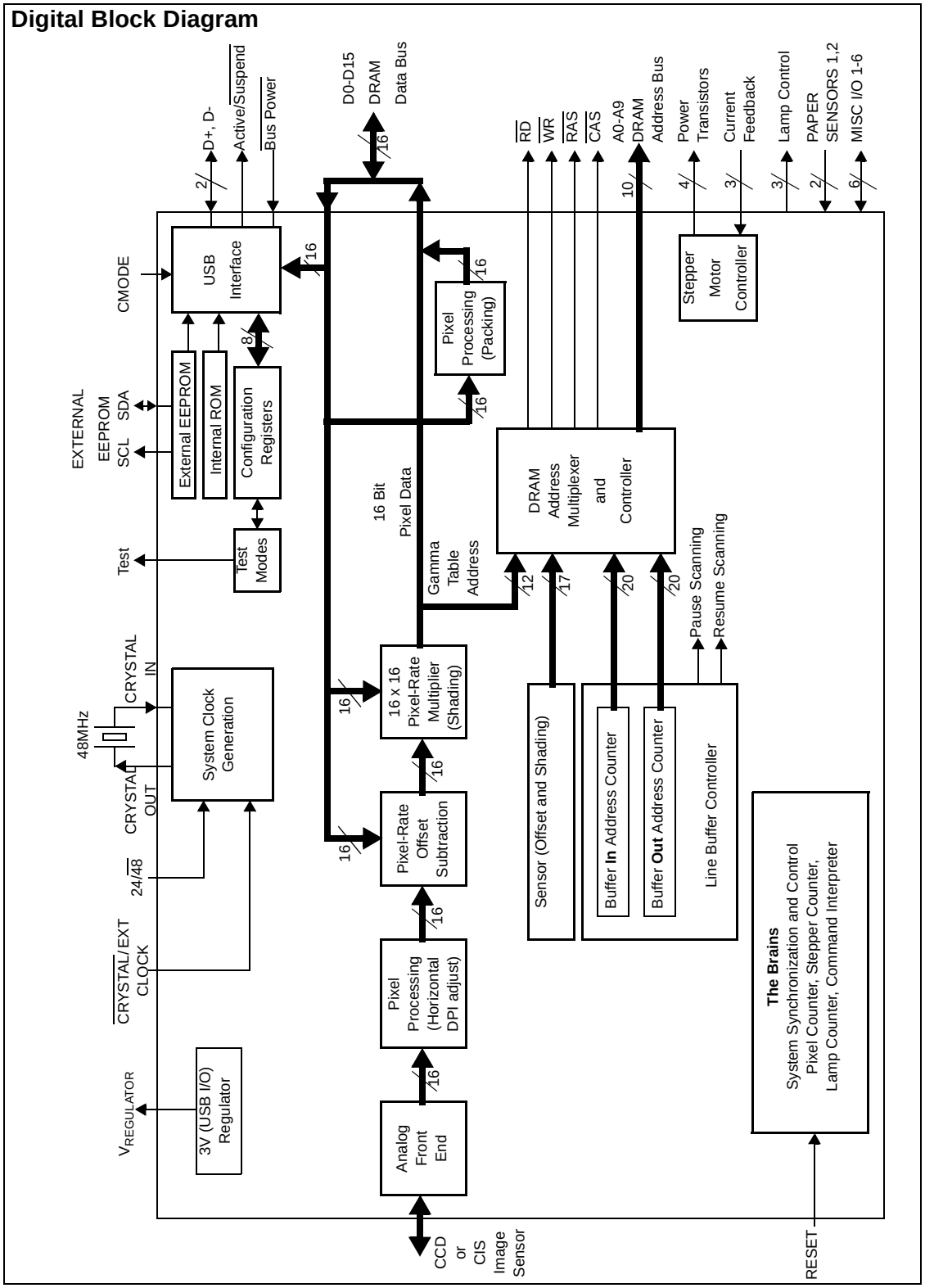
The contents of register 01 is not reset by the start of a new scan, but it is updated to the correct value after the first line has been scanned. To reset this counter prior to starting a scan, the chip can be briefly reset (register 7 = 0x20). Since resetting the chip may have undesired consequences (turning the lamp off briefly, interrupting DRAM refresh), it is also acceptable to simply wait until register 01 starts incrementing. At that point the register 01 data will be correct.

Gamma and gain/offset coefficient data should be written with reg07=0 (idle).

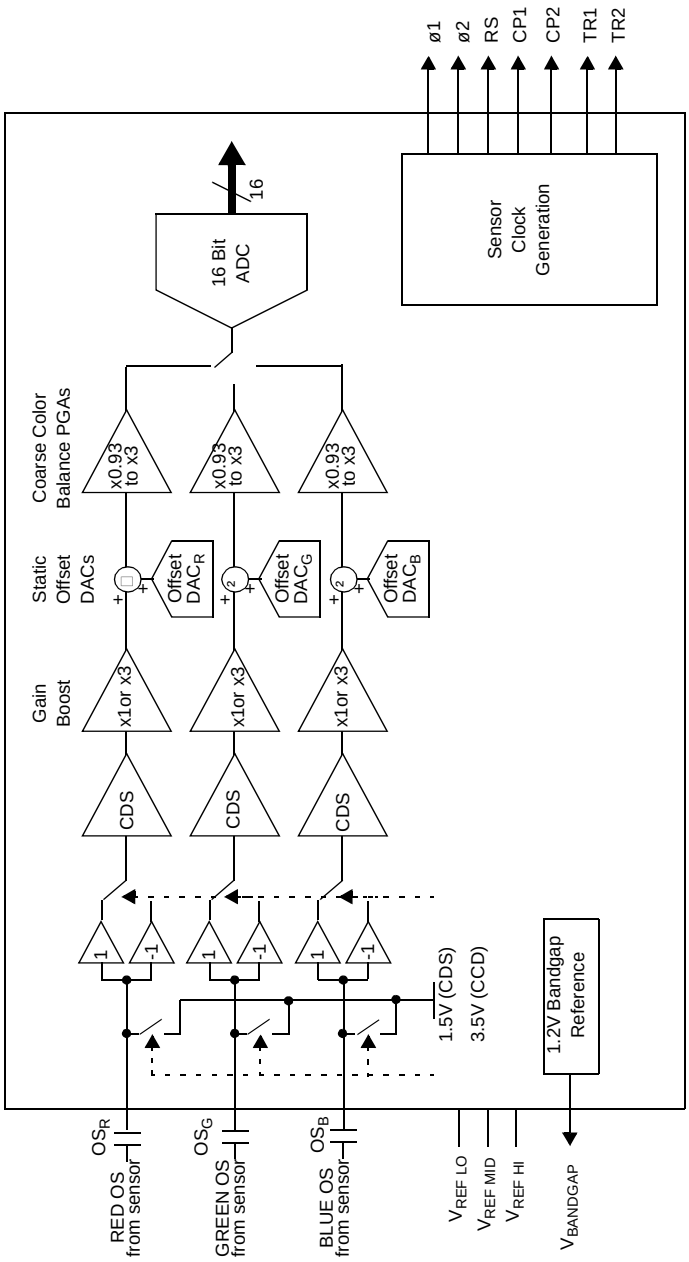
When configured to do so, changes on the Paper Sense and MISC I/O pins were supposed to generate USB Interrupts. This functionality is not working at the time of this datasheet's publication. The solution (as demonstrated in our Twain Driver software) is to poll register 02 every 200 to 500ms. This uses very little additional bandwidth compared to the USB interrupt solution.

Paper Sensor #2 Doesn't Stop Sensor When Homing: See Section *12.16*.

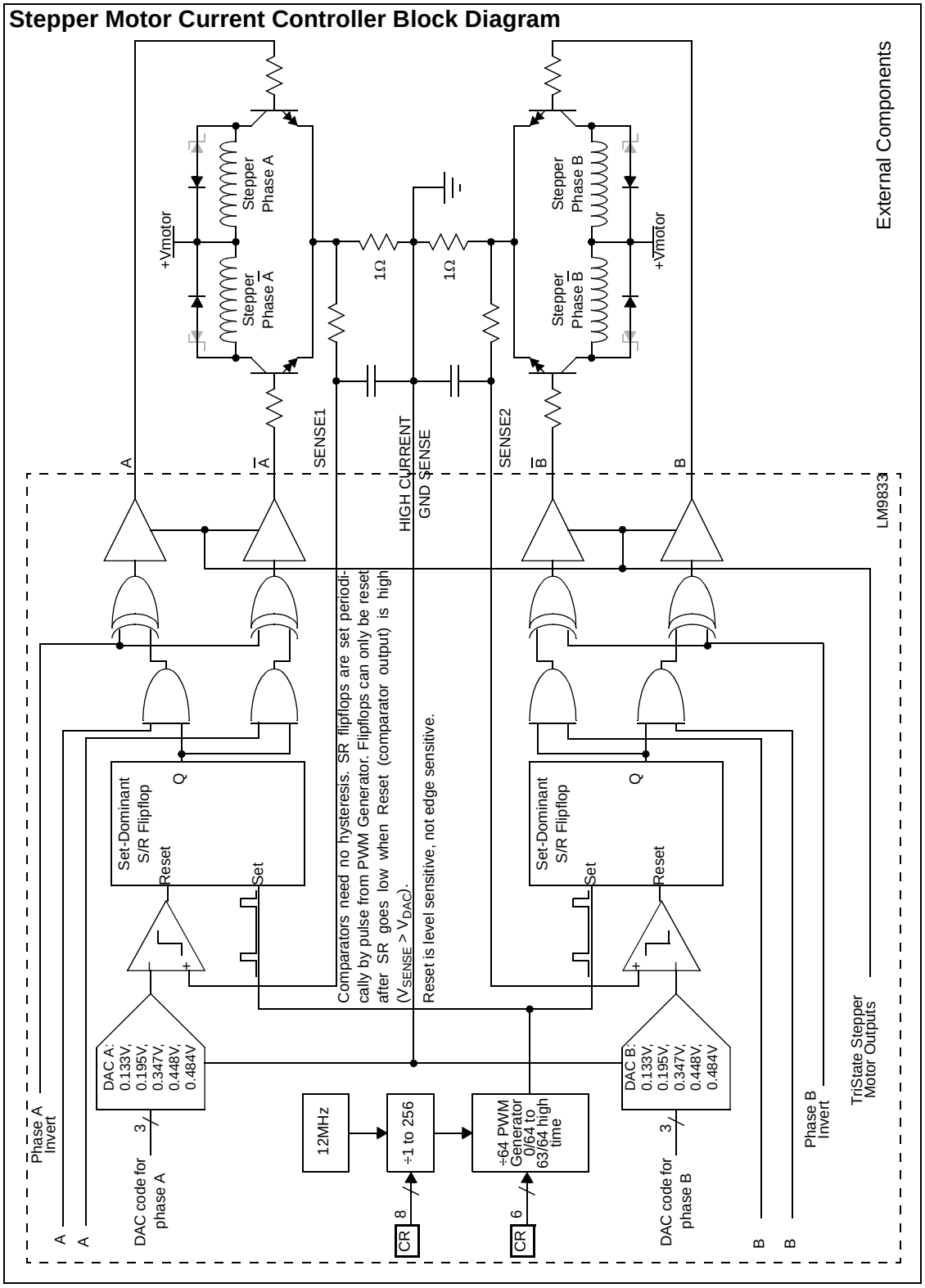
Digital Block Diagram



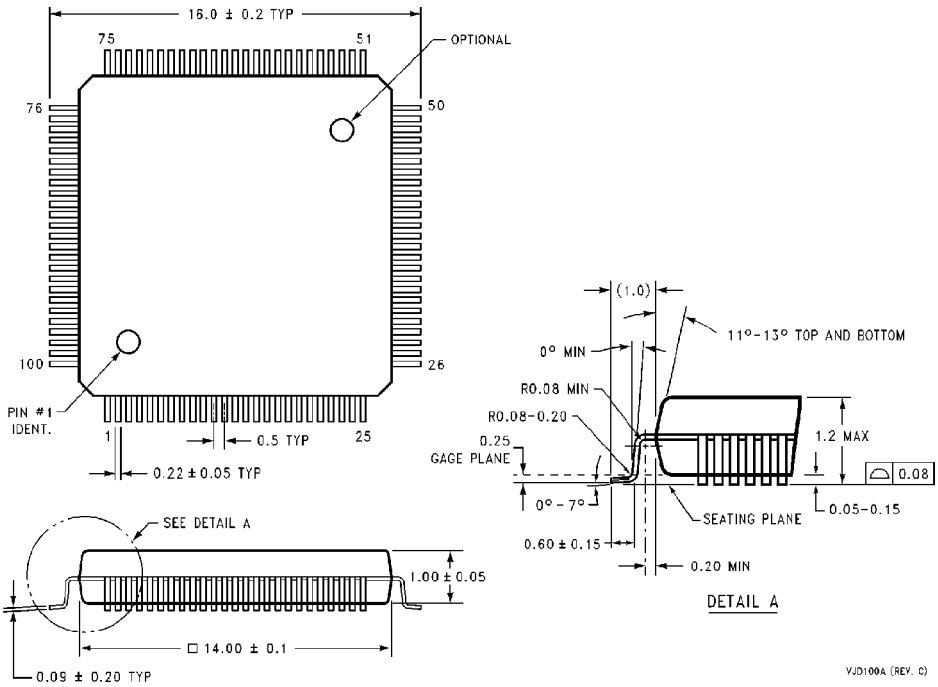
Analog Front End Block Diagram



Stepper Motor Current Controller Block Diagram



Physical Dimensions (millimeters)



100-Pin Thin Plastic Quad FlatPac (JEDEC) (TQFP)

NS Package Number VJD100A

Order Number LM9833CCVJD

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