

## LMV301

# Low Input Bias Current, 1.8V Op Amp w/ Rail-to-Rail Output

### General Description

The LMV301 CMOS operational amplifier is ideal for single supply, low voltage operation with a guaranteed operating voltage range from 1.8V to 5V. The low input bias current of less than 0.182pA typical, eliminates input voltage errors that may originate from small input signals. This makes the LMV301 ideal for electrometer applications requiring low input leakage such as sensitive photodetection transimpedance amplifiers and sensor amplifiers. The LMV301 also features a rail-to-rail output voltage swing in addition to an input common-mode range that includes ground. The LMV301 will drive a 600Ω resistive load and up to 1000pF capacitive load in unity gain follower applications. The low supply voltage also makes the LMV301 well suited for portable two-cell battery systems and single cell Li-Ion systems.

The LMV301 exhibits excellent speed-power ratio, achieving 1MHz at unity gain with low supply current. The high DC gain of 100dB makes it ideal for other low frequency applications.

The LMV301 is offered in a space saving SC-70 package, which is only 2.0X2.1X1.0mm. It is also similar to the LMV321 except the LMV301 has a CMOS input.

### Key Specifications

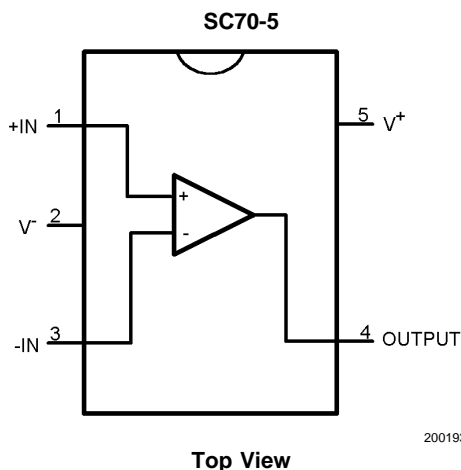
(Typical values unless otherwise specified)

■ Input bias current	0.182pA
■ Gain bandwidth product	1MHz
■ Supply voltage @ 1.8V	1.8V to 5V
■ Supply current	150μA
■ Input referred voltage noise @ 1kHz	40nV/√Hz
■ DC Gain (600Ω load)	100dB
■ Output voltage range @ 1.8V	0.024 to 1.77V
■ Input common-mode voltage range	-0.3V to V <sup>+</sup> - 1.2V

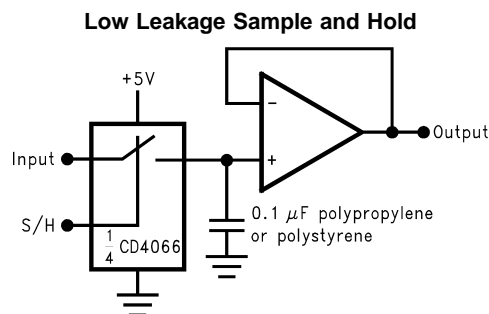
### Applications

- Thermocouple amplifiers
- Photo current amplifiers
- Transducer amplifiers
- Sample and hold circuits
- Low frequency active filters

### Connection Diagram



### Applications Circuit



### Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SC70-5	LMV301MG	A48	1k Units Tape and Reel	MAA05A
	LMV301MGX		3k Units Tape and Reel	

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 7)

Machine Model 200V

Human Body Model 2000V

Differential Input Voltage  $\pm$ Supply VoltageSupply Voltage ( $V^+ - V^-$ ) 5.5VOutput Short Circuit to  $V^+$  (Note 2)Output Short Circuit to  $V^-$  (Note 2)Storage Temperature Range  $-65^\circ\text{C}$  to  $150^\circ\text{C}$ 

Mounting Temperature

Infrared or Convection (20 sec)  $235^\circ\text{C}$ Junction Temperature (Note 3)  $150^\circ\text{C}$ **Operating Ratings**(Note 1)

Supply Voltage 1.8V to 5.0V

Temperature Range  $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ Thermal Resistance ( $\theta_{JA}$ )

Ultra Tiny SC70-5 Package

5-pin Surface Mount  $478^\circ\text{C/W}$ 

**1.8V DC Electrical Characteristics** Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 1.8\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$ , and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
$V_{OS}$	Input Offset Voltage	$V_{CM} = 0.4\text{V}$ , $V^+ = 1.3\text{V}$ , $V^- = -0.5\text{V}$		0.9	8 <b>9</b>	mV
$I_B$	Input Bias Current			0.182	35 <b>50</b>	pA
$I_S$	Supply Current	$V_{CM} = 0.4\text{V}$ , $V^+ = 1.3\text{V}$ , $V^- = -0.5\text{V}$		150	250 <b>275</b>	$\mu\text{A}$
CMRR	Common Mode Rejection Ratio	$0.3\text{V} \leq V_{CM} \leq 0.9\text{V}$	62 <b>60</b>	108		dB
PSRR	Power Supply Rejection Ratio	$1.8\text{V} \leq V^+ \leq 5\text{V}$ , $0.9 \leq V_{CM} \leq 2.5\text{V}$	67 <b>62</b>	110		dB
$V_{CM}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{dB}$	-0.3 <b>0</b>		0.6	V
$A_V$	Large Signal Voltage Gain Sourcing	$R_L = 600\Omega$ to $0\text{V}$ , $V^+ = 1.2\text{V}$ , $V^- = -0.6\text{V}$ , $V_O = -0.2\text{V}$ to $0.8\text{V}$ , $V_{CM} = 0\text{V}$	80 <b>75</b>	119		dB
		$R_L = 2\text{k}\Omega$ to $0\text{V}$ , $V^+ = 1.2\text{V}$ , $V^- = -0.6\text{V}$ , $V_O = -0.2\text{V}$ to $0.8\text{V}$ , $V_{CM} = 0\text{V}$	80 <b>75</b>	111		
	Sinking	$R_L = 600\Omega$ to $0\text{V}$ , $V^+ = 1.2\text{V}$ , $V^- = -0.6\text{V}$ , $V_O = -0.2\text{V}$ to $0.8\text{V}$ , $V_{CM} = 0\text{V}$	80 <b>75</b>	94		dB
		$R_L = 2\text{k}\Omega$ to $0\text{V}$ , $V^+ = 1.2\text{V}$ , $V^- = -0.6\text{V}$ , $V_O = -0.2\text{V}$ to $0.8\text{V}$ , $V_{CM} = 0\text{V}$	80 <b>75</b>	96		
$V_O$	Output Swing	$R_L = 600\Omega$ to $0.9\text{V}$ $V_{IN} = \pm 100\text{mV}$	$V_{OH}$	1.65 <b>1.63</b>		V
			$V_{OL}$		0.074	V
		$R_L = 2\text{k}\Omega$ to $0.9\text{V}$ $V_{IN} = \pm 100\text{mV}$	$V_{OH}$	1.75 <b>1.74</b>		V
			$V_{OL}$		0.024 <b>0.040</b>	V
$I_O$	Output Short Circuit Current	Sourcing, $V_O = 0\text{V}$ , $V_{IN} = 100\text{mV}$	4 <b>3.3</b>	8.4		mA
		Sinking, $V_O = 1.8\text{V}$ , $V_{IN} = -100\text{mV}$	7	9.8		mA

## 1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 1.8\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$ , and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 4)	Units
SR	Slew Rate	(Note 6)	0.57	V/ $\mu\text{s}$
GBW	Gain Bandwidth Product		1	MHz
$\phi_m$	Phase Margin		60	Deg
$G_m$	Gain Margin		10	dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{kHz}$ , $V_{CM} = 0.5\text{V}$ $f = 100\text{kHz}$	40 30	nV/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$ , $A_V = +1$ $R_L = 600\text{k}\Omega$ , $V_{IN} = 1V_{PP}$	0.089	%

## 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$ , and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units	
V <sub>OS</sub>	Input Offset Voltage	V <sub>CM</sub> = 0.35V, V <sup>+</sup> = 1.7V, V <sup>-</sup> = -1V		0.9	8 9	mV	
I <sub>B</sub>	Input Bias Current			0.182	35 50	pA	
I <sub>S</sub>	Supply Current	V <sub>CM</sub> = 0.35V, V <sup>+</sup> = 1.7V, V <sup>-</sup> = -1V		153	250 275	μA	
CMRR	Common Mode Rejection Ratio	-0.15V ≤ V <sub>CM</sub> ≤ 1.35V	62 60	115		dB	
PSRR	Power Supply Rejection Ratio	1.8V ≤ V <sub>+</sub> ≤ 5V	67 62	110		dB	
V <sub>CM</sub>	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3 0		1.5	V	
A <sub>V</sub>	Large Signal Voltage Gain Sourcing	R <sub>L</sub> = 600Ω to 0V, V <sup>+</sup> = 1.35V, V <sup>-</sup> = -1.35V, V <sub>O</sub> = -1V to 1V, V <sub>CM</sub> = 0V	80 75	100		dB	
		R <sub>L</sub> = 2kΩ to 0V, V <sup>+</sup> = 1.35V, V <sup>-</sup> = -1.35V, V <sub>O</sub> = -1V to 1V, V <sub>CM</sub> = 0V	83 77	114			
	Sinking	R <sub>L</sub> = 600Ω to 0V, V <sup>+</sup> = 1.35V, V <sup>-</sup> = -1.35V, V <sub>O</sub> = -1V to 1V, V <sub>CM</sub> = 0V	80 75	98		dB	
		R <sub>L</sub> = 2kΩ to 0V, V <sup>+</sup> = 1.35V, V <sup>-</sup> = -1.35V, V <sub>O</sub> = -1V to 1V, V <sub>CM</sub> = 0V	80 75	99			
V <sub>O</sub>	Output Swing	R <sub>L</sub> = 600Ω to 1.35V V <sub>IN</sub> = ±100mV	V <sub>OH</sub>	2.550 2.530	2.62		V
			V <sub>OL</sub>		0.078	0.100	V
		R <sub>L</sub> = 2kΩ to 1.35V V <sub>IN</sub> = ±100mV	V <sub>OH</sub>	2.650 2.640	2.675		V
			V <sub>OL</sub>		0.024	0.045	V
I <sub>O</sub>	Output Short Circuit Current	Sourcing, V <sub>O</sub> = 0V, V <sub>IN</sub> = 100mV	20 15	32		mA	
		Sinking, V <sub>O</sub> = 2.7V, V <sub>IN</sub> = -100mV	19 12	24		mA	

## 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 4)	Units
SR	Slew Rate	(Note 6)	0.60	V/ $\mu\text{s}$
GBW	Gain Bandwidth Product		1	MHz
$\phi_m$	Phase Margin		65	Deg
$G_m$	Gain Margin		10	dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{kHz}$ , $V_{CM} = 0.5\text{V}$ $f = 100\text{kHz}$	40 30	nV/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$ , $A_V = +1$ $R_L = 600\text{k}\Omega$ , $V_{IN} = 1V_{PP}$	0.077	%

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$ , and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units	
V <sub>OS</sub>	Input Offset Voltage	V <sub>CM</sub> = 0.5V, V <sup>+</sup> = 3V, V <sup>-</sup> = -2V		0.9	8 9	mV	
I <sub>B</sub>	Input Bias Current			0.182	35 50	pA	
I <sub>S</sub>	Supply Current	V <sub>CM</sub> = 0.5V, V <sup>+</sup> = 3V, V <sup>-</sup> = -2V		163	260 285	μA	
CMRR	Common Mode Rejection Ratio	-1.3V ≤ V <sub>CM</sub> ≤ 2.5V	62 61	111		dB	
PSRR	Power Supply Rejection Ratio	1.8V ≤ V <sup>+</sup> ≤ 5V	67 62	110		dB	
V <sub>CM</sub>	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3 0		3.8	V	
A <sub>V</sub>	Large Signal Voltage Gain Sourcing	R <sub>L</sub> = 600Ω to 0V, V <sup>+</sup> = 2.5V, V <sup>-</sup> = -2.5V, V <sub>O</sub> = -2V to 2V, V <sub>CM</sub> = 0V	86 82	117		dB	
		R <sub>L</sub> = 2kΩ to 0V, V <sup>+</sup> = 2.5V, V <sup>-</sup> = -2.5V, V <sub>O</sub> = -2V to 2V, V <sub>CM</sub> = 0V	89 85	116			
	Sinking	R <sub>L</sub> = 600Ω to 0V, V <sup>+</sup> = 2.5V, V <sup>-</sup> = -2.5V, V <sub>O</sub> = -2V to 2V, V <sub>CM</sub> = 0V	80 75	105		dB	
		R <sub>L</sub> = 2kΩ to 0V, V <sup>+</sup> = 2.5V, V <sup>-</sup> = -2.5V, V <sub>O</sub> = -2V to 2V, V <sub>CM</sub> = 0V	80 75	107			
V <sub>O</sub>	Output Swing	R <sub>L</sub> = 600Ω to 2.5V V <sub>IN</sub> = ±100mV	V <sub>OH</sub>	4.850 4.840	4.893		V
			V <sub>OL</sub>		0.1	0.150 1.160	V
		R <sub>L</sub> = 2kΩ to 2.5V V <sub>IN</sub> = ±100mV	V <sub>OH</sub>	4.935	4.966		V
			V <sub>OL</sub>		0.034	0.065 0.075	V
I <sub>O</sub>	Output Short Circuit Current	Sourcing, V <sub>O</sub> = 0V, V <sub>IN</sub> = 100mV	85 68	108		mA	
		Sinking, V <sub>O</sub> = 5V, V <sub>IN</sub> = -100mV	60 45	69		mA	

**5V AC Electrical Characteristics**

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 4)	Units
SR	Slew Rate	(Note 6)	0.66	V/ $\mu\text{s}$
GBW	Gain Bandwidth Product		1	MHz
$\phi_m$	Phase Margin		70	Deg
$G_m$	Gain Margin		15	dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{kHz}$ , $V_{CM} = 1\text{V}$ $f = 100\text{kHz}$	40 30	nV/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$ , $A_V = +1$ $R_L = 600\Omega$ , $V_O = 1V_{PP}$	0.069	%

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Note 2:** Applies to both single supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ . Output currents in excess of 45mA over long term may adversely affect reliability.

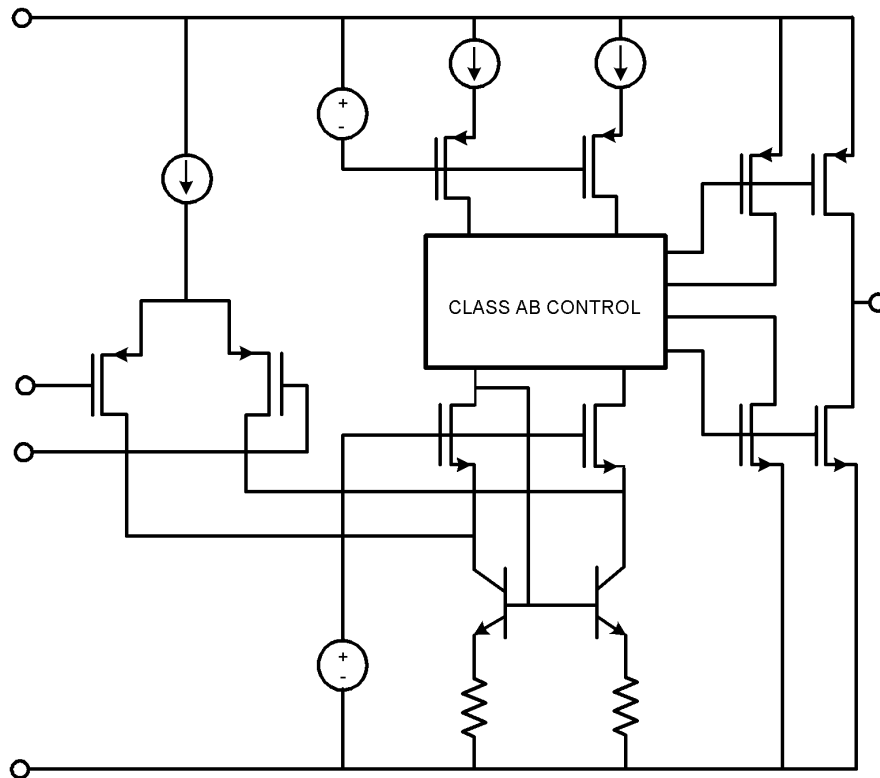
**Note 3:** The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A)\theta_{JA}$ . All numbers apply for packages soldered directly into a PC board.

**Note 4:** Typical value represent the most likely parametric norm.

**Note 5:** All limits are guaranteed by testing or statistical analysis.

**Note 6:**  $V^+ = 5\text{V}$ . Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

**Note 7:** Human body model, 1.5k $\Omega$  in series with 100pF. Machine model, 200 $\Omega$  in series with 100pF.

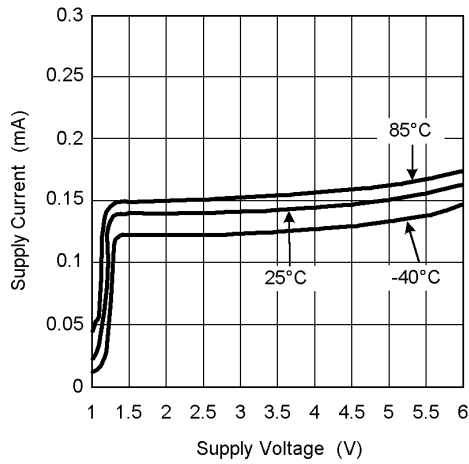
**Simplified Schematic**

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# Typical Performance Characteristics

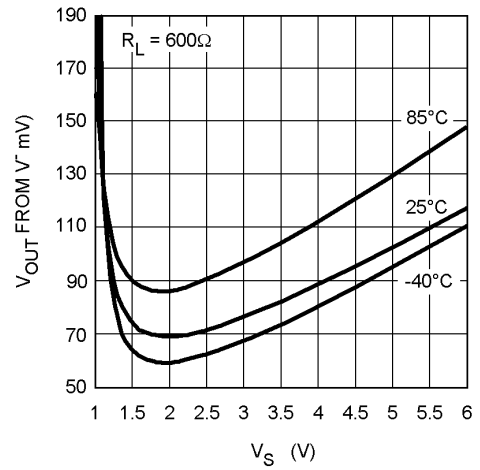
Unless otherwise specified,  $T_A = 25^\circ\text{C}$ .

Supply Current vs. Supply Voltage



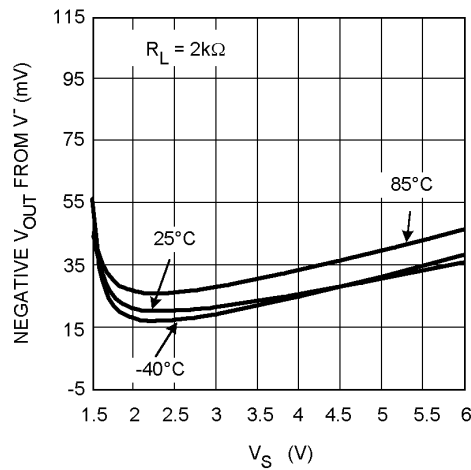
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Output Negative Swing vs. Supply Voltage



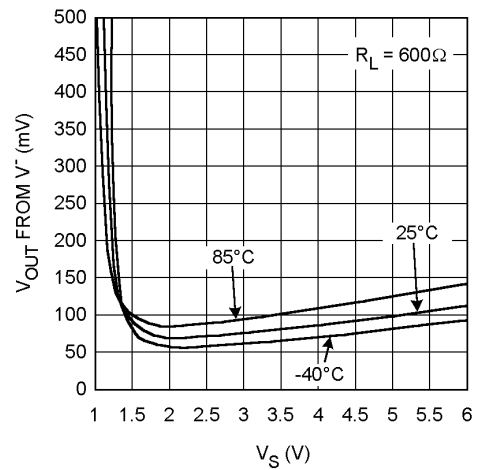
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Output Negative Swing vs. Supply Voltage



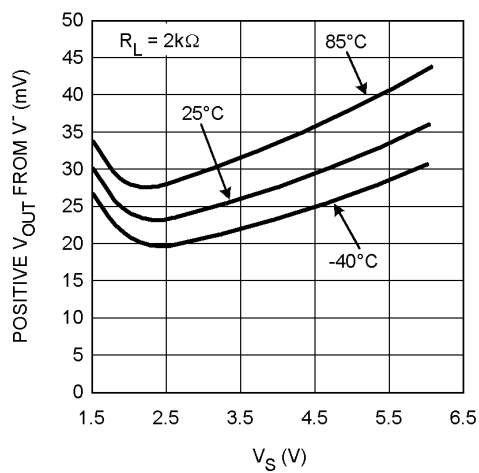
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Output Positive Swing vs. Supply Voltage



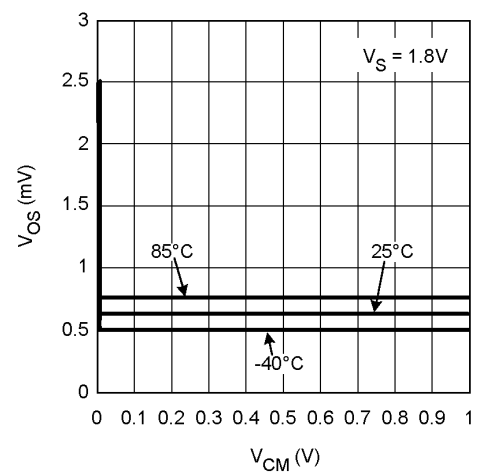
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Output Positive Swing vs. Supply Voltage



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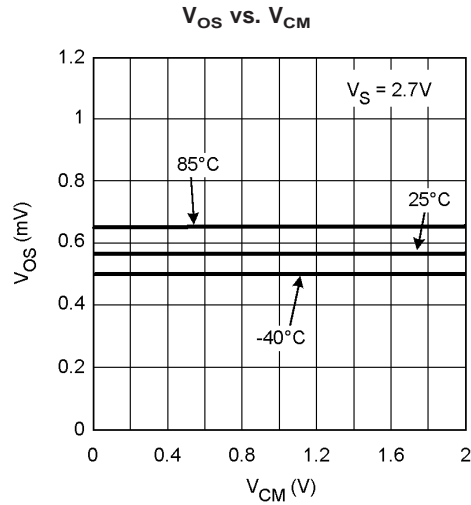
$V_{OS}$  vs.  $V_{CM}$



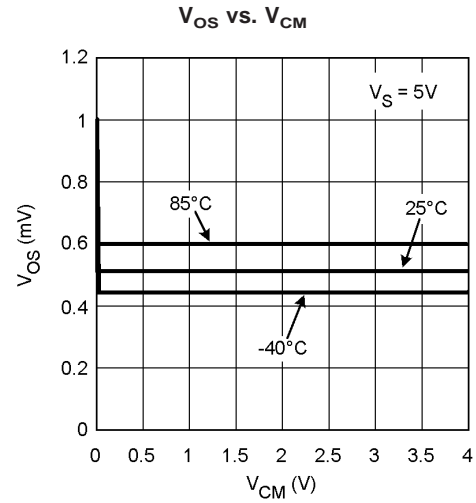
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# Typical Performance Characteristics

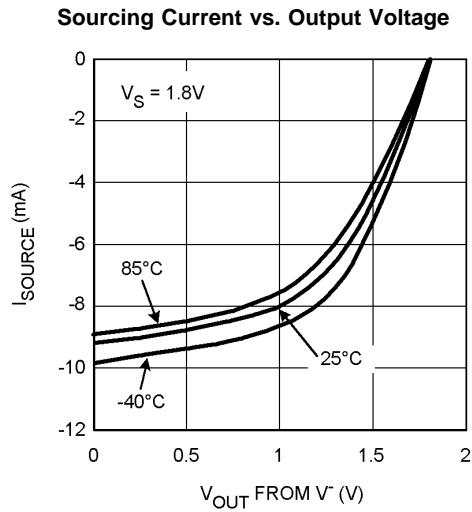
Unless otherwise specified,  $T_A = 25^\circ\text{C}$ . (Continued)



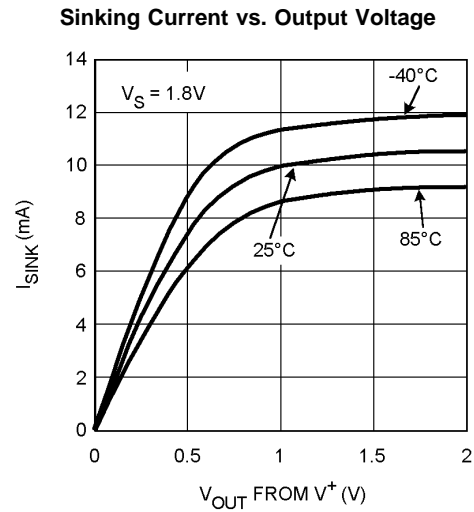
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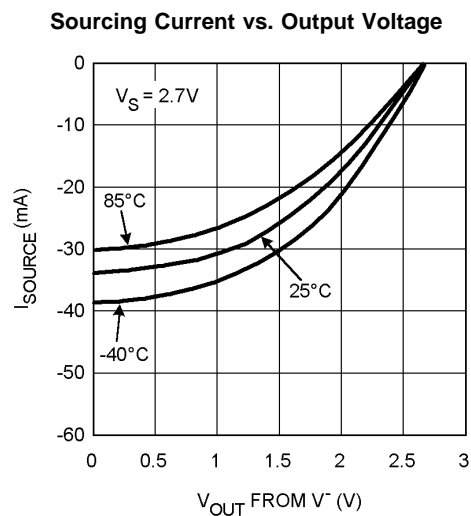
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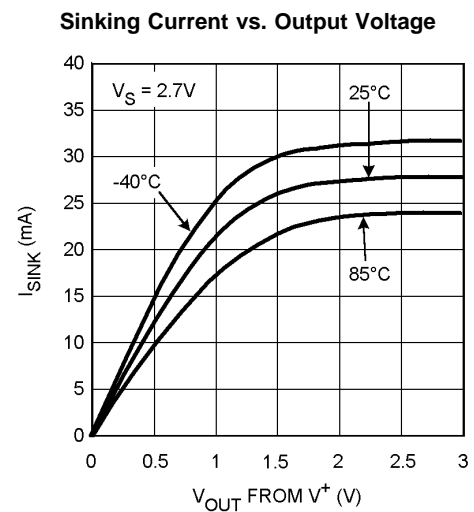
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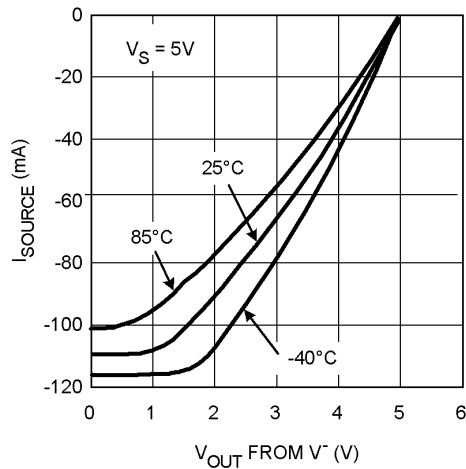


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# Typical Performance Characteristics

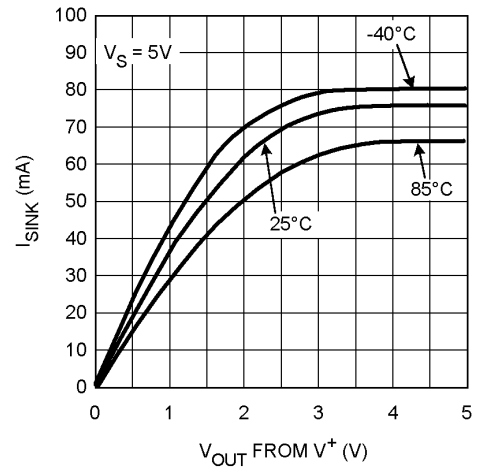
Unless otherwise specified,  $T_A = 25^\circ\text{C}$ . (Continued)

Sourcing Current vs. Output Voltage



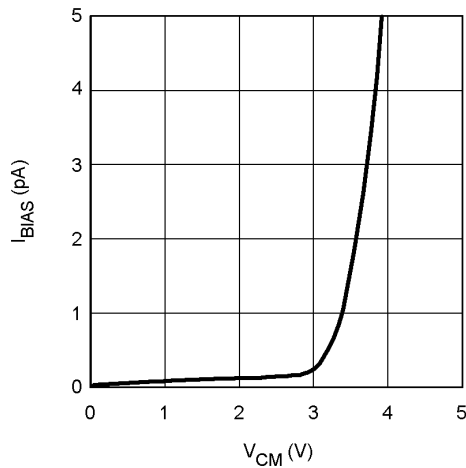
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Sinking Current vs. Output Voltage



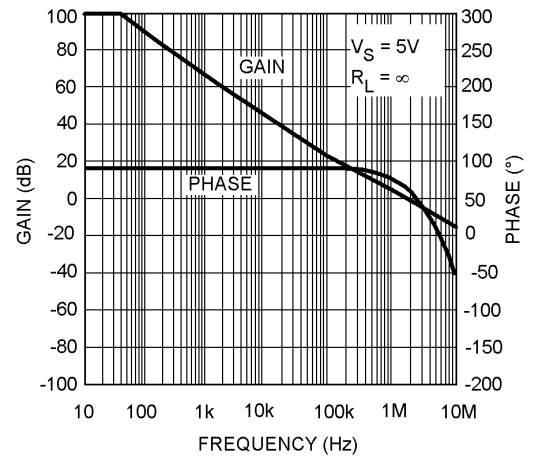
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$I_{\text{BIAS}}$  Current vs.  $V_{\text{CM}}$



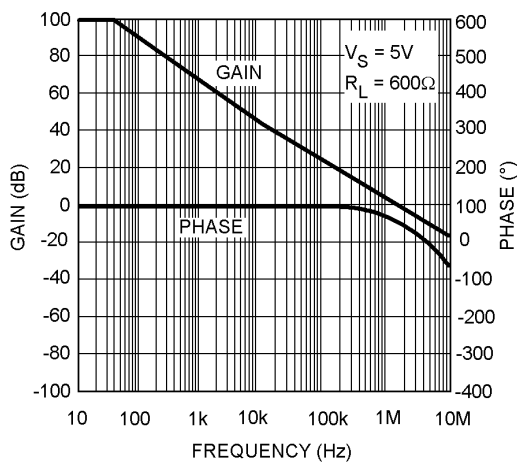
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Open Loop Frequency Response



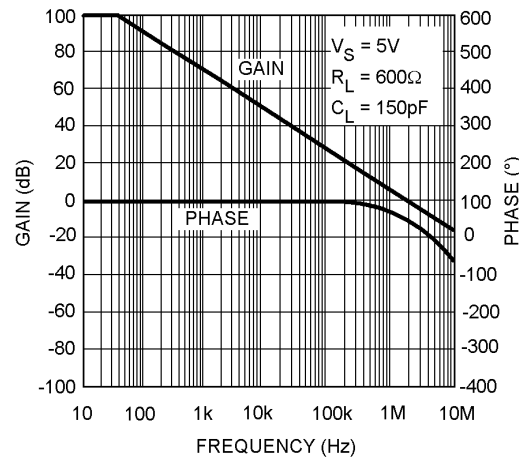
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Open Loop Frequency Response



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Open Loop Frequency Response



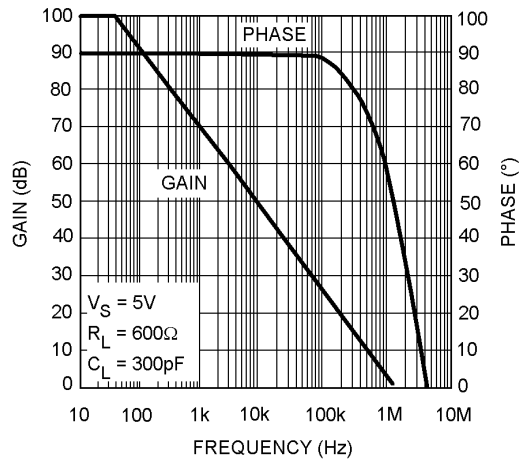
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# Typical Performance Characteristics

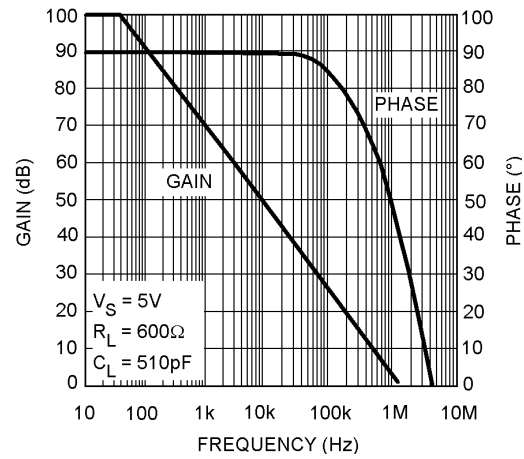
Unless otherwise specified,  $T_A = 25^\circ\text{C}$ . (Continued)

Open Loop Frequency Response



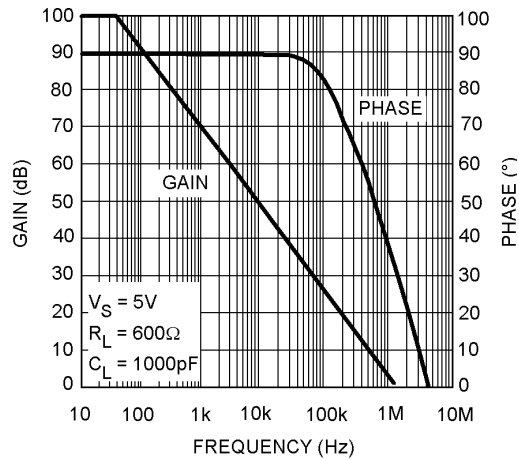
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Open Loop Frequency Response



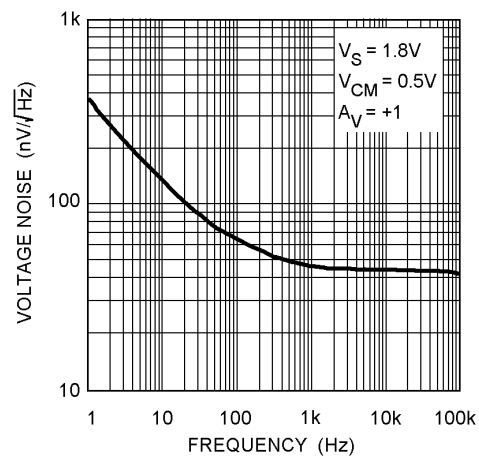
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Open Loop Frequency Response



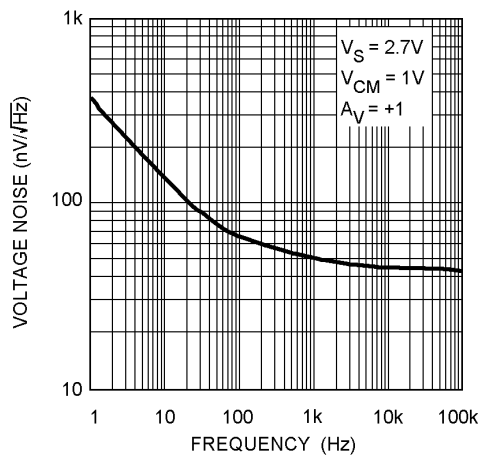
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Noise vs. Frequency Response



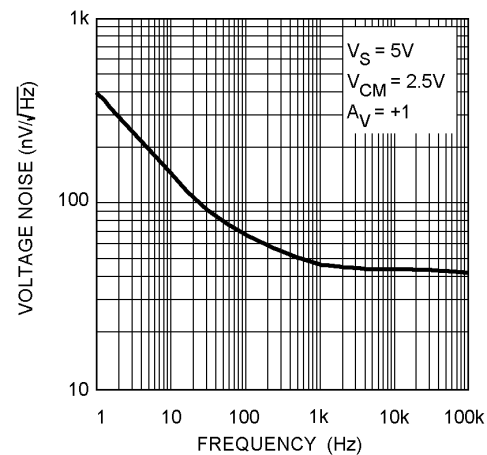
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Noise vs. Frequency Response



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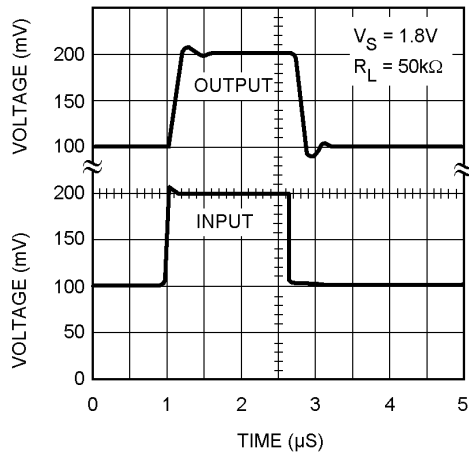
Noise vs. Frequency Response



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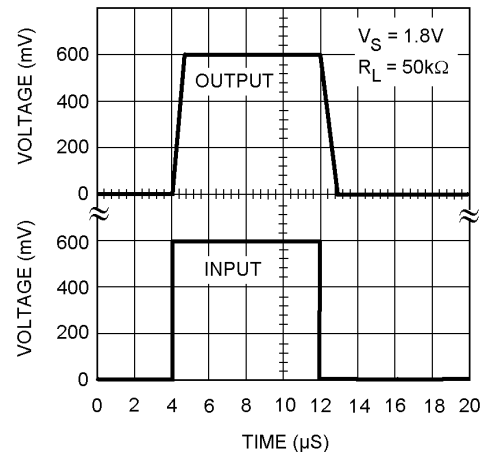
# Typical Performance Characteristics Unless otherwise specified, $T_A = 25^\circ\text{C}$ . (Continued)

Small Signal Response



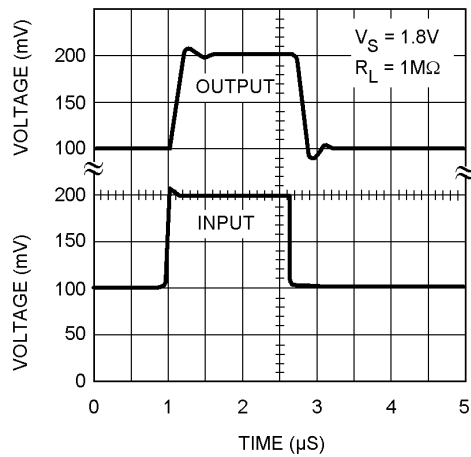
20019345

Large Signal Response



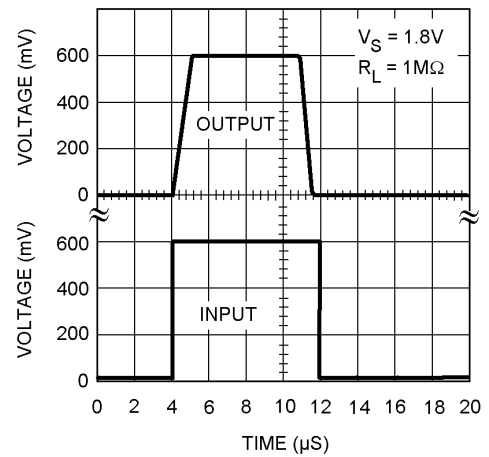
20019346

Small Signal Response



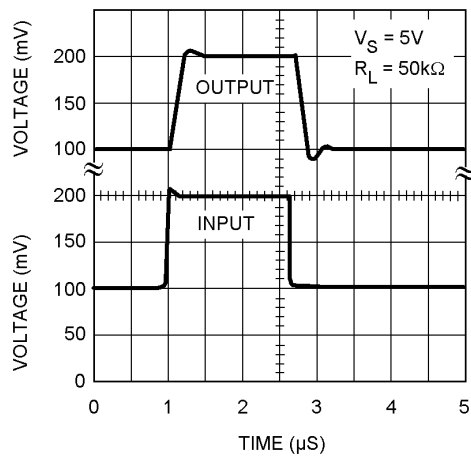
20019347

Large Signal Response



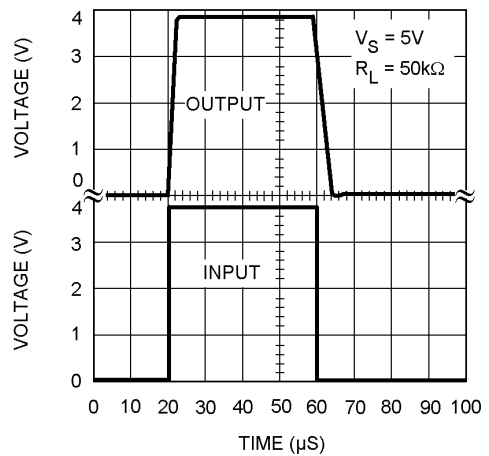
20019348

Small Signal Response



20019349

Large Signal Response

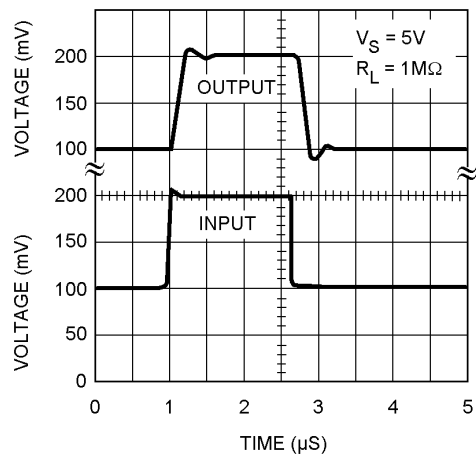


20019350

# Typical Performance Characteristics

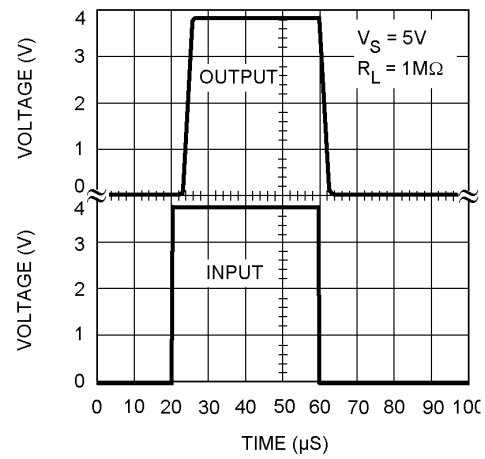
Unless otherwise specified,  $T_A = 25^\circ\text{C}$ . (Continued)

Small Signal Response



20019352

Large Signal Response



20019351

## Application Hints

### Compensating Input Capacitance

The high input resistance of the LMV301 op amp allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, *Figure 1*, the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P}$$

where  $C_S$  is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and  $R_P$  is the parallel combination of  $R_F$  and  $R_{IN}$ . This formula, as well as all formulae derived below, apply to inverting and non-inverting op amp configurations.

When the feedback resistors are smaller than a few k $\Omega$ , the frequency of the feedback pole will be quite high, since  $C_S$  is generally less than 10pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of  $C_S$ ), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" -3dB frequency, a feedback capacitor,  $C_F$ , should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low frequency noise gain. To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times \text{GBW} \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{\text{GBW} \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

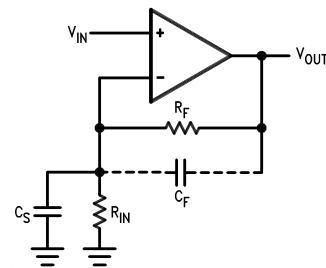
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{\text{GBW} \times R_F \times C_S}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{\text{GBW} \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$



20019306

$C_S$  consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket.  $C_F$  compensates for the pole caused by  $C_S$  and the feedback resistors.

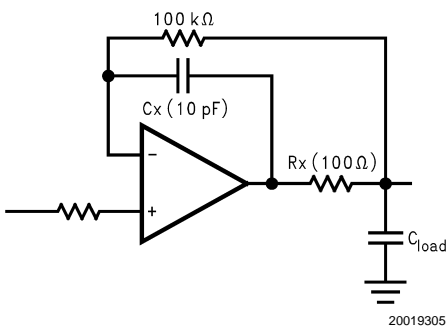
**FIGURE 1. General Operational Amplifier Circuit**

Using the smaller capacitor will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for  $C_F$  may be different from the one estimated using the breadboard. In most cases, the values of  $C_F$  should be checked on the actual circuit, starting with the computed value.

## Application Hints (Continued)

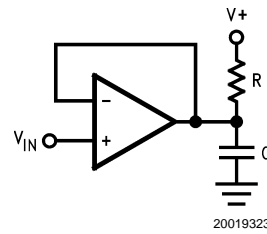
### Capacitive Load Tolerance

Like many other op amps, the LMV301 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity gain follower. The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable. As shown in *Figure 2*, the addition of a small resistor ( $50\Omega$  to  $100\Omega$ ) in series with the op amp's output, and a capacitor ( $5\text{pF}$  to  $10\text{pF}$ ) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



**FIGURE 2. Rx, Cx Improve Capacitive Load Tolerance**

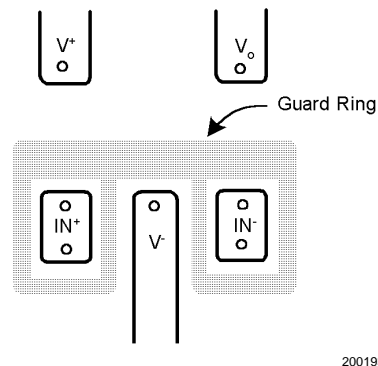
Capacitive load driving capability is enhanced by using a pull up resistor to  $V^+$  (*Figure 3*). Typically a pull up resistor conducting  $500\mu\text{A}$  or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor.



**FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor**

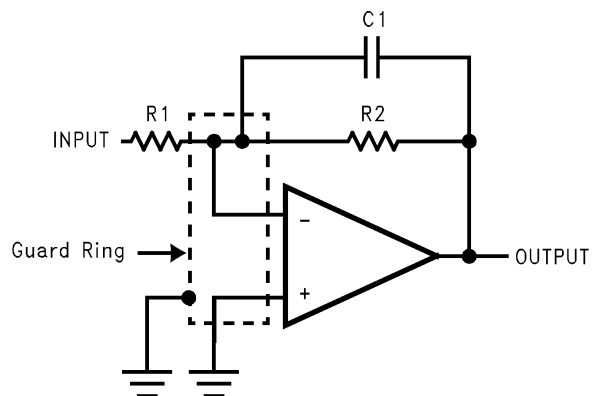
### PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than  $100\text{pA}$  of leakage current requires special layout of the PC board. When one wishes to take advantage of the low bias current of the LMV301, typically less than  $0.182\text{pA}$ , it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptable low, because under conditions of the high humidity or dust or contamination, the surface leakage will be appreciable. To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMV301's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. The PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of  $10^{12}\Omega$ , which is normally considered a very large resistance, could leak  $5\text{pA}$  if the trace were a  $5\text{V}$  bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMV301's actual performance. However, if a guard ring is held within  $5\text{mV}$  of the inputs, then even a resistance of  $10^{11}\Omega$  would cause only  $0.05\text{pA}$  of leakage current, or perhaps a minor (2:1) degradation of the amplifier performance. See *Figure 5a*, *Figure 5b*, *Figure 5c* for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d*.



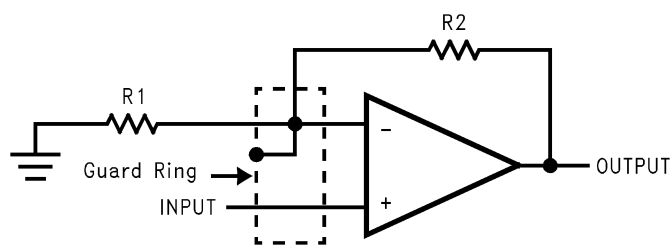
**FIGURE 4. Example, using the LMV301, of Guard Ring in P.C. Board Layout**

# Application Hints (Continued)



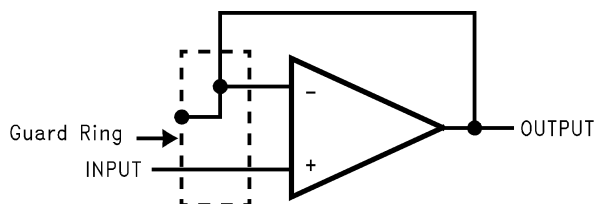
20019317

(a) Inverting Amplifier



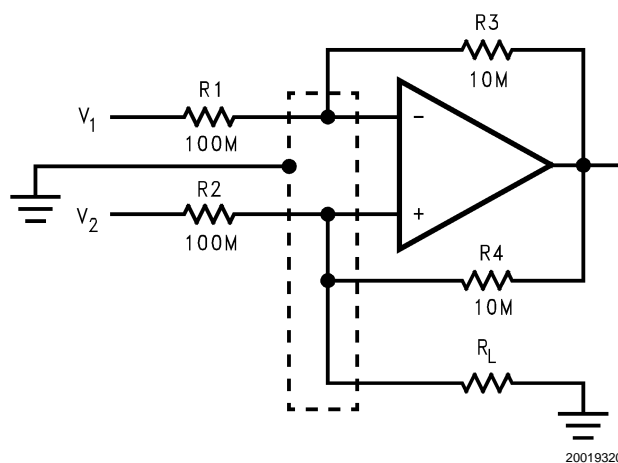
20019318

(b) Non-Inverting Amplifier



20019319

(c) Follower



20019320

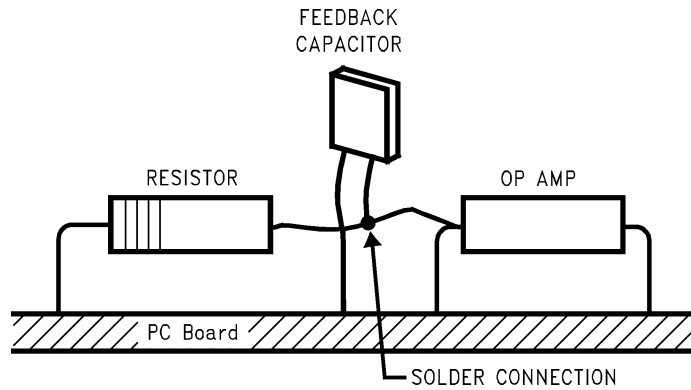
(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

## Application Hints (Continued)

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an

insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*



20019321

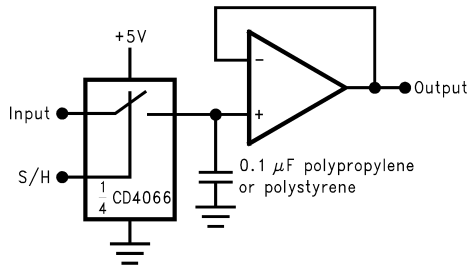
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

**FIGURE 6. Air Wiring**

## Typical Single-Supply Applications

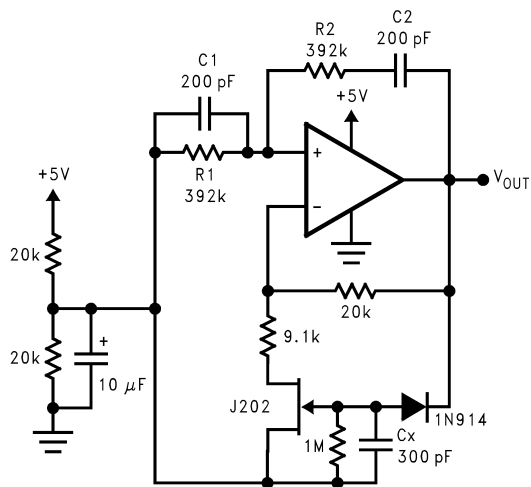
( $V_+ = 5.0$  VDC)

### Low-Leakage Sample-and-Hold



20019307

### Sine-Wave Oscillator



20019309

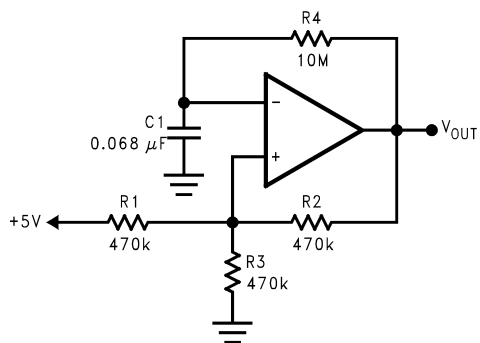
Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{osc} = 1/2\pi RC$ , where  $R = R1 = R2$  and

$C = C1 = C2$ .

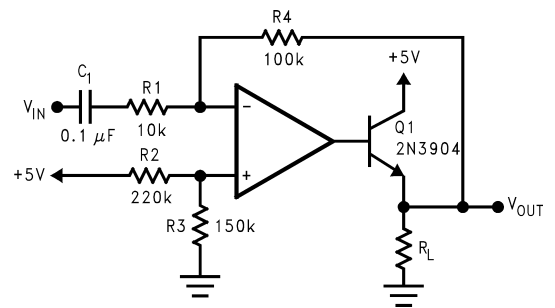
This circuit, as shown, oscillates at 2.0kHz with a peak-to-peak output swing of 4.5V.

### 1 Hz Square-Wave Oscillator



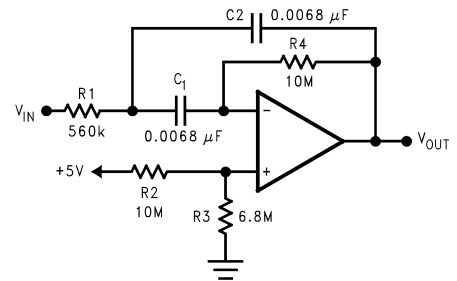
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### Power Amplifier



20019311

### 10Hz Bandpass Filter



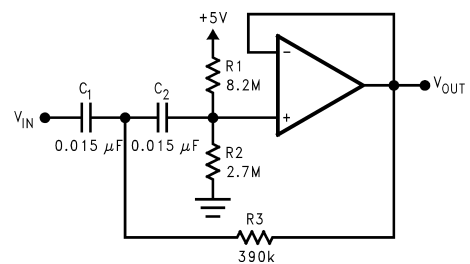
20019312

$f_0 = 10$  Hz

$Q = 2.1$

Gain = -8.8

### 10 Hz High-Pass Filter



20019313

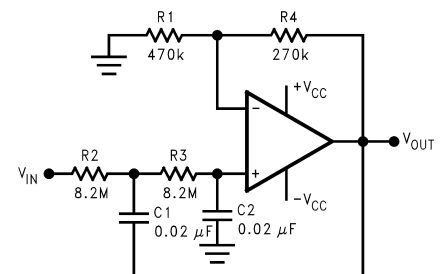
$f_c = 10$  Hz

$d = 0.895$

Gain = 1

2 dB passband ripple

### 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



20019314

$f_c = 1$  Hz

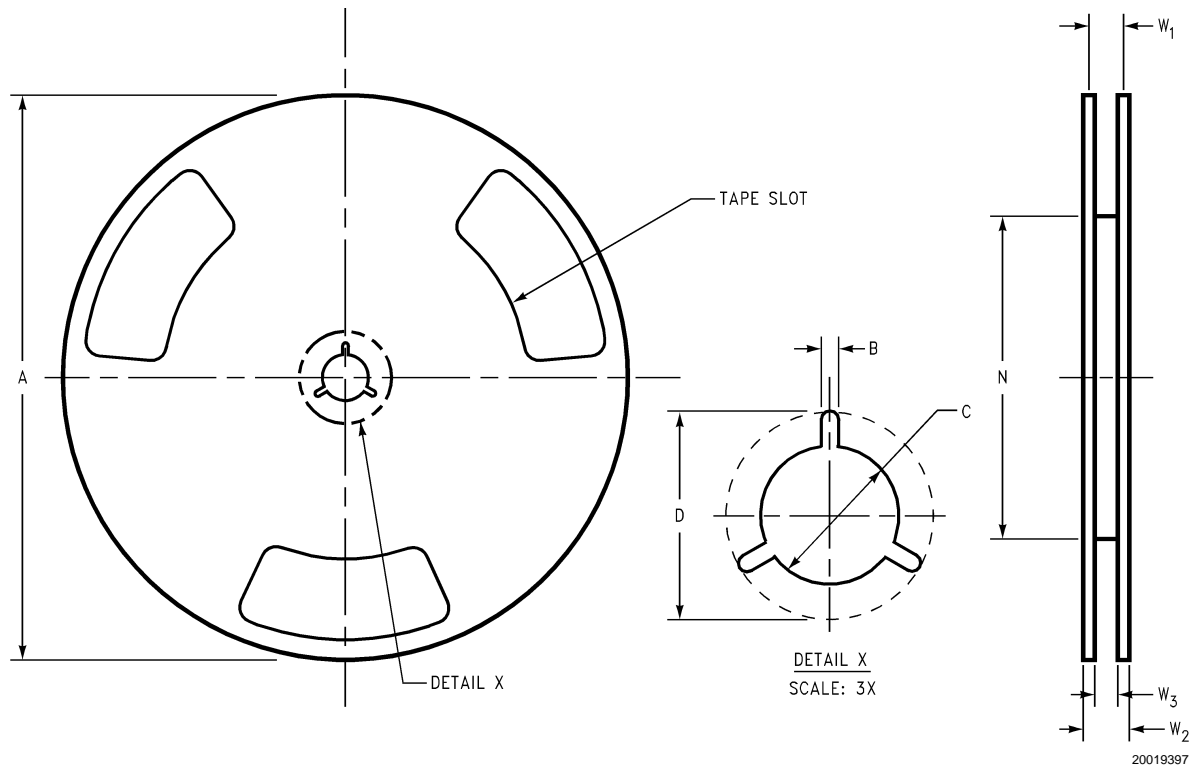
$d = 1.414$

Gain = 1.57





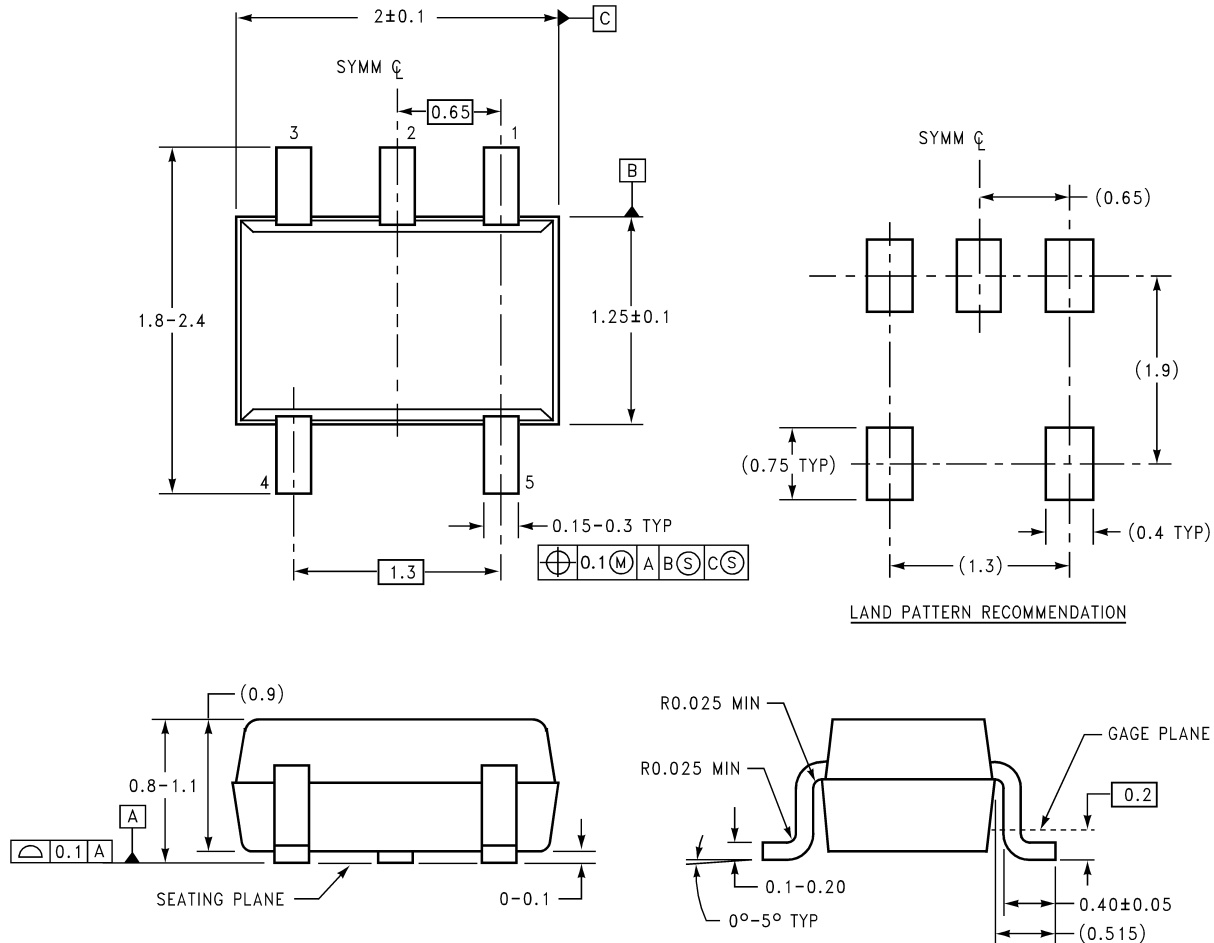
SC70-5 Reel Dimensions



8mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331+ 0.059/-0.000 8.40 + 1.50/- 0.00	0.567 14.40	W1 + 0.078/-0.039 W1 + 2.00/-1.00
Tape Size	A	B	C	D	N	W1	W2	W3

## Physical Dimensions

unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

MAA05A (REV B)

**SC70-5**  
**NS Package Number MAA05A**

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