

## LPV531

# Programmable Micropower CMOS Input, Rail-to-Rail Output Operational Amplifier

### General Description

The LPV531 is an extremely versatile operational amplifier. A single external resistor gives the system designer the ability to define the quiescent current, gain bandwidth product and output short circuit current. This innovative feature gives the system designer a method to dynamically switch the power level to optimize the performance of the op amp and meet the system design requirements.

The LPV531 can be tailored to a wide variety of applications. It offers the system designer the ability to dynamically trade off supply current for bandwidth by adjusting the current drawn from the  $I_{SEL}$  pin using a DAC or switching in different value resistors in series with the  $I_{SEL}$  pin. The LPV531 is capable of operating from 73 kHz, consuming only 5  $\mu$ A, to as fast as 4.6 MHz, consuming only 425  $\mu$ A. The input offset voltage is relatively independent and therefore is not significantly affected by the chosen power level.

Utilizing a CMOS input stage, the LPV531 achieves an input bias current of 50 fA and a common mode input voltage which extends from the negative rail to within 1.2V of the positive supply. The LPV531's rail-to-rail class AB output stage enables this op amp to offer maximum dynamic range at low supply voltage.

Offered in the space saving 6-pin TSOT23 package, the LPV531 is ideal for use in handheld electronics and portable applications. The LPV531 is manufactured using National's advanced VIP50 process.

A fixed supply current/gain bandwidth is available upon request.

### Features

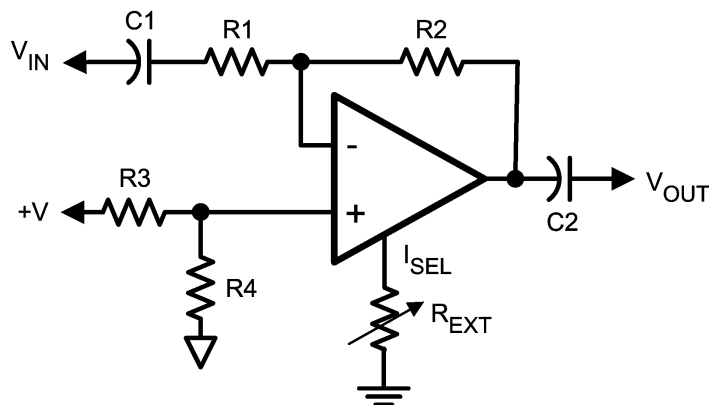
(Typical 5V supply, unless otherwise noted.)

- Supply voltage 2.7V to 5.5V
- Dynamic power mode setting
- Continuously programmable supply current
  - Range 5  $\mu$ A to 425  $\mu$ A
- Continuously programmable bandwidth
  - Range 73 kHz to 4.6 MHz
- Input common mode voltage range -0.3V to 3.8V
- CMRR 95 dB
- Rail-to-rail output voltage swing
- Input offset voltage 1 mV

### Applications

- AC coupled circuits
- Portable instrumentation
- Active filters

### Typical Application



AC Coupled Application

20132335

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)

Human Body Model	2000V
Machine Model	200V
$V_{IN}$ Differential	$\pm 2V$
Supply Voltage ( $V^+ - V^-$ )	6V
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Junction Temperature (Note 5)	$+150^\circ\text{C}$

Soldering Information

Infrared or Convection (20 sec)	$235^\circ\text{C}$
Wave Soldering Lead Temp. (10 sec)	$260^\circ\text{C}$

**Operating Ratings** (Note 1)

Operating Temperature Range	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Supply Voltage ( $V^+ - V^-$ )	2.7V to 5.5V
Package Thermal Resistance ( $\theta_{JA}$ ) (Note 4)	
6-Pin TSOT23	$171^\circ\text{C/W}$

**5V Full Power Mode Electrical Characteristics**

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$ ,  $I_{SEL}$  pin connected to  $V^-$ ,  $R_L = 100\text{ k}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
$V_{OS}$	Input Offset Voltage			$\pm 1$	$\pm 4.5$ <b><math>\pm 5</math></b>	mV
$\Delta V_{OS}$	Input Offset Voltage Difference	( $V_{OS}$ in Full Power Mode) – ( $V_{OS}$ in Low Power Mode)		$\pm 0.1$	$\pm 2$	mV
TC $V_{OS}$	Input Offset Average Drift	(Note 8)		$\pm 2$		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	(Note 9)		.05	$\pm 10$ <b><math>\pm 100</math></b>	pA
CMRR	Common Mode Rejection Ratio	$V_{CM}$ Stepped from 0V to 3.5V	72 <b>68</b>	95		dB
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7V$ to $5.5V$ $V_{CM} = 1V$	74 <b>70</b>	90		dB
CMVR	Input Common Mode Voltage Range	CMRR $\geq 50\text{ dB}$	-0.3		3.8	V
$A_{VOL}$	Large Signal Voltage Gain	$V_O = 0.5V$ to $4.5V$ $R_L = 1\text{ k}\Omega$ to $V^+/2$	87 <b>84</b>	96		dB
		$V_O = 0.5V$ to $4.5V$ $R_L = 10\text{ k}\Omega$ to $V^+/2$	104 <b>100</b>	114		
		$V_O = 0.5V$ to $4.5V$ $R_L = 100\text{ k}\Omega$ , to $V^+/2$	108 <b>104</b>	128		
$V_O$	Output Swing High	$R_L = 1\text{ k}\Omega$ to $V^+/2$		120	180 <b>195</b>	mV from $V^+$
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		55	80 <b>85</b>	
		$R_L = 100\text{ k}\Omega$ to $V^+/2$		30	50 <b>60</b>	
	Output Swing Low	$R_L = 1\text{ k}\Omega$ to $V^+/2$		160	210 <b>230</b>	mV
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		105	120 <b>135</b>	
		$R_L = 100\text{ k}\Omega$ to $V^+/2$		95	120 <b>135</b>	
$I_{SC}$	Output Short Circuit Current (Note 3)	Sourcing, $V_O = 2.5V$ $V_{ID} = 100\text{ mV}$		-15	-8 <b>-3</b>	mA
		Sinking, $V_O = 2.5V$ $V_{ID} = -100\text{ mV}$	13 <b>10</b>	24		
$I_S$	Supply Current			425	530 <b>650</b>	$\mu\text{A}$

## 5V Full Power Mode Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$ ,  $I_{SEL}$  pin connected to  $V^-$ ,  $R_L = 100\text{ k}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate (Note 7)	$A_V = +1$ , $V_{IN} = 0.5\text{V}$ to $3.5\text{V}$ $C_L = 15\text{ pF}$	1.55 <b>1</b>	2.5		V/ $\mu\text{s}$
GBW	Gain Bandwidth Product	$C_L = 20\text{ pF}$		4.6		MHz
$e_n$	Input-Referred Voltage Noise	$f = 100\text{ kHz}$		20		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		28		
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$		6		fA/ $\sqrt{\text{Hz}}$

## 5V Mid-Power Mode Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$ ,  $I_{SEL}$  pin connected to  $V^-$  through  $100\text{ k}\Omega$  resistor,  $R_L = 100\text{ k}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
$V_{OS}$	Input Offset Voltage			$\pm 1$	$\pm 4.5$ <b><math>\pm 5</math></b>	mV
$\Delta V_{OS}$	Input Offset Voltage Difference	( $V_{OS}$ in Full Power Mode) – ( $V_{OS}$ in Low Power Mode)		$\pm 0.1$	$\pm 2$	mV
TC $V_{OS}$	Input Offset Average Drift	(Note 8)		$\pm 2$		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	(Note 9)		.05	$\pm 10$ <b><math>\pm 100</math></b>	pA
CMRR	Common Mode Rejection Ratio	$V_{CM}$ Stepped from $0\text{V}$ to $3.5\text{V}$	72 <b>68</b>	92		dB
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{V}$ to $5.5\text{V}$	72 <b>68</b>	88		dB
CMVR	Input Common Mode Voltage Range	CMRR $\geq 50\text{ dB}$	-0.3		3.8	V
$A_{VOL}$	Large Signal Voltage Gain	$V_O = 0.5\text{V}$ to $4.5\text{V}$ $R_L = 10\text{ k}\Omega$ to $V^+/2$	86 <b>82</b>	96		dB
		$V_O = 0.5\text{V}$ to $4.5\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$	100 <b>98</b>	114		
$V_O$	Output Swing High	$R_L = 10\text{ k}\Omega$ to $V^+/2$		115	160 <b>175</b>	mV from $V^+$
		$R_L = 100\text{ k}\Omega$ to $V^+/2$		65	110 <b>120</b>	
	Output Swing Low	$R_L = 10\text{ k}\Omega$ to $V^+/2$		150	165 <b>180</b>	mV
		$R_L = 100\text{ k}\Omega$ to $V^+/2$		105	120 <b>135</b>	
$I_{SC}$	Output Short Circuit Current (Note 3)	Sourcing, $V_O = 2.5\text{V}$ $V_{ID} = 100\text{ mV}$		-4	-1.5 <b>-1</b>	mA
		Sinking, $V_O = 2.5\text{V}$ $V_{ID} = -100\text{ mV}$	1.5 <b>1</b>	4		
$I_S$	Supply Current			42	55 <b>62</b>	$\mu\text{A}$
SR	Slew Rate (Note 7)	$A_V = +1$ , $V_{IN} = 0.5\text{V}$ to $3.5\text{V}$	180 <b>100</b>	250		V/ms
GBW	Gain Bandwidth Product	$C_L = 20\text{ pF}$		625		kHz
$e_n$	Input-Referred Voltage Noise	$f = 100\text{ kHz}$		55		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		60		

## 5V Mid-Power Mode Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$ ,  $I_{SEL}$  pin connected to  $V^-$  through 100 k $\Omega$  resistor,  $R_L = 100\text{ k}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$		6		fA/ $\sqrt{\text{Hz}}$

## 5V Low Power Mode Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$ ,  $I_{SEL}$  connected to  $V^-$  through 1 M $\Omega$  resistor,  $R_L = 100\text{ k}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
$V_{OS}$	Input Offset Voltage			$\pm 1$	$\pm 4.5$ <b><math>\pm 5</math></b>	mV
$\Delta V_{OS}$	Input Offset Voltage Difference	( $V_{OS}$ in Full Power Mode) – ( $V_{OS}$ in Low Power Mode)		$\pm 0.1$	$\pm 2$	mV
TC $V_{OS}$	Input Offset Average Drift	(Note 8)		$\pm 2$		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	(Note 9)		.05	$\pm 10$ <b><math>\pm 100</math></b>	pA
CMRR	Common Mode Rejection Ratio	$V_{CM}$ Stepped from 0V to 3.5V	72 <b>68</b>	90		dB
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{V}$ to 5.5V	72 <b>68</b>	85		dB
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50\text{ dB}$	-0.3		3.8	V
$A_{VOL}$	Large Signal Voltage Gain	$V_O = 0.5\text{V}$ to 4.5V $R_L = 10\text{ k}\Omega$ to $V^+/2$		90		dB
		$V_O = 0.5\text{V}$ to 4.5V $R_L = 100\text{ k}\Omega$ to $V^+/2$	80 <b>78</b>	100		
$V_O$	Output Swing High	$R_L = 10\text{ k}\Omega$ to $V^+/2$		175	400 <b>1600</b>	mV from $V^+$
		$R_L = 100\text{ k}\Omega$ to $V^+/2$		115	200 <b>230</b>	
	Output Swing Low	$R_L = 10\text{ k}\Omega$ to $V^+/2$		250	1200 <b>1800</b>	mV
		$R_L = 100\text{ k}\Omega$ to $V^+/2$		150	165 <b>180</b>	
$I_{SC}$	Output Short Circuit Current (Note 3)	Sourcing, $V_O = 2.5\text{V}$ $V_{ID} = 100\text{ mV}$		-400	-100 <b>-35</b>	$\mu\text{A}$
		Sinking, $V_O = 2.5\text{V}$ $V_{ID} = -100\text{ mV}$	80 <b>35</b>	300		
$I_S$	Supply Current			5	7 <b>8</b>	$\mu\text{A}$
SR	Slew Rate (Note 7)	$A_V = +1$ , $V_{IN} = 0.5\text{V}$ to 3.5V	10 <b>8</b>	28		V/ms
GBW	Gain Bandwidth Product	$C_L = 20\text{ pF}$		73		kHz
$e_n$	Input-Referred Voltage Noise	$f = 1\text{ kHz}$		200		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$		60		fA/ $\sqrt{\text{Hz}}$

## Power Select Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V_O = V^+/2$ ,  $R_L = 100\text{ k}\Omega$ . **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
$t_{LF}$	Time from Low Power Mode to Full Power Mode			210		ns
$t_{FL}$	Time from Full Power Mode to Low Power Mode			500		ns
$V_{REXT}$	Voltage @ $I_{SEL}$ Pin	$I_{SEL}$ Pin Left Open	100	110	125	mV
$R_{INT}$			9	11	14.5	$\text{k}\Omega$

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

**Note 2:** Human Body Model is  $1.5\text{ k}\Omega$  in series with  $100\text{ pF}$ . Machine Model is  $0\Omega$  in series with  $200\text{ pF}$ .

**Note 3:** Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ .

**Note 4:** The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC board.

**Note 5:** Typical values represent the most likely parametric norm.

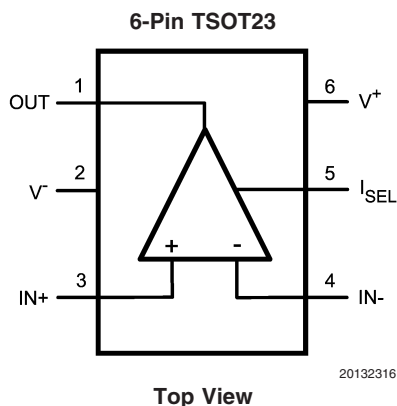
**Note 6:** All limits are guaranteed by testing or statistical analysis.

**Note 7:** Slew rate is the slower of the rising or falling slew rates.

**Note 8:** Offset voltage average drift is determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.

**Note 9:** Guaranteed by design.

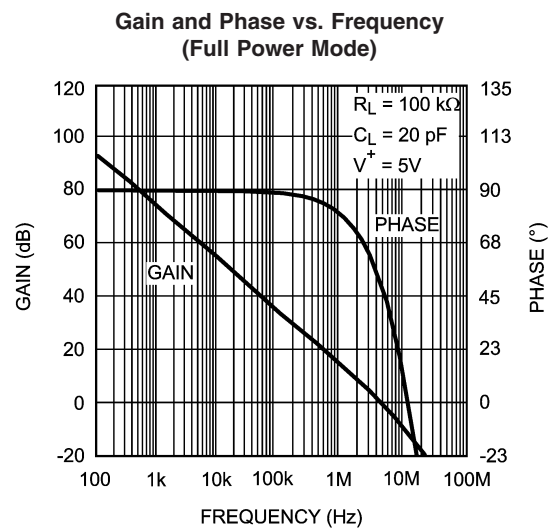
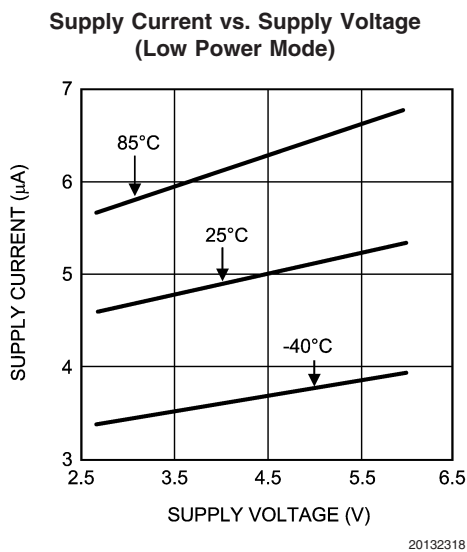
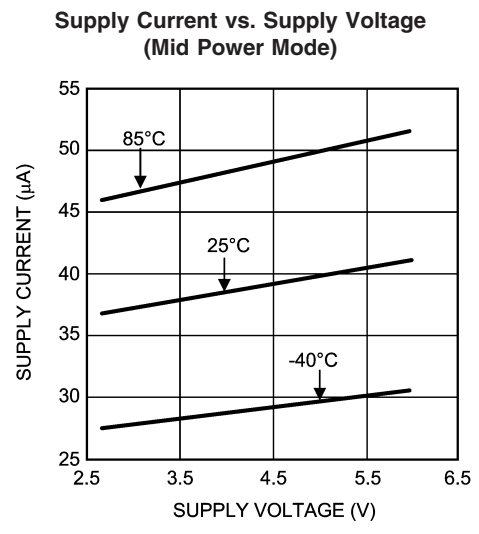
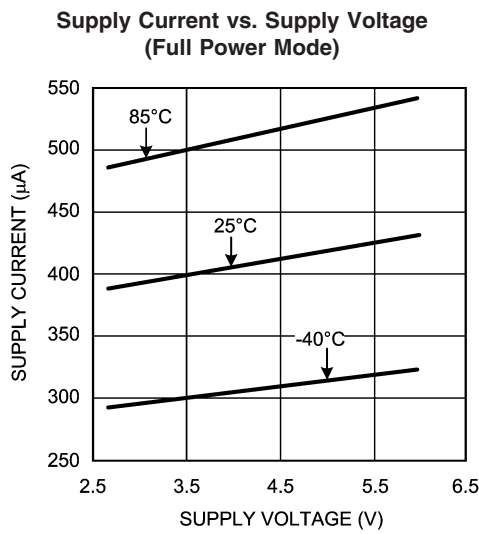
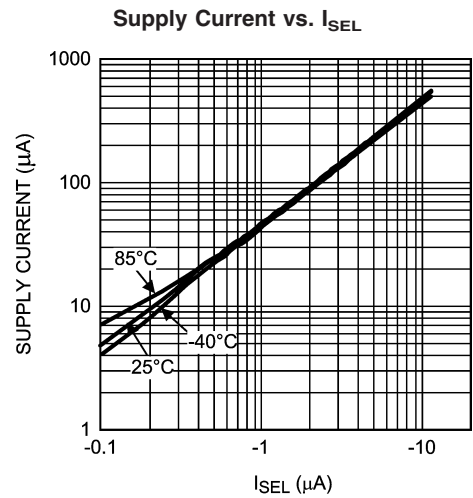
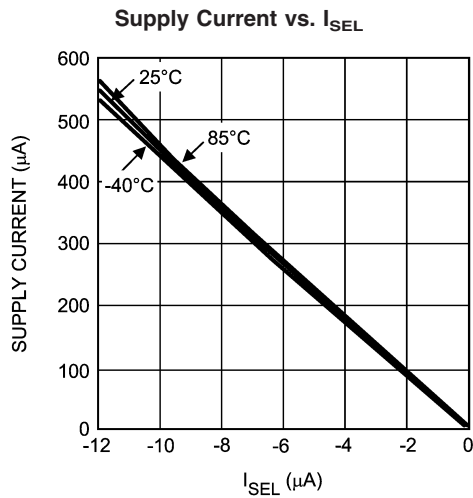
## Connection Diagram



## Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
6-Pin TSOT23	LPV531MK	AV2A	1k Units Tape and Reel	MK06A
	LPV531MKX		3k Units Tape and Reel	

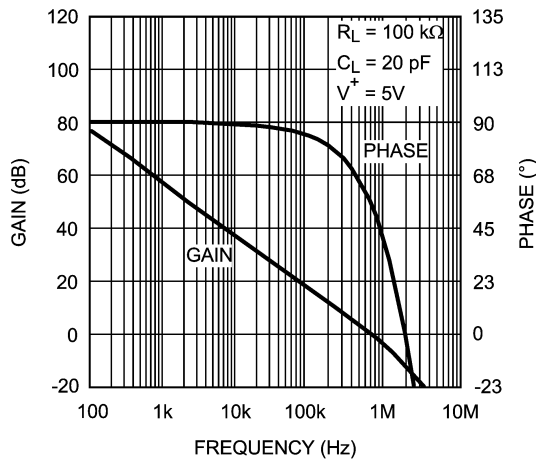
**Typical Performance Characteristics** Unless otherwise specified,  $V^+ = 5V$ ,  $T_J = 25^\circ C$ . For Full Power Mode the  $I_{SEL}$  pin is connected to  $V^-$ ; for Mid-Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 100 k $\Omega$  resistor; for Low Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 1 M $\Omega$  resistor.



## Typical Performance Characteristics

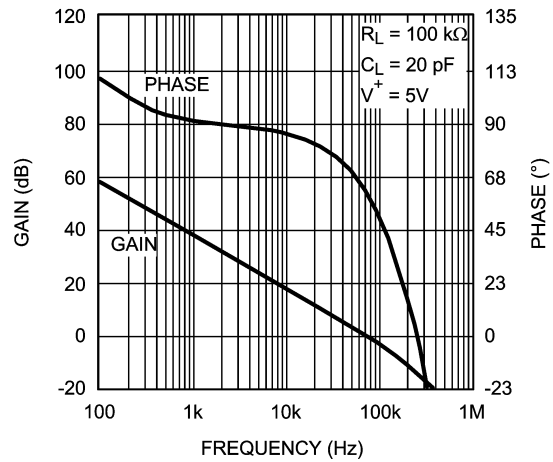
Unless otherwise specified,  $V^+ = 5V$ ,  $T_J = 25^\circ C$ . For Full Power Mode the  $I_{SEL}$  pin is connected to  $V^-$ ; for Mid-Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a  $100\text{ k}\Omega$  resistor; for Low Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a  $1\text{ M}\Omega$  resistor. (Continued)

Gain and Phase vs. Frequency  
(Mid Power Mode)



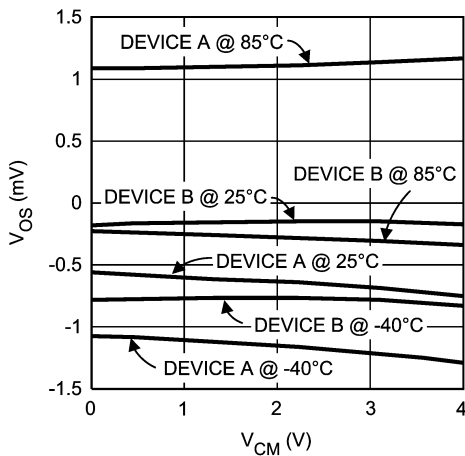
20132331

Gain and Phase vs. Frequency  
(Low Power Mode)



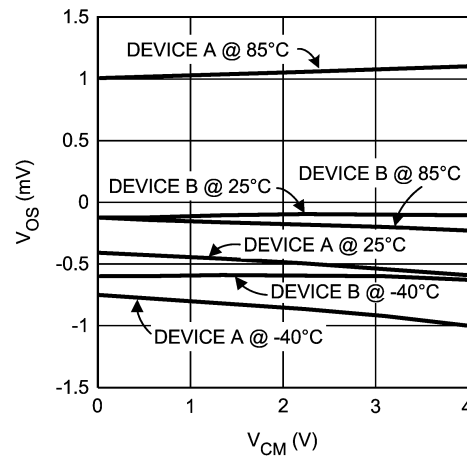
20132329

Input Offset Voltage vs. Common Mode Voltage  
(Full Power Mode)



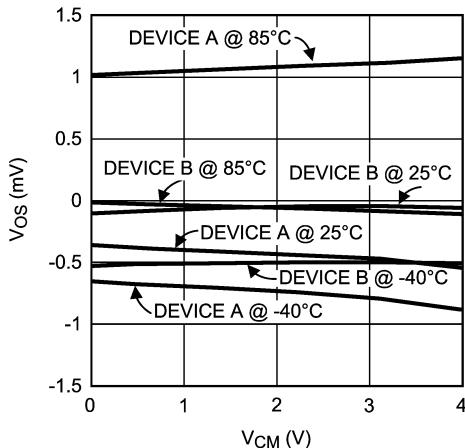
20132360

Input Offset Voltage vs. Common Mode Voltage  
(Mid Power Mode)



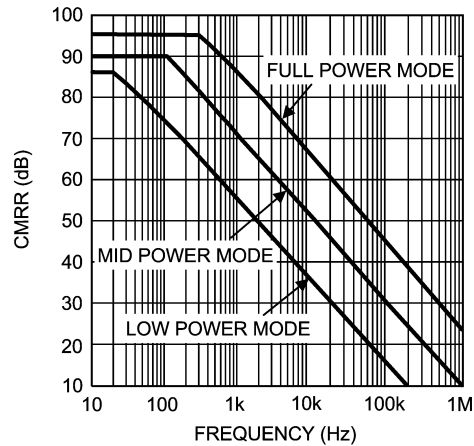
20132359

Input Offset Voltage vs. Common Mode Voltage  
(Low Power Mode)



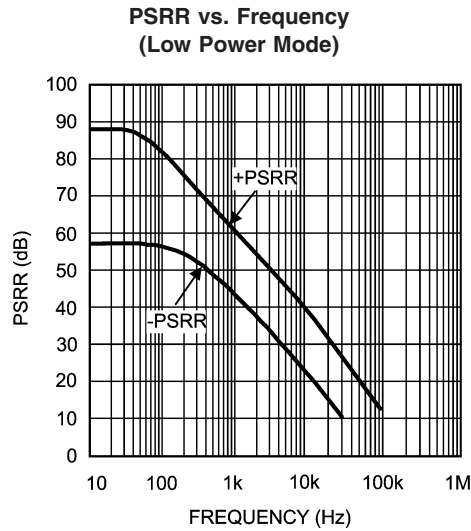
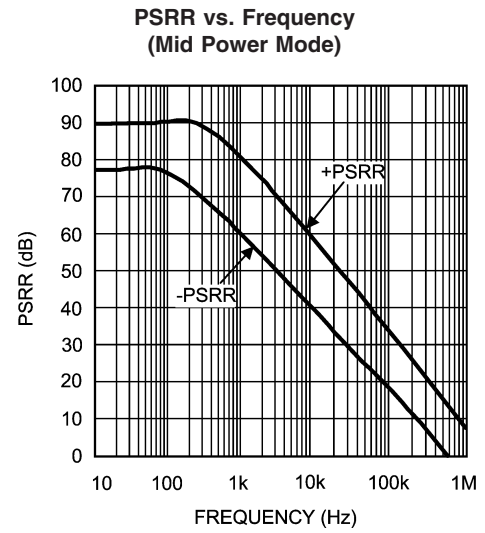
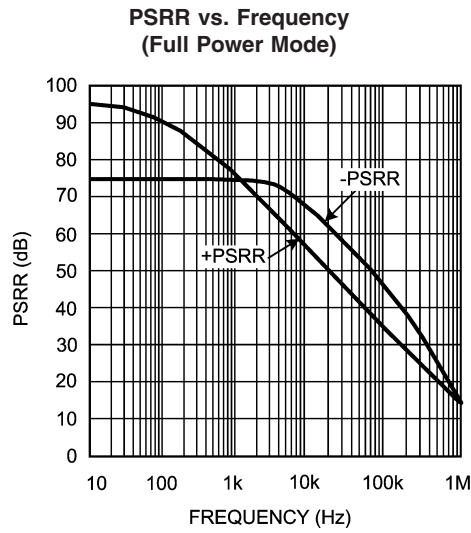
20132358

CMRR vs. Frequency

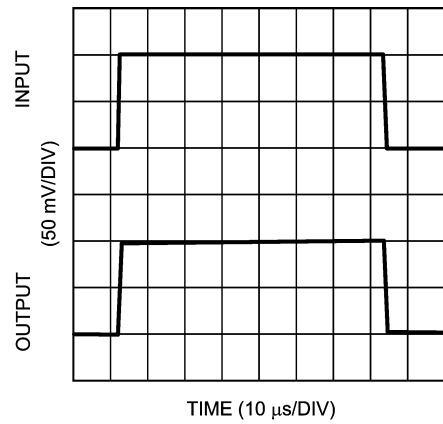


20132362

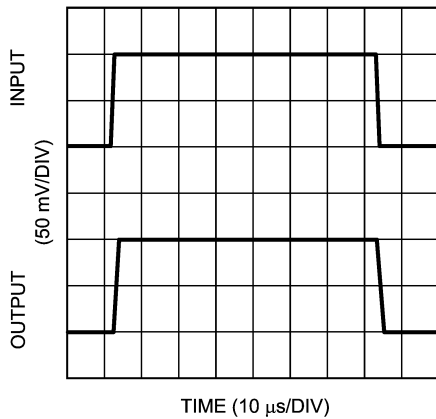
**Typical Performance Characteristics** Unless otherwise specified,  $V^+ = 5V$ ,  $T_J = 25^\circ C$ . For Full Power Mode the  $I_{SEL}$  pin is connected to  $V^-$ ; for Mid-Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 100 k $\Omega$  resistor; for Low Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 1 M $\Omega$  resistor. (Continued)



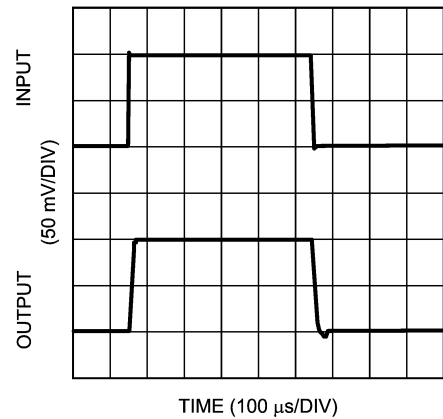
**Small Signal Non-Inverting Response (Full Power Mode)**



**Small Signal Non-Inverting Response (Mid Power Mode)**

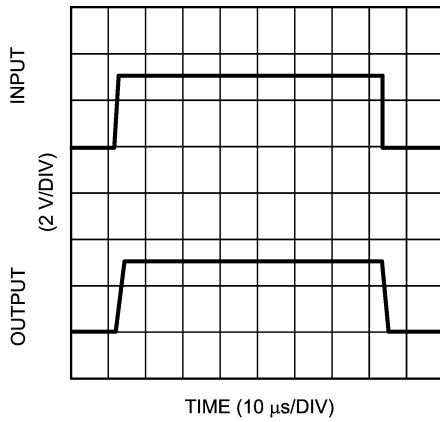


**Small Signal Non-Inverting Response (Low Power Mode)**



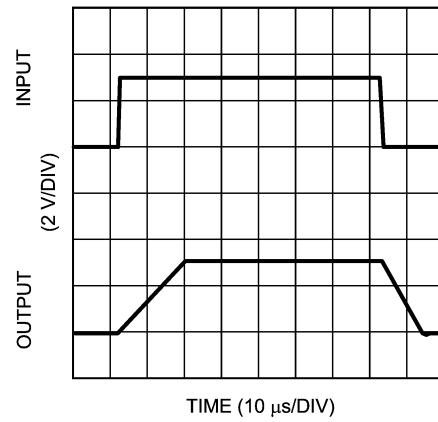
**Typical Performance Characteristics** Unless otherwise specified,  $V^+ = 5V$ ,  $T_J = 25^\circ C$ . For Full Power Mode the  $I_{SEL}$  pin is connected to  $V^-$ ; for Mid-Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 100 k $\Omega$  resistor; for Low Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 1 M $\Omega$  resistor. (Continued)

**Large Signal Non-Inverting Response  
(Full Power Mode)**



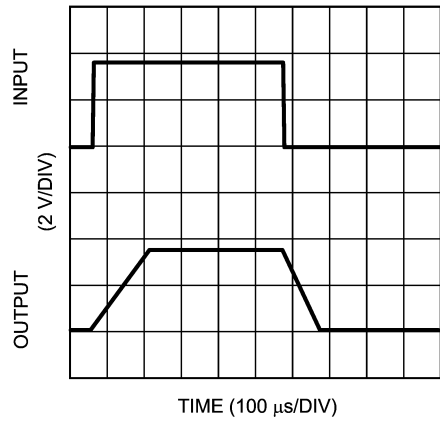
20132347

**Large Signal Non-Inverting Response  
(Mid Power Mode)**



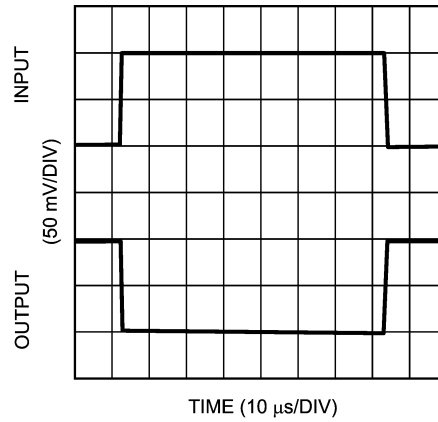
20132351

**Large Signal Non-Inverting Response  
(Low Power Mode)**



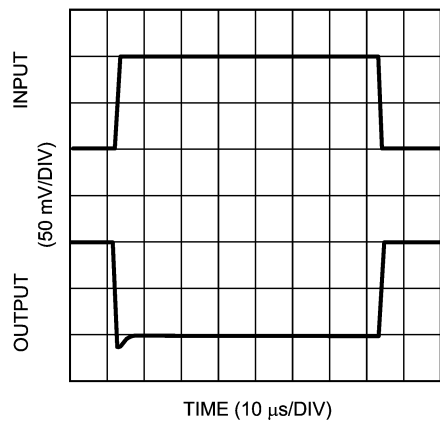
20132355

**Small Signal Inverting Pulse Response  
(Full Power Mode)**



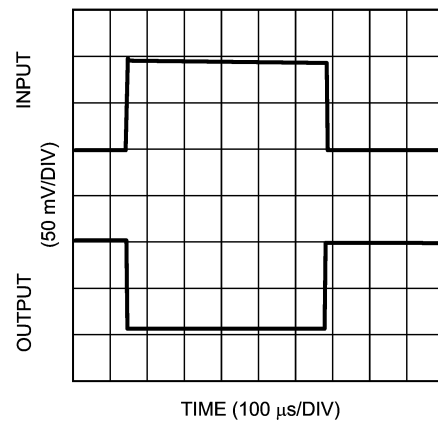
20132348

**Small Signal Inverting Pulse Response  
(Mid Power Mode)**



20132352

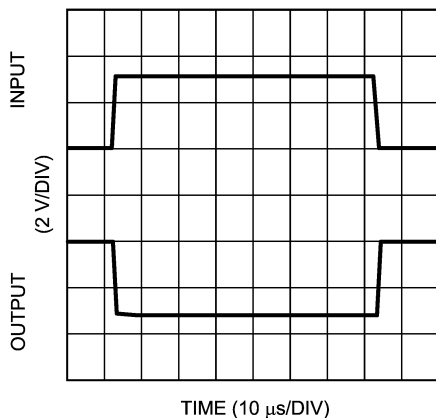
**Small Signal Inverting Pulse Response  
(Low Power Mode)**



20132356

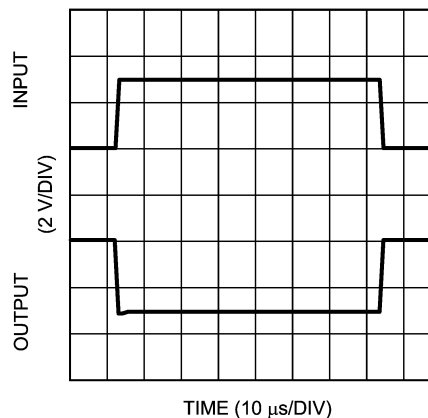
**Typical Performance Characteristics** Unless otherwise specified,  $V^+ = 5V$ ,  $T_J = 25^\circ C$ . For Full Power Mode the  $I_{SEL}$  pin is connected to  $V^-$ ; for Mid-Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a  $100\text{ k}\Omega$  resistor; for Low Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a  $1\text{ M}\Omega$  resistor. (Continued)

**Large Signal Inverting Response  
(Full Power Mode)**



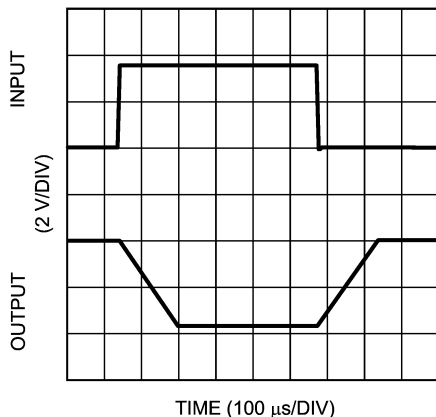
20132349

**Large Signal Inverting Response  
(Mid Power Mode)**



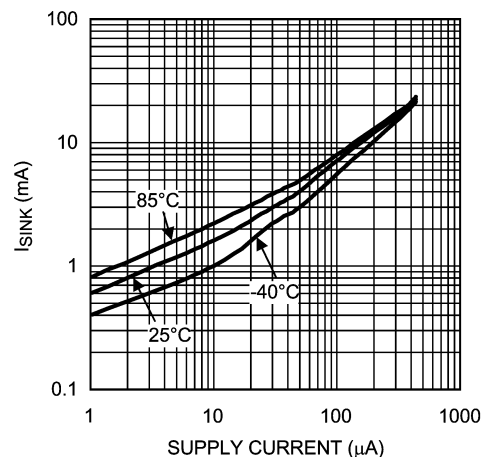
20132353

**Large Signal Inverting Response  
(Low Power Mode)**



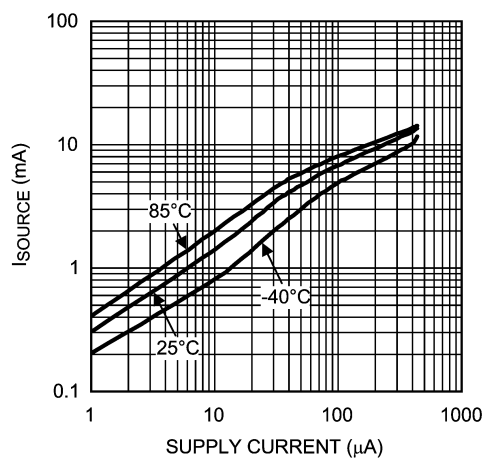
20132357

**$I_{SINK}$  vs. Supply Current**



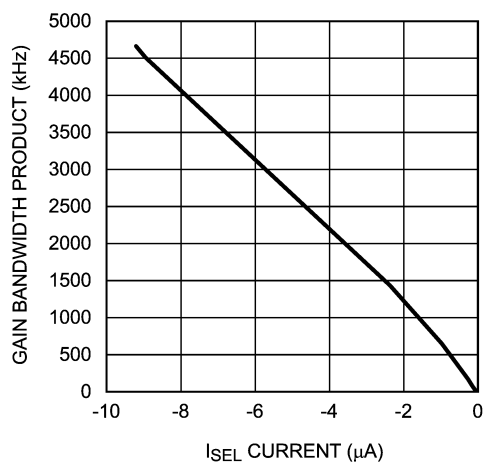
20132344

**$I_{SOURCE}$  vs. Supply Current**



20132343

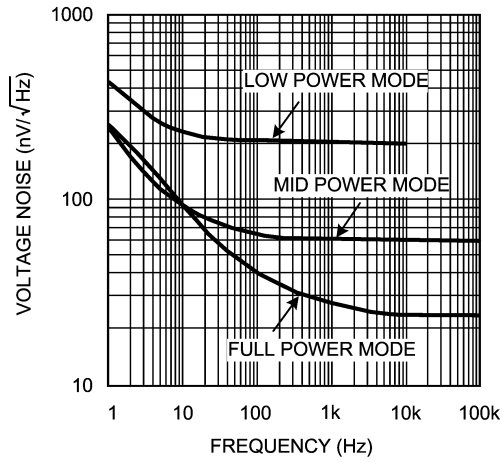
**Gain Bandwidth Product vs.  $I_{SEL}$**



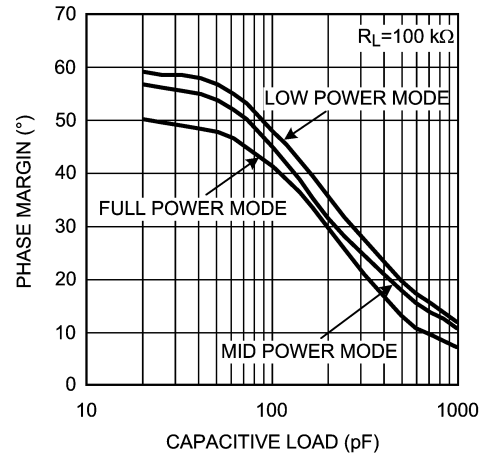
20132345

**Typical Performance Characteristics** Unless otherwise specified,  $V^+ = 5V$ ,  $T_J = 25^\circ C$ . For Full Power Mode the  $I_{SEL}$  pin is connected to  $V^-$ ; for Mid-Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 100 k $\Omega$  resistor; for Low Power Mode the  $I_{SEL}$  pin is connected to  $V^-$  through a 1 M $\Omega$  resistor. (Continued)

**Input Referred Voltage Noise vs. Frequency**



**Phase Margin vs. Capacitive Load**



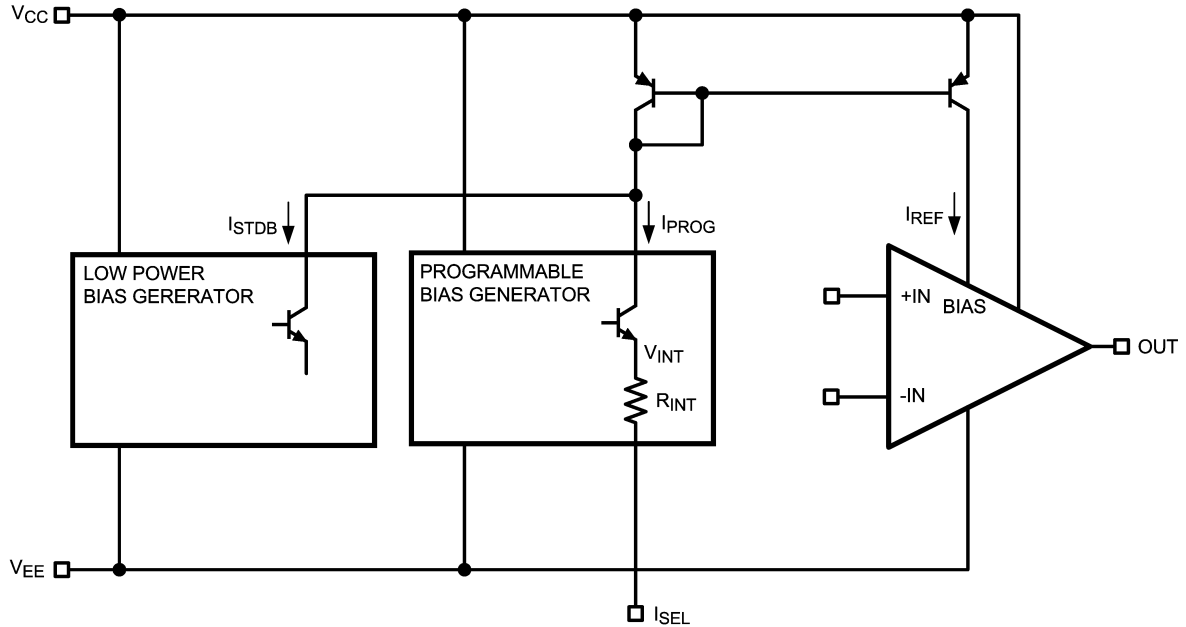
## Application Information

The LPV531 is an extremely versatile operational amplifier because performance and power consumption can be adjusted during operation. This provides a method to dynamically optimize the supply current, the bandwidth and the output short circuit current in the application. The power level can be set by the current drawn from the  $I_{SEL}$  pin according to the application performance requirements.

### CIRCUIT TOPOLOGY

As shown in *Figure 1*, the LPV531 contains two internal bias reference generators that deliver a reference current ( $I_{REF}$ ) to the amplifier core. The programmable bias generator gen-

erates a 110 mV reference voltage ( $V_{INT}$ ). This reference voltage is converted into a programmable reference current ( $I_{PROG}$ ) through the internal resistor ( $R_{INT}$ ) and the external resistor ( $R_{EXT}$ ) connected to the  $I_{SEL}$  pin. Internally,  $I_{PROG}$  is added to the output current from the low power bias generator ( $I_{STDB}$ ). When the  $I_{SEL}$  pin is left floating,  $I_{PROG}$  equals zero and the  $I_{REF}$  equals  $I_{STDB}$ . The value of  $I_{STDB}$  is such that in this mode the power supply current is below 1  $\mu A$ . In this 1  $\mu A$  power mode, the LPV531 is functional but performance over the full temperature range is not guaranteed. The 1  $\mu A$  power mode operation is only recommended for applications with a temperature range between 0 and 70°C.



20132337

FIGURE 1. Simplified Schematic

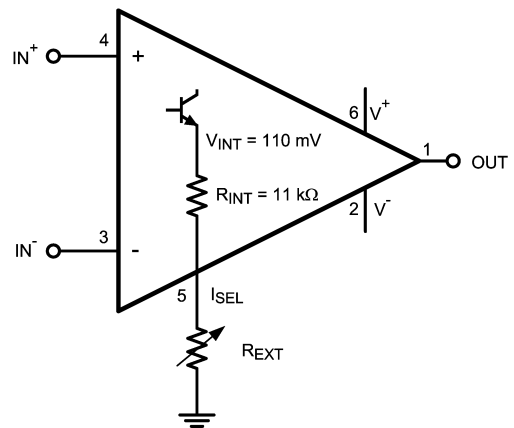
### POWER MODE CONTROL

To illustrate typical configurations three possible solutions to control the power mode(s) of the LPV531 will be described.

#### 1. Single Power Mode

If the application requires one single power mode for the LPV531, then the easiest way to achieve this is to connect a resistor ( $R_{EXT}$ ) from the  $I_{SEL}$  pin to  $V^-$ . Together with the internal circuitry,  $R_{EXT}$  will determine the current drawn from the  $I_{SEL}$  pin. Internally the  $I_{SEL}$  pin is connected to an 11 k $\Omega$  internal series resistor ( $R_{INT}$ ) which is biased at  $V_{INT} = 110$  mV. This set up is illustrated in *Figure 2*.

For a desired supply current, bandwidth, short circuit current, or load resistance, the required value of  $R_{EXT}$  can be calculated using the equations in the section "DETERMINING THE  $I_{SEL}$  LEVELS".



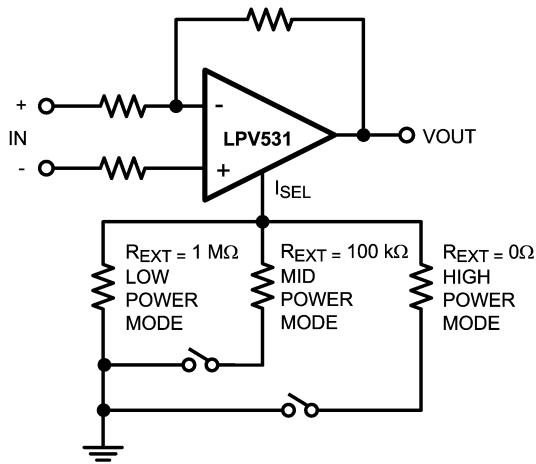
20132336

FIGURE 2. Single Power Mode

## Application Information (Continued)

### 2. Switched Discrete Power Modes

In this typical application, the LPV531 can operate at two (or more) power modes in order to fulfill the demands of the design. One of the modes is used to save power. It is a low power mode which is set by using a large resistor. The others are the higher power modes which are set by one or more smaller resistors. The larger resistor that sets the low power mode can be permanently connected while the smaller resistor(s) can be switched in parallel to set the high power mode(s). This configuration allows the designer to get the required performance from the LPV531 when needed.



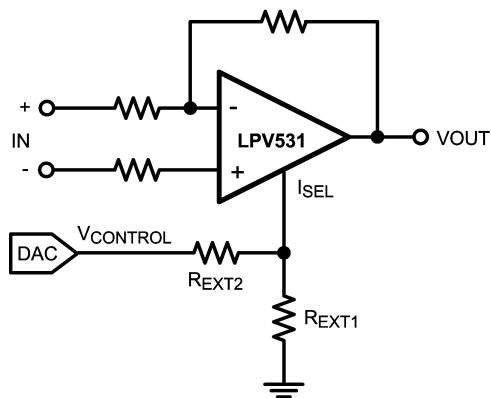
20132363

FIGURE 3. Power Modes Set by Resistors and Switches

The switches shown in *Figure 3* can be easily implemented with an open drain I/O port of an ASIC or any other simple pull down switch.

### 3. DAC Controlled Power Modes

For voltage controlled filter applications, where control of the gain bandwidth is essential, a DAC and a resistive voltage divider can be used. In this application the current drawn from the ISEL pin is controlled by the DAC. The DAC's total output range is divided to match the  $V^-$  to  $V_{INT}$  voltage which has the range of 0-110 mV.



20132364

FIGURE 4. DAC Controlled Power Mode Configurations

The output of the resistive voltage divider should have an impedance that is small compared to the value of  $R_{INT}$  to allow a linear control of the power level. Therefore,  $R_{EXT2}$  needs to have a value in the order of  $R_{INT}/10$  and  $R_{EXT1} = 125 \text{ mV} \cdot R_{EXT2} / V_{CONTROL,MAX}$ . For 1  $\mu\text{A}$  power mode operation, these resistor values will divide the maximum voltage of  $V_{CONTROL}$  to 125 mV.

### DETERMINING THE $R_{EXT}$ VALUES AND $I_{SEL}$ LEVELS

To determine the value of  $R_{EXT}$  that is needed for a certain supply current or bandwidth, the following equations can be used:

$$PSI = 1 \mu\text{A} + 40 \times \frac{110 \text{ mV}}{R_{EXT} + 11 \text{ k}}$$

or

$$R_{EXT} = 40 \times \frac{110 \text{ mV}}{PSI - 1 \mu\text{A}} - 11 \text{ k}$$

$$GBW = 11 \text{ kHz} + \frac{50[\text{GHz} \cdot \Omega]}{R_{EXT} + 11 \text{ k}} \quad \text{or} \quad R_{EXT} = \frac{50[\text{GHz} \cdot \Omega]}{GBW - 11 \text{ kHz}} - 11 \text{ k}$$

For the power modes characterized in this datasheet, these formulas lead to the values in *Table 1*. These values deviate slightly from the typical values presented in the electrical characteristic tables. The values in *Table 1* are calculated using approximated linear equations while the values in the Electrical Characteristics table are the result of characterization measurement procedures.

TABLE 1. Values for Characterized Power Modes

$R_{EXT}$	$I_{SEL}$	Supply Current	Gain Bandwidth Product
1 $\Omega$	9 $\mu\text{A}$	400 $\mu\text{A}$	4.6 MHz
100 k $\Omega$	0.9 $\mu\text{A}$	40 $\mu\text{A}$	460 kHz
1 M $\Omega$	99 nA	5.3 $\mu\text{A}$	60 kHz

To calculate the  $R_{EXT}$  which will allow the LPV531 to deliver a minimum output current at all times and over all temperatures, use the following equations:

$$ISC = \frac{35 \text{ V}}{R_{EXT} + 11 \text{ k}} \quad \text{or} \quad R_{EXT} = \frac{35 \text{ V}}{ISC} - 11 \text{ k}$$

If the output has to be kept at  $V^+/2$  for a known load resistance, the required  $R_{EXT}$  can be calculated with the following equations:

$$R_{LOAD,MIN} = \frac{0.07}{R_{EXT} + 11 \text{ k}} \quad \text{or} \quad R_{EXT} = \frac{0.07}{R_{LOAD,MIN}} - 11 \text{ k}$$

## Application Information (Continued)

For the characterized power modes these equations lead to the minimum values in *Table 2* below.

**TABLE 2. Minimum Values for Characterized Power Modes**

$R_{EXT}$	$I_{SEL}$	$I_{SC}$	$R_{LOAD}$
1 $\Omega$	9 $\mu A$	3 mA	770 $\Omega$
100 k $\Omega$	0.9 $\mu A$	300 $\mu A$	7.8 k $\Omega$
1 M $\Omega$	99 nA	55 $\mu A$	70.8 k $\Omega$

The smallest load resistor that the LPV531 can drive when in low power mode is 70.8 k $\Omega$ , as shown in *Table 2*. When driving smaller loads, such as the 10 k $\Omega$  load resistor used in the Electrical Characteristics table specification, the output swing in the low power mode is limited. If the application requires a 10 k $\Omega$  load then it is not recommended to use the LPV531 in low power mode.

### $I_{SEL}$ SENSITIVITY

The  $I_{SEL}$  pin is a current reference that directly affects the entire internal bias condition. Therefore, the  $I_{SEL}$  pin is very sensitive to parasitic signal coupling. In order to protect the  $I_{SEL}$  pin from unwanted distortion, it is important to route the PCB layout such that there is as little coupling between the  $I_{SEL}$  pin and the output or other signal traces as possible.

## Typical Application

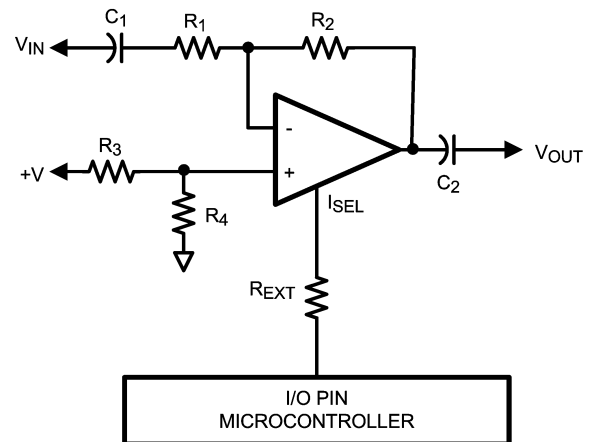
### AC COUPLED CIRCUITS

The programmable power mode makes the LPV531 ideal for AC coupled circuits where the circuit needs to be kept active to maintain a quiescent charge on the coupling capacitors with minimal power consumption. *Figure 5* shows the schematic of an inverting AC coupled amplifier using the LPV531 with the  $I_{SEL}$  pin controlled by I/O ports of a microcontroller. The advantage of the low power active mode for AC coupled amplifiers is the elimination of the time needed to re-establish a quiescent operating point when the amplifier is switched to full power mode.

When an amplifier without a low power active mode is used in low power applications, there are two ways to minimize power consumption. The first method turns off the amplifier by switching off power to the op amp using a transistor switch. The second method uses an amplifier with a shut-down pin. Both of these methods have the problem of allowing the coupling capacitors,  $C_1$  and  $C_2$  to discharge the quiescent DC voltage stored on them when in the shutdown state. When the amplifier is turned on again, the quiescent DC voltages must reestablish themselves. During this time, the amplifier's output is not usable because the output signal is a mixture of the amplified input signal and the charging voltage on the coupling capacitors. The settling time can range from a several milliseconds to several seconds depending on the resistor and capacitor values.

When the LPV531 is placed into the low power mode, the power consumption is minimal but the amplifier is active to maintain the quiescent DC voltage on the coupling capacitors. The transition back to the operational high power mode is fast, within a few hundred nanoseconds. The active low power mode of the LPV531 separates two critical aspects of

a low power AC amplifier design. The values of the gain resistors, bias resistors, and coupling capacitors can be chosen independently of the turn-on and stabilization time.



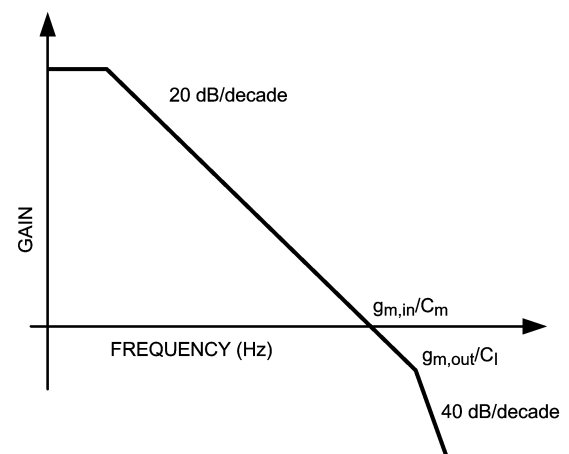
20132334

**FIGURE 5. Inverting AC Coupled Application**

### PROGRAMMABLE POWER LEVELS AND THE EFFECTS OF STABILITY COMPENSATION METHODS USING EXTERNAL COMPONENTS

In some op amp application circuits, external capacitors are used to improve the stability of the feedback loop around the amplifier. When using the programmable power level feature of the LPV531 such stability improvement methods may not work. This is related to the internal frequency compensation method applied inside the LPV531.

*Figure 6* shows the bode plot of the frequency response of the LPV531. The gain-bandwidth product is determined by the transconductance of the input stage ( $g_{m,in}$ ) and the internal Miller compensation capacitor ( $C_m$ ). The non-dominant pole is formed by the transconductance of the output stage ( $g_{m,out}$ ) and the load capacitance connected to the output of the LPV531 ( $C_l$ ). The frequency response crosses the frequency axis with a single-pole slope (20 dB/decade). This ensures the stability of feedback loops formed around the LPV531.



20132371

**FIGURE 6. Bode Plot of the Frequency Response**

## Typical Application (Continued)

When the load capacitance is increased, the pole at the output will shift to lower frequencies. Eventually, the output pole will shift below the unity gain frequency. This will cause the frequency characteristic to move through the 0 dB axis with a slope of 40 dB/decade and a feedback loop formed around the LPV531 may oscillate. The LPV531 is internally compensated in such a manner that it will be stable for load capacitances up to 100 pF.

When the power setting of the LPV531 is reduced, both the transconductance of the input stage and the transconductance of the output stage will scale linearly with the power level to lower levels. This means that both the unity gain frequency and the pole to the transconductance of the output stage and the load capacitance will move down. Because both the unity gain frequency and the output pole move down in similar amounts, the stability of the LPV531 is still the same. This is shown in *Figure 7* which gives the phase margin as a function of the load capacitance in the low power mode (5  $\mu$ A), mid-power mode (40  $\mu$ A) and high power mode (400  $\mu$ A). Though the power level and unity gain frequency move with about two decades, the phase margin as a function of the capacitive load is hardly affected. This means that when the LPV531 is stable in an application circuit with a given load capacitance in the high power mode, the circuit will remain stable with the same capacitive load connected when the power level is reduced.

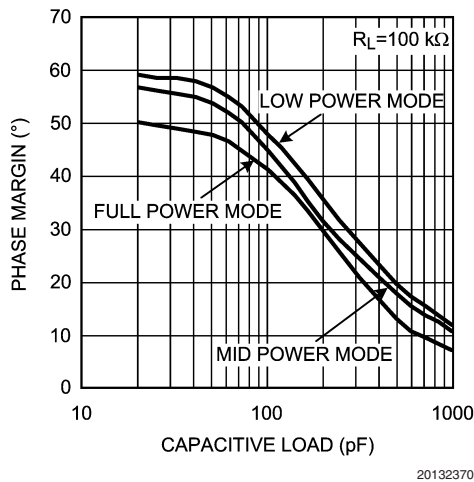


FIGURE 7. Phase Margin vs. Capacitive Load

*Figure 8* shows a method that is sometimes used to allow an op amp to drive larger capacitors than it was originally designed to do. The capacitive load is isolated from the output of the op amp with an isolation resistor ( $R_{ISO}$ ). This moves the output pole, that was originally located at  $g_{m,out}/C_L$ , to a higher frequency. This method requires that the value of  $R_{ISO}$  is in the same order of magnitude as  $1/g_{m,out}$ . For the LPV531, this method will not be effective when used across a broad range of power levels. This is because the high power mode will require a relatively small value for  $R_{ISO}$ , while such a small  $R_{ISO}$  will be ineffective at low power levels. In most applications this should not be a problem as

the LPV531 can drive sufficient capacitive loads without the need for an external isolation resistor.

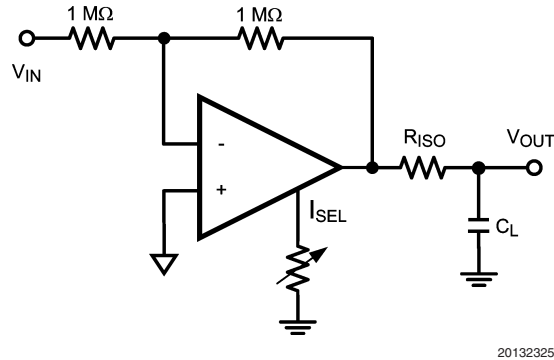
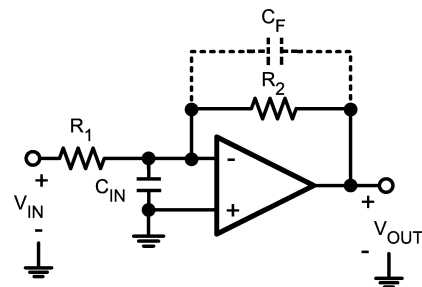


FIGURE 8. Compensation by Isolation Resistor

### INPUT CAPACITANCE AND FEEDBACK CIRCUIT ELEMENTS

The LPV531 has a very low input bias current (50 fA). To obtain this performance a large CMOS input stage is used, which adds to the input capacitance of the op amp,  $C_{IN}$ . Though this does not affect the DC and low frequency performance, at higher frequencies the input capacitance interacts with the input and the feedback impedances to create a pole, which results in lower phase margin and gain peaking. The gain peaking can be reduced by carefully choosing the appropriate feedback resistor, as well as, by using a feedback capacitance,  $C_F$ . For example, in the inverting amplifier shown in *Figure 9*, if  $C_{IN}$  and  $C_F$  are ignored and the open loop gain of the op amp is considered infinite then the gain of the circuit is  $-R_2/R_1$ . An op amp, however, usually has a dominant pole, which causes its gain to drop with frequency. Hence, this gain is only valid for DC and low frequency. To understand the effect of the input capacitance coupled with the non-ideal gain of the op amp, the circuit needs to be analyzed in the frequency domain using a Laplace transform.



$$A_V = - \frac{V_{OUT}}{V_{IN}} = - \frac{R_2}{R_1}$$

FIGURE 9. Inverting Amplifier

## Typical Application (Continued)

For simplicity, the op amp is modelled as an ideal integrator with a unity gain frequency of  $A_0$ . Hence, its transfer function (or gain) in the frequency domain is  $A_0/s$ . Solving the circuit equations in the frequency domain, ignoring  $C_F$  for the moment, results in the following equation for the gain:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}} \quad (1)$$

It can be inferred from the denominator of the transfer function that it has two poles, whose expressions can be obtained by solving for the roots of the denominator:

$$P_{1,2} = \frac{-1}{2C_{IN}} \left[ \frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4A_0 C_{IN}}{R_2}} \right] \quad (2)$$

Equation (2) shows that as the values of  $R_1$  and  $R_2$  are increased, the magnitude of the poles is reduced, and hence the bandwidth of the amplifier is decreased. Furthermore,  $R_1$  and  $R_2$  are related by the gain of the amplifier.

$$A_V = -R_2/R_1, \text{ or alternatively}$$

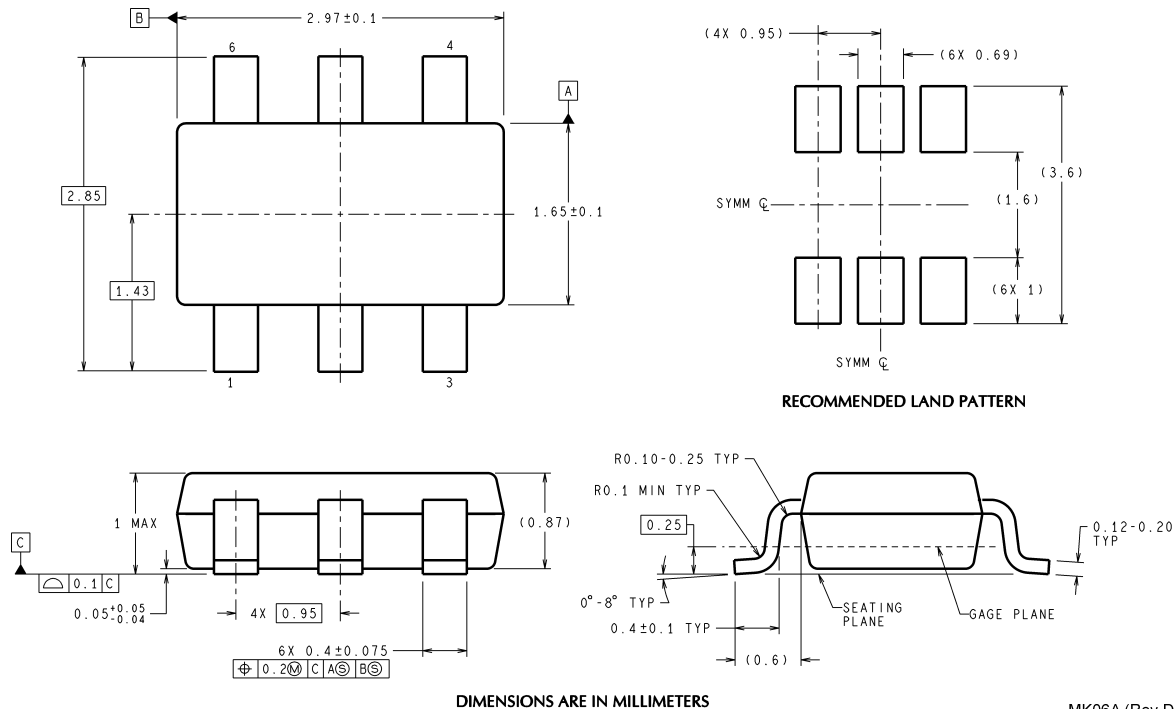
$$R_2 = -A_V R_1$$

It is the presence of pairs of poles in Equation (2) that causes gain peaking. In order to eliminate this effect, the poles should be placed in Butterworth position, since poles in Butterworth position do not cause gain peaking. To achieve a Butterworth pair, the quantity under the square root in Equation 2 should be set to equal  $-1$ . Using this fact and the relation between  $R_1$  and  $R_2$ , the optimum value for  $R_1$  can be found. This is shown in Equation (3). If  $R_1$  is chosen to be larger than this optimum value, gain peaking will occur.

$$R_1 < \frac{(1 - A_V)^2}{2A_0 A_V C_{IN}} \quad (3)$$

In Figure 9,  $C_F$  is added to compensate for input capacitance and to increase stability. In addition,  $C_F$  reduce or eliminates the gain peaking that can be caused by having a larger feedback resistor.

## Physical Dimensions inches (millimeters) unless otherwise noted



MK06A (Rev D)

**6-Pin TSOT23  
NS Package Number MK06A**

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at [www.national.com](http://www.national.com).

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### BANNED SUBSTANCE COMPLIANCE

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

Leadfree products are RoHS compliant.



**National Semiconductor**  
Americas Customer  
Support Center  
Email: [new.feedback@nsc.com](mailto:new.feedback@nsc.com)  
Tel: 1-800-272-9959

[www.national.com](http://www.national.com)

**National Semiconductor**  
Europe Customer Support Center  
Fax: +49 (0) 180-530 85 86  
Email: [europe.support@nsc.com](mailto:europe.support@nsc.com)  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**  
Asia Pacific Customer  
Support Center  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor**  
Japan Customer Support Center  
Fax: 81-3-5639-7507  
Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)  
Tel: 81-3-5639-7560