

NTE3470 Integrated Circuit Floppy Disk Read Amplifier System

Description:

The NTE3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential AC signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

Features:

- Combines All the Active Circuitry to Perform the Floppy Disk Read Amplifier Function in One Circuit
- Improved (Positive) Gain T_C and Tolerance
- Improved Input Common Mode

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$, Note 1 unless otherwise specified)

Power Supply Voltage (Pin11), V_{CC1}	7V
Power Supply Voltage (Pin18), V_{CC2}	16V
Input Voltage (Pin1 and Pin2), V_I	-0.2 to +7.0V
Output Voltage (Pin10), V_O	-0.2 to +7.0V
Operating Ambient Temperature Range, T_A	0° to $+70^\circ\text{C}$
Operating Junction Temperature, T_J	$+150^\circ\text{C}$
Storage Temperature Range, T_{stg}	-65° to $+150^\circ\text{C}$

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Recommended Operating Conditions:

Power Supply Voltage, V_{CC}	
(V_{CC1})	+4.75 to +5.25V
(V_{CC2})	+10 to +14V
Operating Ambient Temperature Range, T_A	0° to $+70^\circ\text{C}$

Electrical Characteristics: ($T_A = 0^\circ$ to $+70^\circ\text{C}$, $V_{CC1} = 4.75$ to 5.25V , $V_{CC2} = 10$ to 14V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Voltage Gain	A _{VD}	f = 200kHz, V _{iD} = 7mV _{RMS}	80	100	130	V/V
Input Base Current	I _{IB}		–	–10	–25	μA
Input Common Mode Range, Linear Operation	V _{ICM}	5% Max THD	–0.1	–	1.5	V
Differential Input Voltage, Linear Op- eration	V _{iD}	5% Max THD	–	–	25	mV _{P-P}
Output Voltage Swing Differential	V _{oD}		3	4	–	V _{P-P}
Output Source Current, Toggled	I _O		–	8.0	–	mA
Output Sink Current (Pin16 and Pin17)	I _{OS}		2.8	4.0	–	mA
Small Signal Input Resistance	r _i	T _A = +25°C	100	250	–	kΩ
Small Signal Output Resistance, Single Ended	r _o	T _A = +25°C, V _{CC1} = 5V, V _{CC2} = 12V	–	15	–	Ω
Bandwidth, –3dB	BW	V _{iD} = 2mV _{RMS} , T _A = +25°C, V _{CC1} = 5V, V _{CC2} = 12V	10	–	–	MHz
Common Mode Rejection Ratio	CMRR	T _A = +25°C, f = 100kHz, A _{VD} = 40dB, v _{in} = 200mV _{P-P} , V _{CC1} = 5V, V _{CC2} = 12V	50	–	–	dB
V _{CC1} Supply Rejection Ratio		T _A = +25°C, V _{CC2} = 12V, 4.75V ≤ V _{CC1} ≤ 5.25V, A _{VD} = 40dB	50	–	–	dB
V _{CC2} Supply Rejection Ratio		T _A = +25°C, V _{CC1} = 5V, 10V ≤ V _{CC2} ≤ 14V, A _{VD} = 40dB	50	–	–	dB
Differential Output Offset	V _{DO}	T _A = +25°C, v _{iD} = v _{in} = 0V	–	–	0.4	V
Common Mode Output Offset	V _{CO}	v _{iD} = v _{in} = 0V, Differential and Common Mode	–	3.0	–	V
Differential Noise Voltage Referred to Input	e _n	T _A = +25°C, BW = 10Hz to 1MHz	–	15	–	μV _{RMS}
Supply Current	I _{CC}	V _{CC1} = 5.25V, S ₁ to Pin12 or Pin13	–	40	–	mA
		V _{CC2} = 14V	–	4.8	–	mA
Active Differentiator Section						
Differentiator Output Sink Current, Pin12 and Pin13	I _{OD}	V _{OD} = V _{CC1}	1.0	1.4	–	mA
Peak Shift	PS	Note 2	–	–	5	%
Differentiator Input Resistance, Differential	r _{iD}		–	30	–	kΩ
Differentiator Output Resistance, Differential	r _{oD}	T _A = +25°C	–	40	–	Ω

Note 2. $f = 250\text{kHz}$, $v_{iD} = 1\text{V}_{P-P}$, $i_{cap} = 500\mu\text{A}$

$$\text{where PS} = \frac{1}{2} \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$$

$$V_{CC1} = 5\text{V}, V_{CC2} = 12\text{V}$$

Electrical Characteristics (Cont'd): ($T_A = 0^\circ$ to $+70^\circ\text{C}$, $V_{CC1} = 4.75$ to 5.25V , $V_{CC2} = 10$ to 14V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Section						
Output Voltage High Logic Level, Pin10	V_{OH}	$V_{CC1} = 4.75\text{V}$, $V_{CC2} = 12\text{V}$, $I_{OH} = -0.4\text{mA}$	2.7	—	—	V
Output Voltage Low Logic Level, Pin10	V_{OL}	$V_{CC1} = 4.75\text{V}$, $V_{CC2} = 12\text{V}$, $I_{OH} = 8\text{mA}$	—	—	0.5	V
Output Rise Time, Pin10	t_{TLH}		—	—	20	ns
Output Fall Time, Pin10	t_{THL}		—	—	25	ns
Timing Range Mono #1 (t_{1A} and t_{1B})	t_{1A} , t_{1B}		500	—	4000	ns
Timing Accuracy Mono #1	E_{t1}	$t1 = 1\mu\text{s} = 0.625 R1C1 + 200\text{ns}$, Note 3, Note 4, Note 5	85	—	115	%
Timing Range Mono #2	$t2$		150	—	1000	ns
Timing Accuracy Mono #2	E_{t2}	$t2 = 200\text{ns} = 0.625 R2C2$, Note 6, Note 7	85	—	115	%

Note 3. $R1 = 6.4\text{k}\Omega$, $C1 = 200\text{pF}$.

Note 4. Accuracy guaranteed for $R1$ in the range $1.5\text{k}\Omega \leq R1 \leq 10\text{k}\Omega$ and $C1$ in the range $150\text{pF} \leq C1 \leq 680\text{pF}$.

Note 5. To minimize current transients, $C1$ should be kept as small as is convenient.

Note 6. $R2 = 1.6\text{k}\Omega$, $C2 = 200\text{pF}$.

Note 7. Accuracy guaranteed for $R2$ in the range $1.5\text{k}\Omega \leq R2 \leq 10\text{k}\Omega$ and $C2$ in the range $100\text{pF} \leq C1 \leq 800\text{pF}$.

Pin Connection Diagram



