

## NTE7133 Integrated Circuit Horizontal and Vertical Deflection Controller for VGA/XGA and Autosync Monitors

### **Description:**

The NTE7133 is an integrated circuit in a 20-Lead DIP type package. This device is designed to provide an economical solution in VGA/XGA and autosync monitors by incorporating complete horizontal and vertical small signal processing. VGA-dependent mode detection and setting are performed on-chip.

### **Features:**

- VGA Operation Fully Implemented Including Alignment-Free Vertical and E/W Amplitude Pre-Settings
- 4th VGA Mode Easy Applicable (XGA, Super VGA)
- Autosync Operation Externally Selectable
- Low Jitter
- All Adjustments DC-Controllable
- Alignment-Free Oscillators
- Sync Separators for Video or Horizontal and Vertical TTL Sync Levels Regardless of Polarity
- Horizontal Oscillator with  $P_{LL1}$  for Sync and  $P_{LL2}$  for Flyback
- Constant Vertical and E/W Amplitude in Multi-Frequency Operation
- DC-Coupling to Vertical Power Amplifier
- Internal Supply Voltage Stabilization with Excellent Ripple Rejection to Ensure Stable Geometrical Adjustments

### **Absolute Maximum Ratings:**

Supply Voltage (Pin1), $V_P$	−0.5 to +16V
Voltage (Pin3, Pin7), $V_3, V_7$	−0.5 to +16V
Voltage (Pin8), $V_8$	−0.5 to +7V
Voltage (Pin5, Pin6, Pin9, Pin10, Pin13, Pin14, Pin18), $V_n$	−0.5 to +6.5V
Current (Pin2), $I_2$	±10mA
Current (Pin3), $I_3$	100mA
Current (Pin7), $I_7$	20mA
Current (Pin8), $I_8$	−10mA
Electrostatic Handling for All Pins (Note 1), $V_{esd}$	±400V
Operating Junction Temperature, $T_J$	+150°C
Operating Ambient Temperature Range, $T_A$	0° to +70°C
Storage Temperature Range, $T_{stg}$	−55° to +150°C
Thermal Resistance, Junction-to-Ambient (In Free Air), $R_{thJA}$	65K/W

Note 1. Equivalent to discharging a 200pF capacitor through a 0Ω series resistor.

**Electrical Characteristics:** ( $V_P = 12V$ ,  $T_A = +25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
Positive Supply Voltage (Pin1)	V <sub>P</sub>		9.2	12.0	16.0	V
Supply Current	I <sub>P</sub>	I <sub>18</sub> = −1.05mA	–	36	44	mA
		I <sub>18</sub> = −3.388mA	–	40	49	mA
<b>Internal Reference Voltage</b>						
Internal Reference Voltage	V <sub>ref</sub>		6.0	6.25	6.5	V
Temperature Coefficient	TC	T <sub>A</sub> = +20° to +100°C	–	–	±90	10 <sup>−6</sup> /K
Power Supply Ripple Rejection	PSRR	f = 1kHz Sine Wave	60	75	–	dB
		f = 1MHz Sine Wave	25	35	–	dB
Supply Voltage (Pin1) to Ensure All Internal Reference Voltages	V <sub>P</sub>		9.2	–	16.0	V
<b>Composite Sync Input</b> (AC–Coupled, V <sub>10</sub> = 5V)						
Sync Amplitude of Video Input Signal (Pin9)	V <sub>i sync</sub>	Sync on Green	–	300	–	mV
Top Sync Clamping Level			1.1	1.28	1.5	V
Slicing Level Above Top Sync Level		Sync on Green, R <sub>S</sub> = 50Ω	90	120	150	mV
Allowed Source Resistance for 7% Duty Cycle	R <sub>S</sub>	V <sub>i sync</sub> > 200mV	–	–	1.5	kΩ
Differential Input Resistance	r <sub>g</sub>	During Sync	–	80	–	Ω
Charging Current of Coupling Capacitor	I <sub>g</sub>	V <sub>g</sub> > 1.5V	1.3	2.0	3.0	μA
Vertical Sync Integration Time to Generate Sync Pulse	t <sub>int</sub>	f <sub>H</sub> = 31kHz, I <sub>18</sub> = −1.050mA	7	10	13	μs
		f <sub>H</sub> = 64kHz, I <sub>18</sub> = −2.169mA	3.5	5.0	6.5	μs
		f <sub>H</sub> = 100kHz, I <sub>18</sub> = −3.388mA	2.5	3.4	4.5	μs
<b>Horizontal Sync Input</b> (DC–Coupled, TTL–Compatible)						
Sync Input Signal (Peak Value, Pin9)	V <sub>u sync</sub>		1.7	–	–	V
Slicing Level			1.2	1.4	1.6	V
Minimum Pulse Width	t <sub>p</sub>		700	–	–	ns
Rise Time and Fall Time	t <sub>r</sub> , t <sub>f</sub>		10	–	500	ns
Input Current	I <sub>g</sub>	V <sub>g</sub> = 0.8V	–	–	−200	μA
		V <sub>g</sub> 5.5V	–	–	10	μA
<b>Automatic Horizontal Polarity Switch</b> (H–Sync on Pin9)						
Horizontal Sync Pulse Width Related to t <sub>H</sub> (Duty Cycle for Automatic Polarity Correction)	t <sub>p</sub> H/t <sub>H</sub>		–	–	30	%
Delay Time for Changing Sync Polarity	t <sub>p</sub>		0.3	–	1.8	ms
<b>Vertical Sync Input</b> (DC–Coupled, TTL–Compatible,,V–Sync on Pin10)						
Sync Input Signal (Peak Value, Pin10)	V <sub>i sync</sub>		1.7	–	–	V
Slicing Level			1.2	1.4	1.6	V
Input Current	I <sub>10</sub>	0 < V <sub>10</sub> < 5.5V	–	–	±10	μA
Maximum Vertical Sync Pulse Width for Automatic Vertical Polarity Switch	t <sub>p</sub> V		–	–	300	μs
<b>Horizontal Mode Detector Output</b> (VGA Mode)						
Output Saturation Voltage LOW (For Modes 1, 2, and 3)	V <sub>7</sub>	I <sub>7</sub> = 6mA	–	0.275	0.33	V
Output Voltage HIGH		Mode 4	–	–	V <sub>P</sub>	V
Load Current to Force VGA Mode–Dependent Vertical and Parabola Amplitudes	I <sub>7</sub>	Modes 1, 2, and 3	2	–	6	mA
Output Current		Mode 4	–	0	–	mA

**Electrical Characteristics (Cont'd):** ( $V_P = 12V$ ,  $T_A = +25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VGA/Autosync Mode Switch						
Input Voltage LOW to Force Autosync Mode	V <sub>7</sub>		0	–	50	mV
Horizontal Comparator P <sub>LL1</sub>						
Upper Control Voltage Limitation	V <sub>17</sub>		–	5.9	–	V
Lower Control Voltage Limitation			–	5.1	–	V
Control Current	I <sub>17</sub>		–	±0.083I <sub>18</sub>	–	μA
Horizontal Oscillator						
Center Frequency	f <sub>OSC</sub>	R <sub>18</sub> = 2.4kΩ (Pin18), C <sub>19</sub> = 10nF (Pin19)	–	31.45	–	kHz
Deviation of Center Frequency	Δf <sub>OSC</sub>		–	–	±3.0	%
Temperature Coefficient	TC		–	+200	+300	10 <sup>–6</sup> /K
Relative Holding/Catching Range	φ <sub>H</sub> /t <sub>H</sub>		±6.0	±6.5	±7.3	%
External Oscillator Current	I <sub>18</sub>		–0.5	–	–4.3	mA
Voltage at Reference Current Input (Pin18)	V <sub>18</sub>		2.35	2.5	2.65	V
Horizontal P <sub>LL2</sub>						
Upper Clamping Level of Flyback Input	V <sub>2</sub>	I <sub>2</sub> = 6mA	–	5.5	–	V
Lower Clamping Level of Flyback Input		I <sub>2</sub> = –1mA	–	–0.75	–	V
H–Flyback Slicing Level			–	3.0	–	V
Delay Between Middle of Sync and Middle of H–Flyback Related to t <sub>H</sub>	t <sub>d</sub> /t <sub>H</sub>		–	3.0	–	%
Upper Control Voltage Limitation	V <sub>20</sub>		–	6.2	–	V
Lower Control Voltage Limitation			–	4.8	–	V
Control Current	I <sub>20</sub>		–	±0.083I <sub>18</sub>	–	μA
P <sub>LL2</sub> Control range Related to t <sub>H</sub>	Δt/t <sub>H</sub>		30	–	–	%
Horizontal Output (Open–Collector)						
Output Voltage LOW	V <sub>3</sub>	I <sub>3</sub> = 20mA	–	–	0.3	V
		I <sub>3</sub> = 60mA	–	–	0.8	V
t <sub>H</sub> Duty Cycle	t <sub>p</sub> /t <sub>H</sub>		42	45	48	%
Threshold to Activate Too Low Supply Voltage Protection	V <sub>P</sub>	Horizontal Output OFF	–	5.6	–	V
Threshold to Activate Too Low Supply Voltage Protection		Horizontal Output ON	–	5.8	–	V
Jitter of Horizontal Output	Δt <sub>H</sub>	f = 31kHz	–	–	3.5	ns
		f = 64kHz	–	–	1.9	ns
		f = 100kHz	–	–	1.2	ns
Horizontal Clamping/Blanking Generator Output						
Output Voltage LOW	V <sub>8</sub>		–	–	0.9	V
Blanking Output Voltage		Internal V Blanking	1.6	1.9	2.2	V
Clamping Output Voltage		H–Sync on Pin9	5.15	5.4	5.65	V
Internal Sink Current for All Output Levels	I <sub>8</sub>	H and V Scanning	2.3	2.9	3.5	mA
		External Load Current	–	–	–3.0	mA
Clamping Pulse Start	t <sub>8</sub>		With End of H–Sync			
Clamping Pulse Width	t <sub>clp</sub>		0.8	1.0	1.2	μs
Steepness of Rise and Fall Times	S		–	60	75	ns/V

**Electrical Characteristics (Cont'd):** ( $V_P = 12V$ ,  $T_A = +25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Vertical Oscillator (V <sub>ref</sub> = 6.25V)						
Vertical Free-Running Frequency	f <sub>o</sub>	R <sub>15</sub> = 22kΩ, C <sub>16</sub> = 0.1μF	–	42	–	Hz
Nominal Vertical Sync Range	f <sub>V</sub>	No f <sub>o</sub> Adjustment	50	–	110	Hz
Voltage on Pin15	V <sub>15</sub>	R <sub>15</sub> = 22kΩ	2.8	3.0	3.2	V
Delay Between Sync Pulse and Start of Vertical Scan in VGA/XGA Mode	t <sub>d</sub>	Measured on Pin8, Activated by an External Resistor on Pin7	500	575	650	μs
Delay Between Sync Pulse and Start of Vertical Scan in Autosync Mode		Measured on Pin8, V <sub>7</sub> < 50mV	240	300	360	μs
Control Current for Amplitude Control	I <sub>12</sub>		–	±200	–	μA
Capacitor for Amplitude Control	C <sub>12</sub>		–	–	0.18	μF
Vertical Differential Output						
Differential Output Current Between Pin5 and Pin6 (Peak-to-Peak Value)	I <sub>o</sub>	Mode 3, I <sub>13</sub> > –135μA, R <sub>15</sub> = 22kΩ	0.9	1.0	1.1	mA
Maximum Offset Current Error		I <sub>o</sub> = 1mA	–	–	±2.5	%
Maximum Linearity Error			–	–	±1.5	%
Vertical Amplitude Adjustment (In Percent of Output Signal)						
Input Voltage	V <sub>13</sub>		–	5.0	–	V
Adjustment Current	I <sub>13</sub>	I <sub>o</sub> max (100%)	–110	–120	–135	μA
		I <sub>o</sub> min (Typically 58%)	–	0	–	μA
VGA Mode-Dependent Pre-Settings Activated by an External Resistor on Pin7	ΔI <sub>o</sub> /Δt					
Mode 1		Table 2,Note 2	116.1	116.8	117.4	%
Mode 2			101.6	102.2	102.8	%
Mode 3			–	100	–	%
Mode 4			–	100	–	%
Autosync Operation (VGA Operation Disabled)		Table 2, Note 2, V <sub>7</sub> < 50mV	–	100	–	%
E/W Output (Note 2)						
Bottom Output Signal During Mid-Scan (Pin11)	V <sub>11</sub>	Internally Stabilized	1.05	1.2	1.35	V
Top Output Signal During Flyback			4.2	4.5	4.8	V
Temperature Coefficient of Output Signal	TC		–	–	250	10 <sup>–6</sup> /K
E/W Amplitude Adjustment (Parabola)						
Input Voltage (Pin14)	V <sub>14</sub>		–	5.0	–	V
Adjustment Current	I <sub>14</sub>	100% Parabola	–110	–120	–135	μA
		Typicall 28% Parabola	–	0	–	μA

Note 2.  $\Delta I_o / \Delta t$  relative to value of Mode 3.

Note 3. Parabola amplitude tracks with mode-dependent vertical amplitude but not with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to Pin14.

## **Functional Description:**

### **Horizontal Sync Separator and Polarity Correction**

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on Pin9. Video signals are clamped with top sync on 12.8V, and are sliced at 1.4V. This results in a fixed absolute slicing level of 120mV relative to top sync.

DC-coupled TTL sync signals are also sliced at 1.4V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected.

The polarity information is fed to the VGA mode detector. The corrected sync is the input signal for the vertical sync integrator and the  $P_{LL1}$  stage.

### **Vertical Sync Separator, Polarity Correction and Vertical Sync Integrator**

DC-coupled vertical TTL sync signals may be applied to Pin10. They are sliced at 1.4V. The polarity of the separated sync is detected by internal integration, then polarity is corrected. The polarity information is fed to the VGA mode detector. If Pin10 is not used, it must be connected to GND.

The separated  $V_{i\text{ sync}}$  signal from Pin10, or the integrated composite sync signal from Pin9 (TTL or video) directly triggers the vertical oscillator.

### **VGA Mode Detector and Mode Output**

The three standard VGA modes and a 4th not fixed mode are decoded by the polarities of the horizontal and the vertical sync input signals. An external resistor (from  $V_P$  to Pin7) is necessary to match this function. In all three VGA modes the correct amplitudes are activated. The presence of the 4th mode is indicated by HIGH on Pin7. This signal can be used externally to switch any horizontal or vertical parameters.

### **VGA Mode Detector Input**

For autosync operation the voltage on Pin7 must be externally forced to a level of  $< 50\text{mV}$ . Vertical amplitude pre-settings for VGA are then inhibited. The delay time between vertical trigger pulse and the start of vertical deflection changes from 575 to  $300\mu\text{s}$  ( $575\mu\text{s}$  is needed for VGA). The vertical amplitude then remains constant in a frequency range from 50 to 110Hz.

### **Clamping and V-Blanking Generator**

A combined clamping and V-blanking pulse is available on Pin8. The lower level of 1.9V is the blanking signal derived from the vertical blanking pulse from the internal vertical oscillator.

Vertical blanking equals the delay between vertical sync and the start of vertical scan. By this, an optimum blanking is achieved for VGA/XGA as well as for multi-frequency operation (selectable via Pin7).

The upper level of 5.4V is the horizontal clamping pulse with internally fixed pulse width of  $0.8\mu\text{s}$ . A mono flop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse. If composite sync is applied one clamping pulse per H-period is generated during V-sync. The pulse of the clamping pulse may change during V-sync.

### **$P_{LL1}$ Phase Detector**

The phase detector is a standard one using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to Pin17. If composite sync is applied, the distributed control voltage is corrected during V-sync.

### **Horizontal Oscillator**

This oscillator is a relaxation type and requires a fixed capacitor of 10nF at Pin19. By changing the current into Pin18 the whole frequency range from 13 to 100kHz can be covered.

The current can be generated either by a frequency to voltage converter or by a resistor. A frequency adjustment may also be added if necessary.

The  $P_{LL1}$  control voltage at Pin17 modulates via a buffer stage the oscillator thresholds. A high DC-loop gain ensures a stable phase relationship between horizontal sync and line flyback pulses.

## **Functional Description (Cont'd):**

### **P<sub>LL2</sub> Phase Detector**

This phase detector is similar to the P<sub>LL1</sub> phase detector. Line flyback signals (Pin2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.

A certain amount of phase adjustment is possible by injecting a DC current from an external source into the P<sub>LL2</sub> filter capacitor on Pin20.

### **Horizontal Driver**

This open-collector output stage (Pin3) can directly drive an external driver transistor. The saturation voltage is 300mV at 20mA. To protect the line deflection transistor, the horizontal output stage does not conduct at V<sub>P</sub> < 6.4V (Pin1).

### **Vertical Oscillator and Amplitude Control**

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions.

The free-running frequency f<sub>o</sub> is determined by the values of R<sub>VOS</sub> and C<sub>VOS</sub>. The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I<sub>5</sub> and I<sub>6</sub> are in relation to the value of R<sub>VOS</sub>. Therefore, the oscillator frequency must be determined only by C<sub>VOS</sub> on Pin16.

$$f_o = \frac{1}{10.8 \times R_{VOS} \times C_{VOS}}$$

To achieve a stabilized amplitude the free-running frequency f<sub>o</sub> (without adjustment) must be lower than the lowest occurring sync frequency. The contributions shown in Table 1 can be assumed.

**Table 1.** Calculation of f<sub>o</sub> Total Spread

Contributing Elements	%
Minimum Frequency Offset Between f <sub>o</sub> and the Lowest Trigger Frequency	10
Spread of IC	±3
Spread of R (22kΩ)	±1
Spread of C (0.1μF)	±5
Total	19

Results for 50 to 110Hz application:  $f_o = \frac{50\text{Hz}}{1.19} = 42\text{Hz}$

**Table 2.** VGA Modes

Mode	Horizontal/Vertical Sync Polarity	Horizontal Frequency (kHz)	Vertical Frequency (Hz)	Number of Active Lines	Output Mode Pin7
1	+/-	31.45	70	350	LOW
2	-/+	31.45	70	400	LOW
3	-/-	31.45	60	480	LOW
4	+/+	Fixed by External Circuitry	—	—	HIGH
Autosync	*/*	Fixed by External Circuitry	—	—	Forced to GND

### Pin Connection Diagram

$V_P$	<b>1</b>	<b>20</b>	$P_{LL2}$ Phase
Horiz Flyback Input	<b>2</b>	<b>19</b>	Horiz OSC Capacitor
Horiz Output	<b>3</b>	<b>18</b>	Horiz OSC Resistor
GND (0V)	<b>4</b>	<b>17</b>	$P_{LL1}$ Phase
Vert Output 1/Neg-Going Sawtooth	<b>5</b>	<b>16</b>	Vert OSC Capacitor
Vert Output 2/Pos-Going Sawtooth	<b>6</b>	<b>15</b>	Vert OSC Resistor
4th Mode Output/Autosync In	<b>7</b>	<b>14</b>	E/W Amp Adj Input (Parabola)
Clamping/Blanking Pulse Out	<b>8</b>	<b>13</b>	Vert Amp Adj Input
Horiz Sync/Video In	<b>9</b>	<b>12</b>	Cap for Amp Control
Vert Sync In	<b>10</b>	<b>11</b>	E/W Output (Parabola to Driver Stage)

