

NTE874 Integrated Circuit TV Horiz/Vert Countdown System Circuit

Description:

The NTE874 is a monolithic bipolar/I²L integrated circuit digital sync system designed for use in consumer TV applications for color/monochrome receivers or monitors. This device takes the composite video input signal in combination with the on-chip master-scan oscillator to provide both horizontal drive and vertical deflection output signals.

Other on-chip functions include sync separator, horizontal APC, horizontal/vertical count-down circuitry, vertical ramp generator, and horizontal drive circuit (Pulse-Width Modulator).

The NTE874 features dual-mode operation and accepts either standard or non-standard video signals. An automatic mode-recognition system forces the operation into the asynchronous mode for non-standard sync signals.

Intended for use with 525-line systems, the NTE874 is supplied in the 28-lead dual-in-line plastic package.

Features:

- Sync Separator
- Master Scan Oscillator (at $64 \times f_H$)
- Automatic Phase Control (APC) of Oscillator
- Horizontal/Vertical Count-down
- Vertical Output
- Horizontal Drive Output (Pulse-Width Modulator)

Absolute Maximum Ratings:

POWER SUPPLY:

Power Supply Voltage, V_{CC}	15V
Power Supply Current, I_{CC}	75mA
Injector Supply Voltage, V_{INJ}	1.75V
Injector Supply Current, I_{INJ}	150mA

Absolute Maximum Ratings (Cont'd):

INPUTS OUTPUTS:

AGC Gate (Pin 9) Source, I_{EAGC}	10mA
Composite Blanking (Pin 16) Sink, I_{CBLNK}	10mA
Horizontal Drive (Pin 5) Sink, I_{CHD}	50mA
Horizontal Output (Pin 3) Sink, I_{CHO}	30mA
Sync Separator Out (Pin 28), I_{SYNC}	30mA
Vertical Drive (Pin 14) Source, I_{VERT}	50mA

DEVICE DISSIPATION:

Maximum Rated Junction Temperature, T_{JMAX}	+150°C
Maximum Power Dissipation, P_D	
Up to $T_A = +50^\circ\text{C}$	1.1W
Above $T_A = +50^\circ\text{C}$	Derate linearly at 11.1 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating, T_{OP}	0° to +85°C
Storage, T_{STG}	-55° to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. ($1.59 \pm 0.79\text{mm}$) from case for 10s max.	+265°C
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Standard Operating Range:

Parameter	Symbol	PIN #	Min	Typ	Max	Units
Analog Supply Voltage	V_{CC}	7	10.9	12.0	12.9	V
Analog Supply Current	I_{CC}	7	30	45	60	mA
Injector Supply Voltage	V_{INJ}	10	1.3	1.6	1.9	V
Total Dissipation, no external loads	P_D	—	—	580	—	mW
Force Asynchronous Low ("0")	V_{FAL}	2	-0.5	0	+0.25	V
Force Asynchronous	V_{FAH}	2	0.7	0.8	1.5	V
Integrated Vertical, Low	V_{IVL}	1	—	—	1.9	V
Integrated Vertical, High	V_{IVH}	1	2.8	—	—	V

Electrical Characteristics: ($T_A = +25^\circ\text{C}$, $V_{CC} = 12V_{DC}$, $V_{25} = 12V_{DC}$, Pin 2, 15, 22 to GND;., $1\mu\text{F}$ from Pin 4 to GND., 10K ohms from Pin 28 to GND., $F_{CLK} = 1\text{MHz}$, (AC Coupled), $V_{Sync} 1.2\text{V}$ to 4V, $V_{IV} 1.9\text{V}$ to 2.8V, $V_{FA} 0.2\text{V}$ to 0.7V)

Parameter	Test Conditions	PIN #	Min	Typ	Max	Units
Power Supply Section						
Supply Current	Pin 10 Open	7	20	45	60	mA
Injector Voltage		10	1.3	1.6	1.9	V
Sync Separator/Diff. Section						
Video Inverter, High Voltage	$V_{27} = 4\text{V}$, $I_{26} = -500\mu\text{A}$	26	4.2	5.1	5.8	V
Sync Processor, Low Voltage	$V_{27} = 4\text{V}$, $I_{26} = 0\mu\text{A}$	28	—	—	.1	V
OSC/Count-Down/APC Section						
APC Bias	$V_{27} = 4\text{V}$, $I_{26} = 0\mu\text{A}$, $V_{21} = \text{Open}$	21	6.5	6.8	7.5	V

Electrical Characteristics (Cont'd): ($T_A = +25^{\circ}\text{C}$, $V_{CC} = 12\text{V}_{\text{DC}}$, $V_{25} = 12\text{V}_{\text{DC}}$, Pin 2, 15, 22 to GND., $1\mu\text{F}$ from Pin 4 to GND., 10K ohms from Pin 28 to GND., $F_{\text{CLK}} = 1\text{MHz}$, (AC Coupled), $V_{\text{Sync}} 1.2\text{V}$ to 4V , $V_{\text{IV}} 1.9\text{V}$ to 2.8V , $V_{\text{FA}} 0.2\text{V}$ to 0.7V)

Parameter	Test Conditions	PIN #	Min	Typ	Max	Units
OSC/Count–Down/APC Section (Cont'd)						
APC Discharge	$V_{27} = 4\text{V}$, $I_{26} = 0\mu\text{A}$, $V_{21} = \text{Open}$	21	6.5	6.8	7.5	V
APC Discharge	$I_{26} = -500\mu\text{A}$, $V_{20} = 2\text{V}$, $V_{21} = 2\text{V}$, $V_{21} = \text{VAPC Bias (above)}$, (Stop Clock When Pin 21 Goes Low)	21	600	803	1100	μA
APC Charge	$V_{27} = 4\text{V}$, $I_{26} = -500\mu\text{A}$, $V_{20} = 6\text{V}$, $V_{21} = \text{VAPC Bias (above)}$	21	-600	-793	-1100	μA
Phase Detector	$I_{21} = \text{APC Discharge–APC Charge}$	21	-30	9.8	30	μA
Sync Width, Wide Differentiation	$V_{27} = 5\text{V}$, $V_{23} = 1\text{MHz}$, $I_{20} = -300\mu\text{A}$, $V_{26} = \text{Sq. Wave } 0 \text{ to } 5\text{V}$ with $T_{\text{on}} = T_{\text{off}} = 31.75\mu\text{s}$	21	5	6	8	μs
Sync Width, Narrow	Same as above except $T_{\text{on}} = 2\mu\text{s}$, $T_{\text{off}} = 61.5\mu\text{s}$	21	1.8	2.3	2.6	μs
Phase Detector Bias	$V_{27} = 4\text{V}$	20	3.9	4.3	4.7	V
Oscillator Current 1	$V_{24} = 3\text{V}$, $V_{23} = 6\text{V}$ $V_{21} = 8.5\text{V}$	25	1.4	1.8	3.0	mA
OSC/Count–Down/APC Section						
Oscillator Current Ratio	$V_{24} = 3\text{V}$, $V_{23} = 6\text{V}$, $V_{21} = \text{Open}$, Measured I_{25} & Divide by Oscillator Current 1	25	.45	.5	.55	Ratio
Oscillator Bias		24	4.5	4.8	5.5	V
+Phase Input Current	$V_{24} = 0\text{V}$	24	-230	312	-570	μA
-Phase Input Current	$V_{23} = 0\text{V}$	23	-230	331	-570	μA
Flyback Charge Current	$V_{17} = 0\text{V}$, $V_{19} = 6\text{V}$	19	-400	-501	-766	μA
Flyback Discharge Current	$I_{17} = 700\mu\text{A}$, $V_{19} = 6\text{V}$	19	2	2.4	3.5	mA
Blanking/Gating Section						
Flyback Input, Low Current 1	$V_{18} = 0\text{V}$	18	-3	-1	3	μA
Flyback Input, High Current 1	$V_{18} = 2\text{V}$	18	0.8	1.6	3.8	mA
Flyback Input, Low Current 2	$V_{17} = 0\text{V}$	17	-3	-.09	3	μA
Flyback Input, High Current 2	$V_{17} = 2\text{V}$	17	0.8	1.5	1.9	mA
Blanking Voltage	$V_{18} = 2\text{V}$, $V_{23} = 1\text{MHz}$, Stop Clock when $3\text{V} < V_{16} < 5\text{V}$	16	5.8	6	6.4	V
Burst Voltage	$V_{18} = 2\text{V}$, $V_{23} = 1\text{MHz}$, Stop Clock when $V_{16} > 9\text{V}$	16	11.2	11.95	–	V
Burst Saturation Voltage	$V_{18} = 0\text{V}$ $I_{16} = 5\mu\text{A}$	16	–	.45	0.6	V

Electrical Characteristics (Cont'd): ($T_A = +25^{\circ}\text{C}$, $V_{CC} = 12\text{V}_{\text{DC}}$, $V_{25} = 12\text{V}_{\text{DC}}$, Pin 2, 15, 22 to GND;., $1\mu\text{F}$ from Pin 4 to GND., 10K ohms from Pin 28 to GND., $F_{\text{CLK}} = 1\text{MHz}$, (AC Coupled), $V_{\text{Sync}} 1.2\text{V}$ to 4V , $V_{\text{IV}} 1.9\text{V}$ to 2.8V , $V_{\text{FA}} 0.2\text{V}$ to 0.7V)

Parameter	Test Conditions	PIN #	Min	Typ	Max	Units
Blanking/Gating Section (Cont'd)						
Horizontal Blanking Starts	(See Notes: 1, 2, 4)	16	–	.07	0.6	μs
Horizontal Blanking Width	(See Notes: 2, 4, 5)	16	11.75	12.3	12.75	μs
Burst Gate Starts	(See Notes: 1, 2, 4)	16	0.15	.44	0.45	μs
Burst Gate Trailing Edge	(See Notes: 1, 2, 4)	16	8.6	–	9.8	μs
AGC Gate Starts	(See Notes: 1, 2, 4)	9	–	.37	0.9	μs
AGC Gate Width 1	(See Notes: 2, 4, 5)	9	4.25	5.3	6.25	μs
AGC Gate Width 2	(See Notes: 3, 4, 5)	9	4.25	5.2	6.25	μs
Horizontal Drive Section						
Horizontal Out, Low Voltage Start	$V_{CC} = 3\text{V}$, 50pF (Pin 3 to GND), 3.9K-ohm (Pin 3 to 3V)	3	2.8	–	–	$V_{\text{P-P}}$
Low Voltage Horizontal Period	$V_{CC} = 3\text{V}$, $V_{23} = 1\text{MHz}$, 50pF (Pin 3 to GND), 3.9K-ohm (Pin 3 to 3V) (Trigger Level 1.5V)	3	55	64	75	μs
Low Voltage Horizontal Pulse Width Symmetry	$V_{CC} = 3\text{V}$, $V_{23} = 1\text{MHz}$, 50pF (Pin 3 to GND), 3.9K-ohm (Pin 3 to 3V) (Trigger Level 1.5V) Find Pulse Width Divide by Period	3	.3	.48	.7	Ratio
Pin 4 Quiescent Voltage	$V_6 = V_8 = 6\text{V}$, $I_5 = 20\text{mA}$, Pin 4 Open		8.4	8.7	9.1	V
Horizontal Drive Saturation Voltage	$V_6 = V_8 = 6\text{V}$	5	–	174	225	mV
Horizontal Drive Symmetry	$V_6 = V_8 = 6\text{V}$, 200 ohm (Pin 5 to GND), 600 ohm (Pin 5 to V_{CC}), $V_4 = 15$, 734Hz , $2V_{\text{P-P}}$	5	26	29.5	33	μs
Horizontal Drive Ratio		3	–	64	–	μs
Horizontal Pulse Width		3	31	–	33	μs
Vertical Drive Section						
Ramp Leakage	$V_{12} = 0\text{V}$, $V_{11} = 1\text{V}$, $V_{13} = 4\text{V}$	11	–	.04	–3	μA
Mirror Ramp Current	$I_{12} = 150\mu\text{A}$, $V_{11} = 4\text{V}$, $V_{13} = 5\text{V}$	11	–	.04	–3	μA
Ramp Charging Current, VD High	$V_{12} = 0\text{V}$, $V_{11} = 0\text{V}$, $V_{13} = 5\text{V}$, Stop Clock when Pin 11 Goes High	11	–5.5	–10	–15.5	mA

Electrical Characteristics (Cont'd): ($T_A = +25^{\circ}\text{C}$, $V_{CC} = 12V_{DC}$, $V_{25} = 12V_{DC}$, Pin 2, 15, 22 to GND;., $1\mu\text{F}$ from Pin 4 to GND., $10K$ ohms from Pin 28 to GND., $F_{CLK} = 1\text{MHz}$, (AC Coupled), $V_{Sync} 1.2V$ to $4V$, $V_{IV} 1.9V$ to $2.8V$, $V_{FA} 0.2V$ to $0.7V$)

Parameter	Test Conditions	PIN #	Min	Typ	Max	Units
Vertical Drive Section (Cont'd)						
Amplifier Input Voltage Range, VD Low	100ohm (Pin 14 to GND) $V_{13} = 1.7V$, Set V_{11} for $V_{14} = 2V$ Record V_{11} , 13; Then $V_{13} = 4V$ Record V_{11} , 13; Find Difference Stop Clock When Pin Goes Low	11,13	—	—	50	mV
Vertical, On–State Voltage	$V_{12} = 0V$, $V_{11} = 3V$, $V_{13} = 5V$, $I_{14} = -45\text{ mA}$	14	1.4	—	—	V
Vertical, Off–State Current	$V_{12} = 0V$, $V_{11} = 4V$, $V_{13} = 3V$, $V_{14} = 5V$	14	—	—	2	μA
Open Loop, Small Signal Voltage Gain	100 ohm (Pin 14 to GND) $V_{13} = 2V$ Set V_{11} thru $1K$ ohm for $V_{14} = 2V$ Apply 1kHz , $1V_{RMS}$ to Pin 11 Thru $99K$ ohm and $1\mu\text{F}$ $A_{vol} = 20 \text{ LOG} V_{14}(\text{AC})/V_{11}(\text{AC}) $	11,14	24	33	39	dB
Mode Change Non–Standard IV Field Count STD/NON–STD	Sync = 9, Within IV Window (See Note 6)	11,16	5	—	7	—
Mode Change Non–Standard Vertical Sync Field Count STD/NON–STD	Sync = Less than 9	11,16	5	—	7	—
Mode Change Field Confidence Count, NON–STD/STD	Number of New Timing IV/Sync Periods to Return to STD Mode	11,16	7	—	14	—
Standard Mode Divide Ratio	$IV = 16800$ Clock Ratio Sync = 9) Serrations within 384 Clock Window (After 8 Fields, i.e: On 9th Field)	—	—	—	16800	
Standard Mode Vertical Pulse Width	(See Note 7) Number of Clock Cycles Output is On	11	383	384	387	—
Non–Standard Mode	IV Ratio Range Can Be and Cause Proper Synchronization, Except for IV Ratio Range of (16748–16832), Sync = Don't Care (After 7 Fields, i.e.: on 8th Field)	—	16160	—	17405	
Non–Standard Vertical Pulse Width	Number of Clock Cycles Output is On	11	362	364	367	—

Electrical Characteristics (Cont'd): ($T_A = +25^{\circ}\text{C}$, $V_{CC} = 12V_{DC}$, $V_{25} = 12V_{DC}$, Pin 2, 15, 22 to GND;., $1\mu\text{F}$ from Pin 4 to GND., 10K ohms from Pin 28 to GND., $F_{CLK} = 1\text{MHz}$, (AC Coupled), $V_{Sync} 1.2\text{V}$ to 4V , $V_{IV} 1.9\text{V}$ to 2.8V , $V_{FA} 0.2\text{V}$ to 0.7V)

Parameter	Test Conditions	PIN #	Min	Typ	Max	Units
Vertical Drive Section (Cont'd)						
Non-Standard Vertical Pulse Width	Sync 9 Serrations Within 384 Clock Window, Number of Clock Cycles Output is On	11	362	364	367	—
Non-Standard Mode Asynchronous Divide Ratio	No IV or Sync Applied (After 7 Fields, i.e., on 8th Field)	11, 16	—	—	21888	—
Blanking Pulse Width	—	16	1200	1216	1220	—
Noise Mode Change	IV Outside the Range of (16784–16832) Sync = 9 Serrations in 384 Clock Window Pulse Applied 2432 to 11520 After an IV, Pulse is 8 to 32 Clocks Wide. Resync results in next field and is maintained for Mode Change Confidence Count	11,16	—	—	16800	—
Force Non-Standard Mode	IV = 16800 Sync = 9 Serrations Within 384 Clock Window. VFA Open Circuit Vertical Pulse Width M Measured in Next Field.	11	362	364	367	μs

Note 1 All timing measurements are with reference to the leading edge of the fly-back pulse input to Pin 18. Fly-back pulse width is $12.00\mu\text{s}$ and it is from 0 to 5V . Fly-back pulse train should start about $500\mu\text{s}$ after the start of vertical drive pulse.

Note 2 Start of fly-back pulse is 90 degrees leading with clock.

Note 3 Start of fly-back pulse is 90 degrees lagging with clock.

Note 4 Threshold for measuring AGC gate and horizontal blanking is 3V and burst gate is at 9V .

Note 5. Timing measurements referenced to trailing edge of negative sync pulse input to Pin 26. The negative sync pulse width is $4.5\mu\text{s}$ and is from 0 to $500\mu\text{A}$, with negative leading edge delayed $0.5\mu\text{s}$ from the positive leading edge of the fly-back pulse. The input to Pin 27 is $+4V_{DC}$.

Note 6 IV Ratio same as in Non-Standard Mode Ratio Range Test.

Note 7 IV Ratio same as in Standard Mode Ratio Test.

Note 8 Burst Gate Start is with reference to trailing edge of sync pulse at Pin 26. Sync Pulse is a $500\mu\text{A}$ Sink Current at Pin 26.

Pin Connection Diagram

Integrated Vert Input	1	28	Sync Output
Mode Select	2	27	Composite Video Input
Horiz Output	3	26	Sync Sep Filter
Horiz Sawtooth Input	4	25	OSC Tank
Horiz Drive Output	5	24	OSC Tank Lag Input
B+ Adjust Ref	6	23	OSC tank Lead Input
V _{CC}	7	22	GND
Beam Current Feedback Ref	8	21	APC Filter
AGC Gate Output	9	20	Flyback Sawtooth Ramp
Shunt Reg	10	19	Flyback Sawtooth Filter
Vert Ramp Shape	11	18	Flyback Input 1
Vert Height Adjust	12	17	Flyback Input 2
Vert Feedback	13	16	Sandcastle Output
Vert Output	14	15	Vert GND

