Nordic VLSI ASA

12-Bit 20MSPS Sampling Analog-to-Digital Converter

nAD1220-18T

FEATURES

- 3.3V power supply
- SINAD min 63.2dB for f_{in} = 50MHz
- Low power (119mW @ 3.3V and 20MSPS)
- Frequency dependent biasing
- Internal, wideband Track/Hold
- Differential input
- Low input capacitance
- Power Down and Sleep Mode

APPLICATIONS

- Imaging
- Test equipment
- Computer scanners
- Wireless communication
- Powerline communication
- Set top boxes
- Video products

GENERAL DESCRIPTION

The nAD1220-18T is a compact, high-speed, low power 12-bit monolithic analog-to-digital converter, implemented in a 0.18µm single poly CMOS process with MiM capacitors and thick oxide transistor option. It has 12-bit resolution with 11 effective bits at low input frequencies, and close to 12 bit dynamic range for video frequency signals. The converter includes a high bandwidth track and hold. Using internal references, the full scale range is ±1V. The full scale range can be set between ±0.75V and ±1.0V using external references. It operates from a single 3.3V supply, while I/O is biased with 1.8V. Its low distortion and high dynamic range offers the performance needed for demanding imaging, multimedia, telecommunications and instrumentation applications. The bias current level for the ADC is automatically adjusted based on the clock input frequency. Hence, the power dissipation of the device is continuously minimised for the current operation frequency.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.97	3.3	3.63	V
I_{DD}	Supply current (30 MSPS)			36		mA
P_D	Power dissipation (15 MSPS)	Except digital output drivers		80		mW
P_D	Power dissipation (20 MSPS)	Except digital output drivers		119		mW
DNL	Differential nonlinearity	f_{IN}=0.9991MHz			±0.5	LSB
INL	Integral nonlinearity	f_{IN}=0.9991MHz			±1.0	LSB
f_S	Conversion rate			20		MHz
N	Resolution				12	bit

Table 1. Quick reference data

GENERAL DESCRIPTION (Continued)

The nAD1220-18T has a pipelined architecture - resulting in low input capacitance. Digital error correction of the 11 most significant bits ensures good linearity for input frequencies approaching Nyquist. The nAD1220-18T is compact. The core occupies less than 4mm^2 of die area in the TSMC MiM 0.18µm CMOS process with thick oxide option. The fully differential architecture makes it insensitive to substrate noise. Thus it is ideal as a mixed signal ASIC macro cell.

BLOCK DIAGRAM

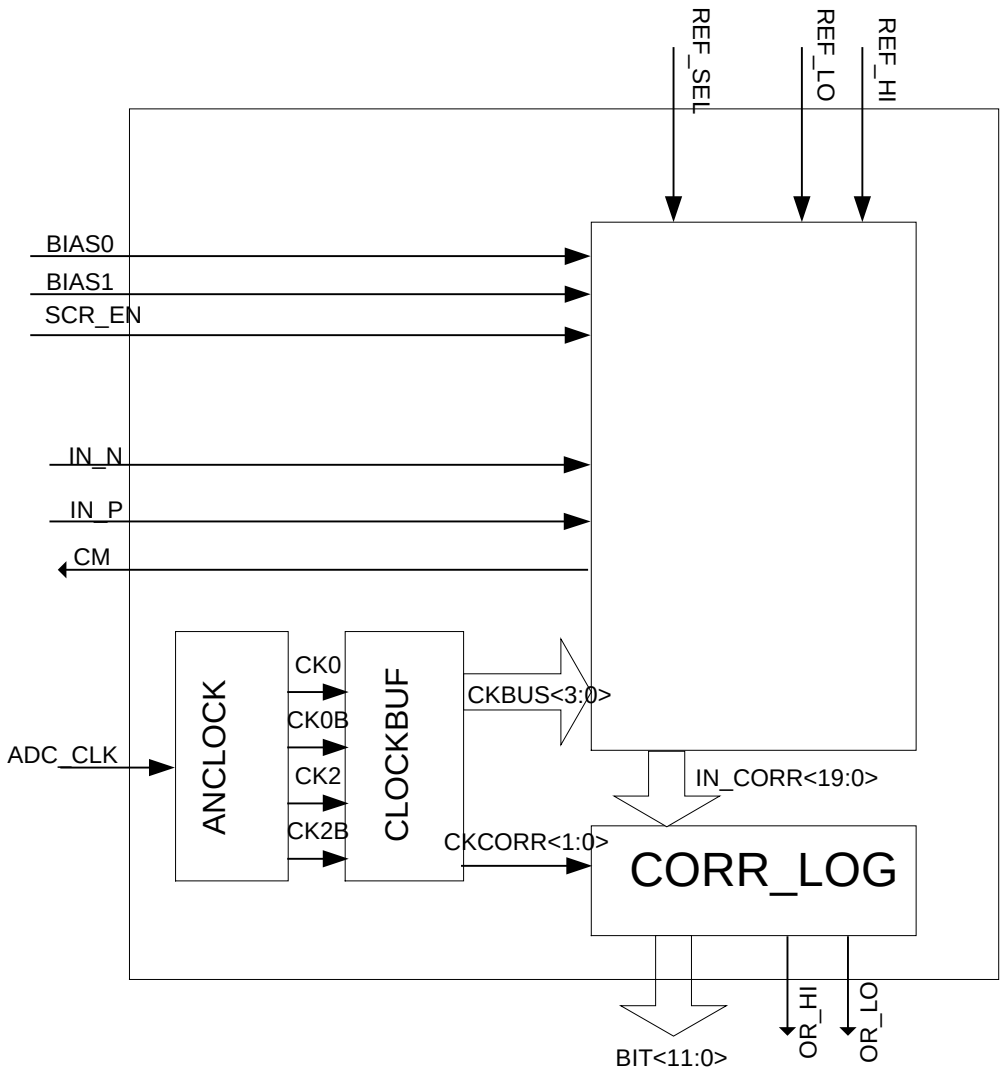

Figure 1. Block diagram nAD1220-18T

ELECTRICAL SPECIFICATIONS

(At T_A = 25°C, V_{DD} = 3.3V, Sampling Rate = 20MHz, Input frequency = 15MHz, Differential input signal, 50% duty cycle clock unless otherwise noted)

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Units
	DC Accuracy					
DNL	Differential Nonlinearity					
	f_{IN} = 0.9991 MHz	IV			±0.5	LSB
INL	Integral Nonlinearity					
	f_{IN} = 0.9991 MHz	IV			±1.0	LSB
V_{OS}	Midscale offset			± 1		%FS
CMRR	Common Mode Rejection Ratio			TBD		dB
ε_G	Gain Error			±2	±5	%FS
	Dynamic Performance					
SNR	Signal to Noise Ratio (without harmonics)					
	f_{IN} = 10 MHz	IV		69		dBFS
	f_{IN} = 50 MHz	IV		63.2		dBFS
SINAD	Signal to Noise and Distortion Ratio					
	f_{IN} = 10 MHz	IV		67		dBFS
	f_{IN} = 50 MHz	IV		63.2		
SFDR	Spurious Free Dynamic Range					
	f_{IN} = 10 MHz	IV		75		dB
	f_{IN} = 50 MHz	IV		70		dB
	Analog Input					
V_{FSR}	Input Voltage Range (differential)	IV	±0.75	±1.0	TBD	V
V_{CMI}	Common mode input voltage	IV		1.65		V
C_{INA}	Input Capacitance (from each input to ground)				150	FF
	Reference Voltages					
	Internal reference voltage drift				100	ppm/°C
V_{REFNO}	Negative Input Voltage	IV	1.05	1.15	TBD	V
V_{REFPO}	Positive Input Voltage	IV	TBD	2.15	2.25	V
V_{REFP}-V_{REFN}	Reference input voltage range [1)]	IV	0.75	0.75	TBD	V
V_{CM}	Common mode output voltage	IV	TBD	1.65	TBD	V
	Switching Performance					
F_S	Conversion Rate	IV		20		MSPS
	Pipeline Delay	IV		6		Clocks
t_{AP}	Aperture delay, IP	V		0.3		ns
t_h	Output hold time, IP	V		2.0		ns
t_d	Output delay time, IP	V		2.7		ns
t_{AP}	Aperture delay, with bonding pad	V		TBD		ns
t_h	Output hold time, with bonding pad	V		TBD		ns
t_d	Output delay time, with bonding pad	V		TBD		ns
	Digital Inputs					
V_{IL}	Logic “0” voltage	IV			0.4	V
V_{IH}	Logic “1” voltage	IV	1.62	1.8	1.98	V
I_{IL}	Logic “0” current (V_I=V_{SS})	IV			±10	µA
I_{IH}	Logic “1” current (V_I=V_{DD})	IV			±10	µA
C_{IND}	Input Capacitance	IV		TBD		pF

(table continued on next page)

	Digital Outputs					
V_{OL}	Logic "0" voltage (I = 2 mA)	IV		0.2	0.4	V
V_{OH}	Logic "1" voltage (I = 2 mA)	IV	85% OV_{DD}	90% OV_{DD}		V
	Power Supply					
V_{DD}	Supply voltage	V	2.97	3.3	3.63	V
I_{DD}	Supply current (except digital output)	IV		36		mA
V_{SS}	Supply voltage			GND		
P_D	Power dissipation (except digital output) (15 MSPS)	IV		80		mW
P_D	Power dissipation (except digital output) (30 MSPS)	IV		119		mW
P_D	Power dissipation (except digital output) Power Down Mode [2]	IV		TBD		µW
P_D	Power dissipation (except digital output) Sleep Mode	IV		TBD		µW
AV_{DD}-DV_{DD1}	Analog power – digital power pins		-0.2		+0.2	V
OV_{DD}	Output driver supply voltage		1.62	1.8	1.98	V
T	Ambient operating temperature		-40		+85	°C

Table 2. Electrical specifications

[1] See Figure 5.
[2] Power Down Mode is only available for IP version of nAD1220-18T.

Test Levels

Test Level I: 100% production tested at +25°C
Test Level II: 100% production tested at +25°C and sample tested at specified temperatures
Test Level III: Sample tested only
Test Level IV: Parameter is guaranteed by design and characterization testing
Test Level V: Parameter is typical value only
Test Level VI: 100% production tested at +25°C. Guaranteed by design and characterization testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply voltages
AV_{DD} ..... - 0.2V to +2.2V
DV_{DD1} ..... - 0.2V to V_{DD} + 0.2V
OV_{DD} ..... - 0.2V to V_{DD} + 0.2V

Input voltages
Analog In..... - 0.2V to AV_{DD} + 0.2V
Digital In..... - 0.2V to V_{DD} + 0.2V
REF_P..... - 0.2V to AV_{DD} + 0.2V
REF_N ..... - 0.2V to AV_{DD} + 0.2V
CLOCK ..... - 0.2V to V_{DD} + 0.2V

Temperatures
Operating Temperature ….-40 to +85°C
Storage Temperature..... - 65 to +125°C

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
IN_P IN_N	Differential input signal pins. Common mode voltage: 2.5V
REF_{HI} REF_{LO}	Reference input pins. Bypass with 100nF capacitors close to the pins. See Application Information below.
BIAS0, BIAS1	Digital inputs for max. sampling rate programming. BIAS1=0, BIAS0=0: Sleep mode (power save) BIAS1=0, BIAS0=1: - 12.5% bias BIAS1=1, BIAS0=0: +12.5% bias BIAS1=1, BIAS0=1: Typ. Bias The bias setting is automatically performed based on the clock input frequency. This function should be used ONLY if another bias setting than typical must be used.
ADC_CLK	Clock input
CM	Common mode voltage output
BIT11 - BIT0	Digital outputs (MSB to LSB)
SCR_EN	Enable scrambling algorithm
REF_SEL	Disable internal references
OR_HI, OR_LO	Overflow HIGH input Overflow LOW input
V_{DD}	Power pins for on chip power
V_{SS}	Ground pins
OV_{DD}	Power pins for output drivers

Table 3. Pin functions

PIN ASSIGNMENT

(TBD)

Figure 2. Pin assignment for the package used for samples

IP BLOCK LAYOUT

(TBD)

Figure 3. Size and pin placement for nAD1220-18T.
The height and width of the layout is X =2000µm and Y=1550µm respectively in the 0.18µm CMOS process.

TIMING DIAGRAM

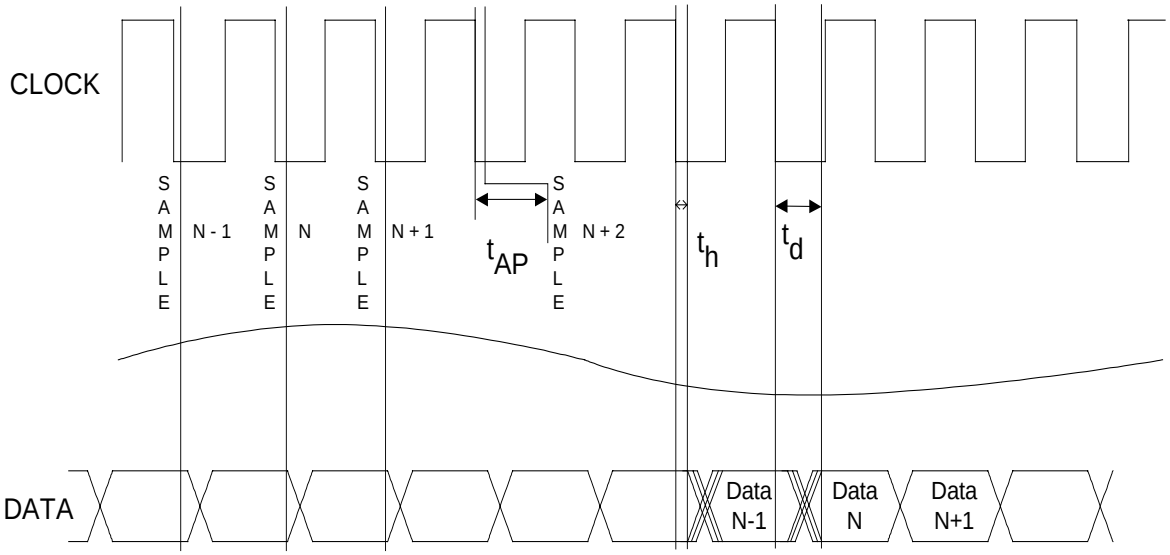

Figure 4. Timing diagram IP version

INPUT SIGNAL RANGE

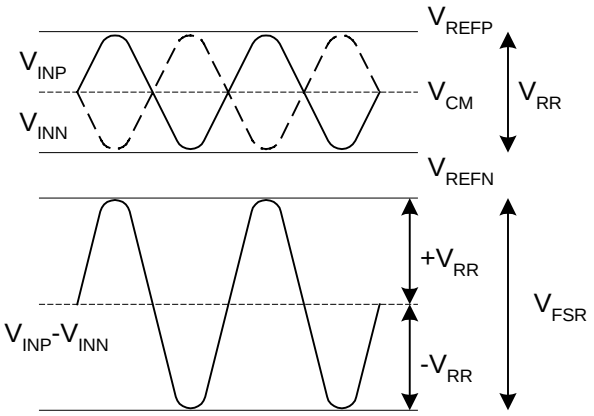

Figure 5. Definition of full scale range

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 4. Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION

References

The nAD1220-18T has a differential analog input. The input range is determined by the voltages V_{REFP} and V_{REFN} applied to reference pins REFP and REFN respectively, and is equal to $\pm(V_{REFP}-V_{REFN})$. Externally generated reference voltages connected to REFP and REFN should be symmetrical around 1.65V. The input range can be defined between ±0.5V and ±0.75V. The references should be bypassed as close to the converter pins as possible using 100nF capacitors in parallel with smaller capacitors (e.g. 1nF) (to ground).

Analog input

The input of the nAD1220-18T can be configured in various ways - dependent upon whether a single ended or differential, AC- or DC-coupled input is wanted.

AC-coupled input is most conveniently implemented using a transformer with a center tapped secondary winding. The center tap is connected to the CM-node, as shown in figure 6. In order to obtain low distortion, it is important that the selected transformer does not exhibit core saturation at full-scale. Excellent results are obtained with the Mini Circuits T1-6T or T1-1T. Proper termination of the input is important for input signal purity. A small capacitor across the inputs attenuates kickback-noise from the sample and hold. Series resistors as shown in Figure 6 may be advantageous to improve linearity. The VCM-node should be bypassed to ground as closed to the converter pin as possible using 100nF capacitors in parallel with a small one.

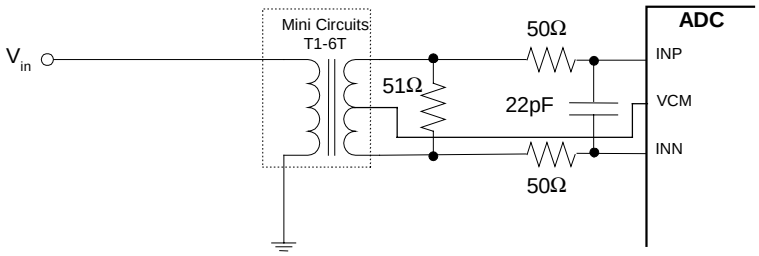

Figure 6. Example of AC coupled input using transformer configuration

If a DC-coupled single ended input is wanted, a solution based on operational amplifiers - as shown in Figure 7, is usually preferred. The AD826 is suggested for low distortion and video bandwidth. Lower cost operational amplifiers may be used if the demands are less strict. A good alternative for high performance applications is to use AD8138 single ended to differential amplifier.

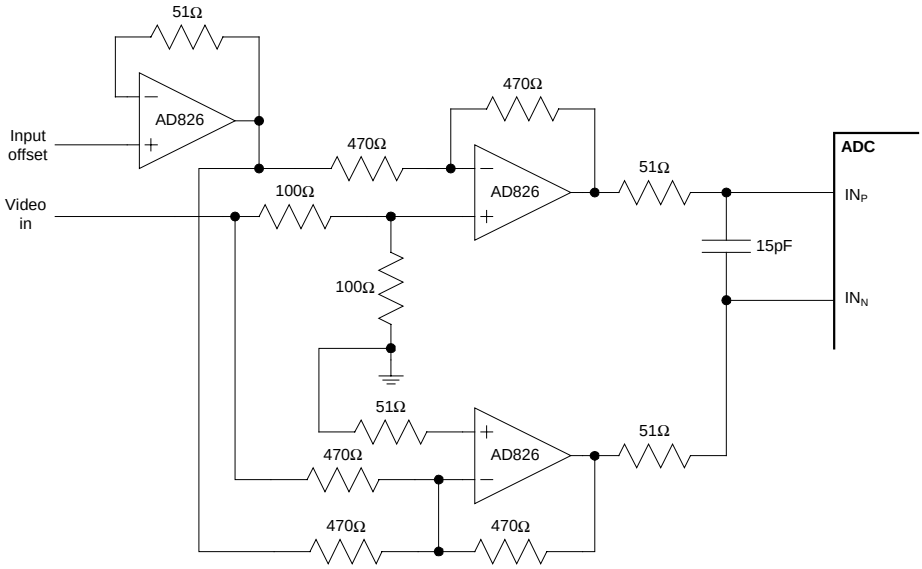

Figure 7. DC-coupled single ended to differential conversion (power supplies and bypassing not shown)

Clock

In order to preserve accuracy at high input frequency, it is important that the clock has low jitter and steep edges. Rise/fall times should be kept shorter than 2ns whenever possible. Overshoot should be avoided. Low jitter is especially important when converting high frequency input signals. Jitter causes the noise floor to rise proportionally to input signal frequency. Jitter may be caused by crosstalk on the PCB. It is therefore recommended that the clock trace on the PCB is made as short as possible.

Digital outputs

The digital output data appears in offset binary code at CMOS logic levels. Full-scale negative input results in output code 000...0. Full-scale positive input results in output code 111...1. Output data are available 6 clock cycles after the data are sampled. The analog input is sampled one aperture delay (t_{AP}) after the high to low clock transition. Output data should be sampled as shown in the timing diagram.

PCB layout and decoupling

A well designed PCB is necessary to get good spectral purity from any high performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC are connected to the analog ground plane. It is our experience that this gives the best performance. The power supply pins should be bypassed using 100nF surface mounted capacitors as close to the package pins as possible. Analog and digital supply pins should be separately filtered.

Dynamic testing

Careful testing using high quality instrumentation is necessary to achieve accurate test results on high speed A/D-converters. It is important that the clock source and signal source has low jitter. A spectrally pure, low noise RF signal generator - such as the HP8662A or HP8644B is recommended for the test signal. Low pass filtering or band pass filtering of the input signal is usually necessary to obtain the required spectral purity (SFDR > 75dB). The clock signal can be obtained from either a crystal oscillator or a low-jitter pulse generator. Alternatively, a low-jitter RF-generator can be used as a clock source. At Nordic VLSI, the Marconi Instruments 2041A is used. The sinewave clock must then be applied to an ultra high-speed comparator (e.g. AD9696) and a TTL to CMOS level shifter (e.g. 74LV04) before application to the converter. The most consistent results are obtained if the clock signal is phase locked to the input signal. Phase locking allows testing without windowing of output data. A logic analyzer with deep memory - such as the HP16500-series, is recommended for test data acquisition.

Power Down Mode and Sleep Mode

The nAD1220-18T has both Power Down Mode and Sleep Mode. The Power Down Mode can be used when the ADC should be put to ‘zero current consumption’ state and when a somewhat longer startup time is allowed. The Sleep Mode can be used to put the ADC in an ‘idle’ state and when the application require a quick startup. The two different power consumption saving schemes can be activated through the PD, BIAS0 and BIAS1 pins/connections in the following manner:

Power Down Mode: (TBD)
Sleep Mode: (TBD)

The actual startup time from these modes are dependent on the external decopling configuration.

DESIGN CENTER

Nordic VLSI ASA
Vestre Rosten 81
N-7075 TILLER
NORWAY
Telephone: +47 72898900
Telefax: +47 72898989

E-mail: For further information regarding our state of the art data converters, please e-mail us at datacon@nvlsi.no.

World Wide Web/Internet: Visit our site at http://www.nvlsi.no.

ORDERING INFORMATION

Type number	Description	Price	Available
nAD1220-18T-IC	nAD1220-18T sample in SSOP28 package (limited availability)	USD 50	January 15th, 2002
nAD1220-18T-EVB	nAD1220-18T evaluation board including characterisation report and user guide	USD 300	January 15th, 2002

Table 5. Ordering information

Product Specification. Revision Date: September 11th, 2001