

Complementary Silicon Power Transistors

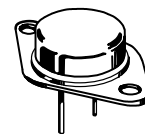
The 2N3773 and 2N6609 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested) 150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
 - $h_{FE} = 15$ (Min) @ 8 A, 4 V
 - $V_{CE(sat)} = 1.4$ V (Max) @ $I_C = 8$ A, $I_B = 0.8$ A
- For Low Distortion Complementary Designs

NPN
2N3773*
PNP
2N6609

*Motorola Preferred Device

16 AMPERE
COMPLEMENTARY
POWER TRANSISTORS
140 VOLTS
150 WATTS



CASE 1-07
TO-204AA
(TO-3)

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Emitter Voltage	V_{CEX}	160	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous — Peak (1)	I_C	16 30	Adc
Base Current — Continuous — Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 0.855	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	$^\circ\text{C/W}$

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

2N3773 2N6609**ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector–Emitter Breakdown Voltage ($I_C = 0.2\text{ A dc}$, $I_B = 0$)	$V_{CEO(sus)}$	140	—	Vdc
*Collector–Emitter Sustaining Voltage ($I_C = 0.1\text{ A dc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $R_{BE} = 100\text{ Ohms}$)	$V_{CEX(sus)}$	160	—	Vdc
Collector–Emitter Sustaining Voltage ($I_C = 0.2\text{ A dc}$, $R_{BE} = 100\text{ Ohms}$)	$V_{CER(sus)}$	150	—	Vdc
*Collector Cutoff Current ($V_{CE} = 120\text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	10	mAdc
*Collector Cutoff Current ($V_{CE} = 140\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 140\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— —	2 10	mAdc
Collector Cutoff Current ($V_{CB} = 140\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	2	mAdc
*Emitter Cutoff Current ($V_{BE} = 7\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5	mAdc

ON CHARACTERISTICS (1)

DC Current Gain *($I_C = 8\text{ A dc}$, $V_{CE} = 4\text{ Vdc}$) ($I_C = 16\text{ A dc}$, $V_{CE} = 4\text{ Vdc}$)	h_{FE}	15 5	60 —	—
Collector–Emitter Saturation Voltage *($I_C = 8\text{ A dc}$, $I_B = 800\text{ mAdc}$) ($I_C = 16\text{ A dc}$, $I_B = 3.2\text{ A dc}$)	$V_{CE(sat)}$	— —	1.4 4	Vdc
*Base–Emitter On Voltage ($I_C = 8\text{ A dc}$, $V_{CE} = 4\text{ Vdc}$)	$V_{BE(on)}$	—	2.2	Vdc

DYNAMIC CHARACTERISTICS

Magnitude of Common–Emitter Small–Signal, Short–Circuit, Forward Current Transfer Ratio ($I_C = 1\text{ A}$, $f = 50\text{ kHz}$)	$ h_{fe} $	4	—	—
*Small–Signal Current Gain ($I_C = 1\text{ A dc}$, $V_{CE} = 4\text{ Vdc}$, $f = 1\text{ kHz}$)	h_{fe}	40	—	—

SECOND BREAKDOWN CHARACTERISTICS

Second Breakdown Collector Current with Base Forward Biased $t = 1\text{ s}$ (non–repetitive), $V_{CE} = 100\text{ V}$, See Figure 12	$I_{S/b}$	1.5	—	Adc
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(1) Pulse Test: Pulse Width = $300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

* Indicates JEDEC Registered Data.

NPN

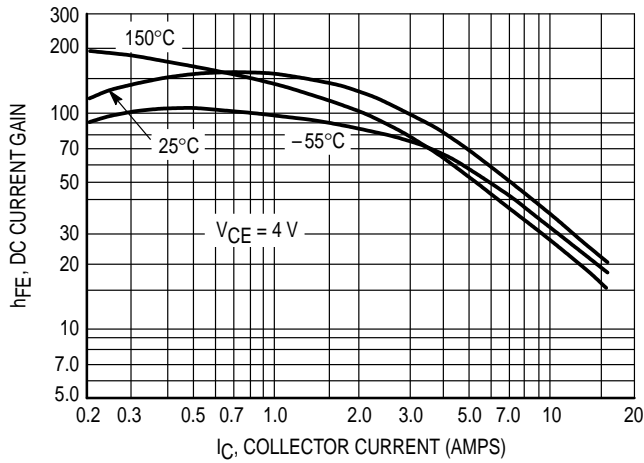


Figure 1. DC Current Gain

PNP

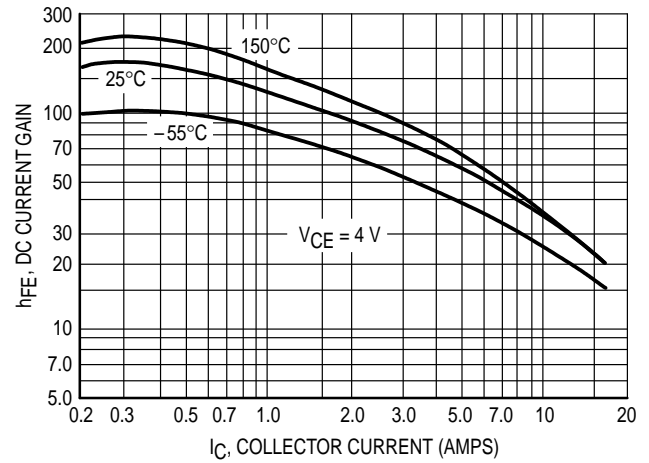


Figure 2. DC Current Gain

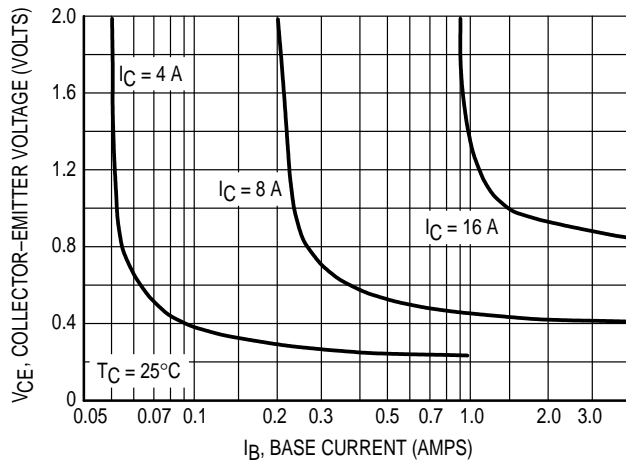


Figure 3. Collector Saturation Region

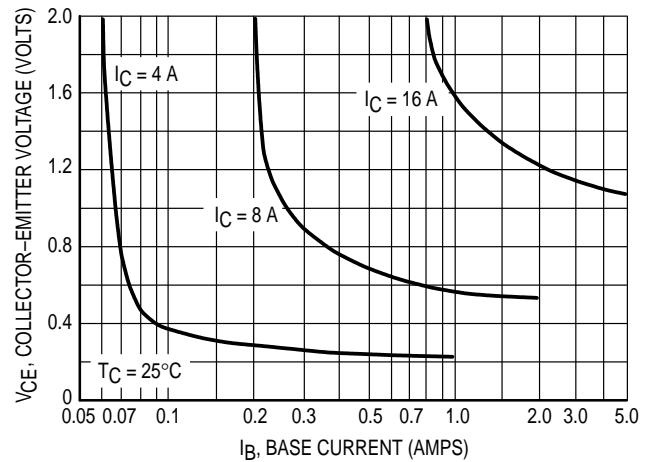


Figure 4. Collector Saturation Region

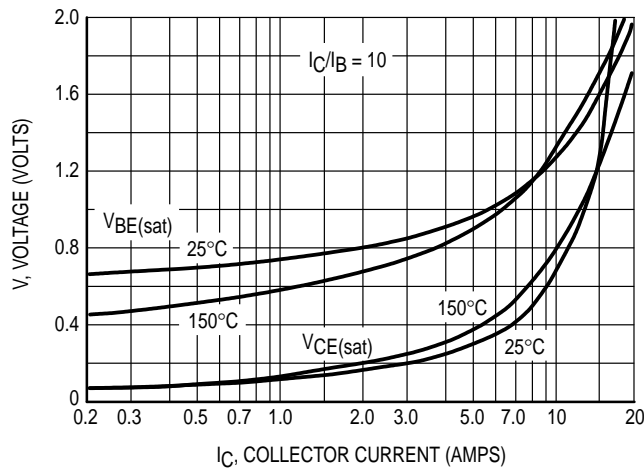


Figure 5. "On" Voltage

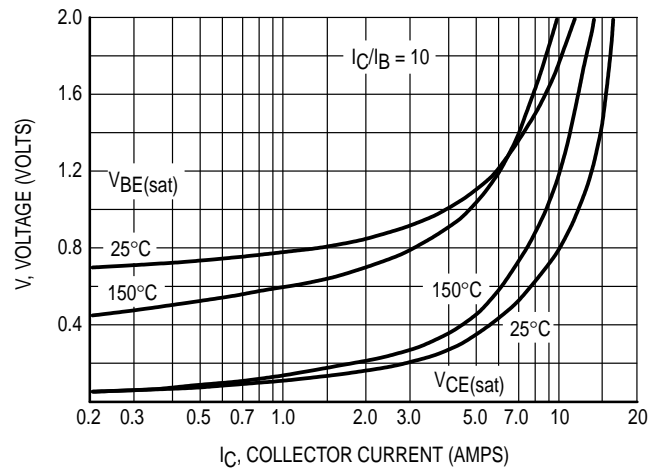


Figure 6. "On" Voltage

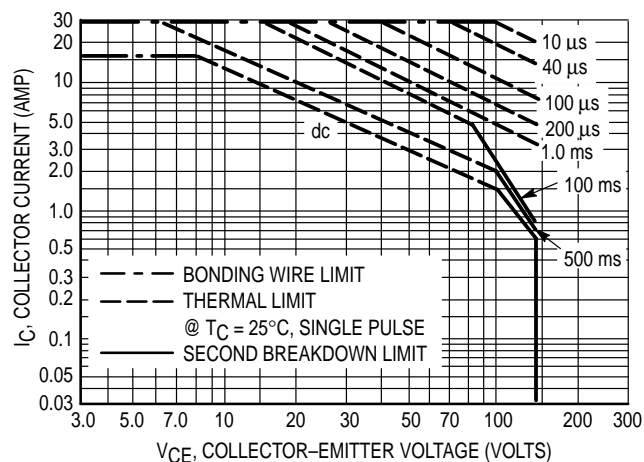


Figure 7. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

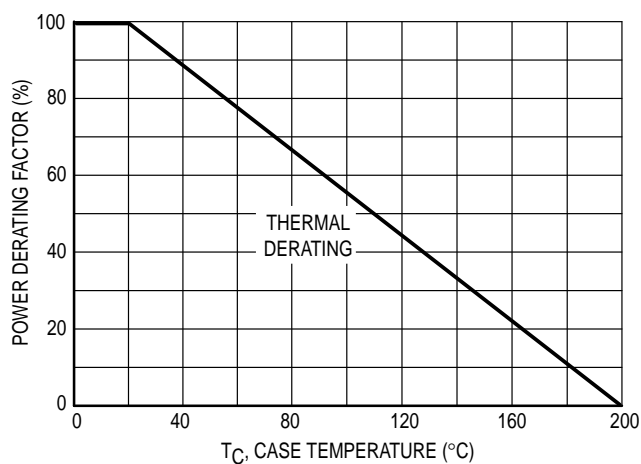
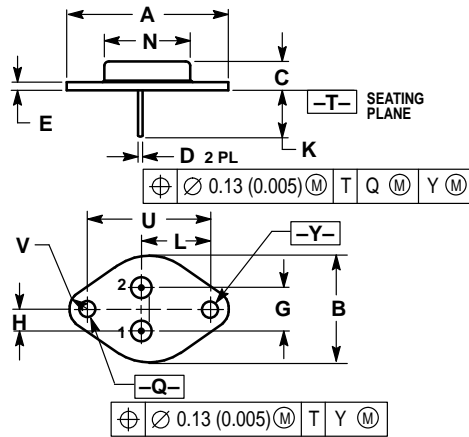


Figure 8. Power Derating

PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77


STYLE 1:

PIN 1. BASE

2. EMITTER

CASE: COLLECTOR

CASE 1-07
TO-204AA (TO-3)
ISSUE Z

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