

# Hex Schmitt Inverter With 5V-Tolerant Inputs

The MC74LVX14 is an advanced high speed CMOS Schmitt inverter. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

The MC74LVX14 is pin and functionally compatible to the MC74LVX04, but the inputs have hysteresis and, with its Schmitt trigger function, can be used as a line receiver which will receive slow input signals.

- High Speed:  $t_{PD} = 6.8\text{ns}$  (Typ) at  $V_{CC} = 3.3\text{V}$
- Low Power Dissipation:  $I_{CC} = 2\mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5\text{V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

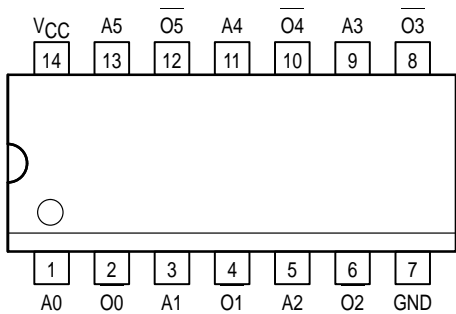


Figure 1. 14-Lead Pinout (Top View)

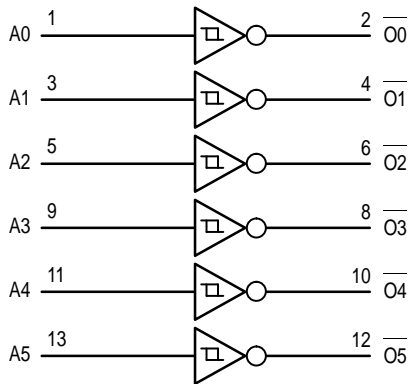


Figure 2. Logic Diagram

MC74LVX14

LVX

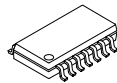
LOW-VOLTAGE CMOS



D SUFFIX  
14-LEAD SOIC PACKAGE  
CASE 751A-03



DT SUFFIX  
14-LEAD TSSOP PACKAGE  
CASE 948G-01



M SUFFIX  
14-LEAD SOIC EIAJ PACKAGE  
CASE 965-01

## PIN NAMES

Pins	Function
$\overline{A_n}$	Data Inputs
$\overline{O_n}$	Outputs

## FUNCTION TABLE

$\overline{A_n}$	$\overline{O_n}$
L	H
H	L



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	−0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	−0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	−0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	−20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	−65 to +150	°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	−40	+85	°C

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>T+</sub>	Positive Threshold Voltage (Figure 5)		3.0			2.20		2.20	V
V <sub>T−</sub>	Negative Threshold Voltage (Figure 5)		3.0	0.90			0.90		V
V <sub>H</sub>	Hysteresis Voltage (Figure 5)		3.0	0.30		1.20	0.30	1.20	V
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OH</sub> = −50μA I <sub>OH</sub> = −50μA I <sub>OH</sub> = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50μA I <sub>OL</sub> = 50μA I <sub>OL</sub> = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6			2.0		20.0	μA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, Input to Output	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		8.7 11.2	16.3 19.8	1.0 1.0	19.5 23.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		6.8 9.3	10.6 14.1	1.0 1.0	12.5 16.0	
$t_{OSHL}$ $t_{OSLH}$	Output-to-Output Skew (Note NO TAG)	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ $C_L = 50\text{pF}$			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

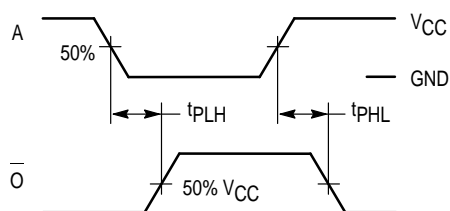
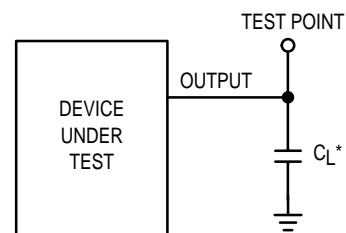
**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
$C_{in}$	Input Capacitance		4	10		10	pF
$C_{PD}$	Power Dissipation Capacitance (Note NO TAG)		21				pF

2.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/6$  (per buffer).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

**NOISE CHARACTERISTICS** (Input  $t_r = t_f = 3.0\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $V_{CC} = 3.3\text{V}$ , Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.3	0.5	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.3	-0.5	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.9	V

**Figure 3. Switching Waveforms**

\* Includes all probe and jig capacitance

**Figure 4. Test Circuit**

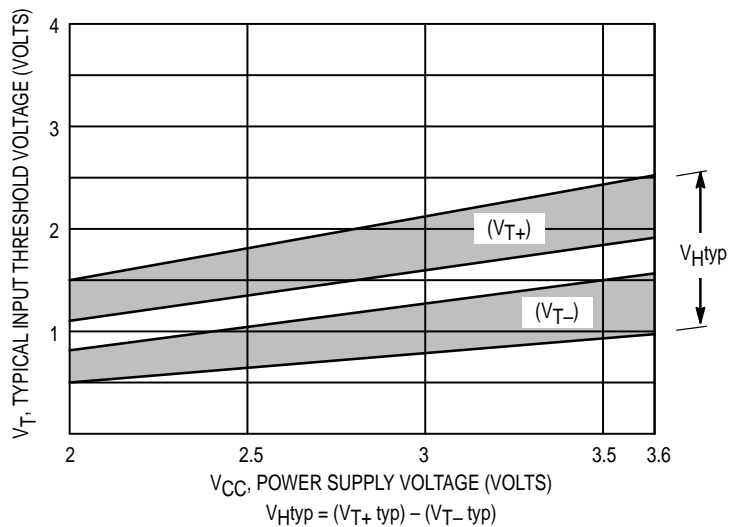
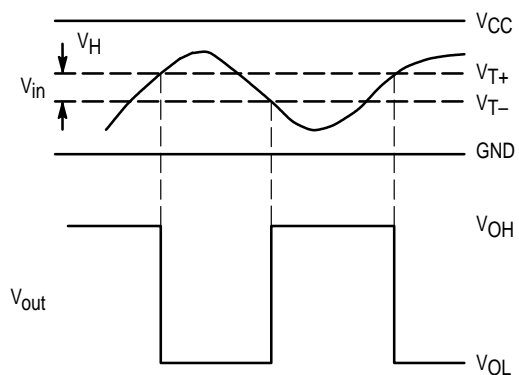


Figure 5. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$  versus Power Supply Voltage

(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

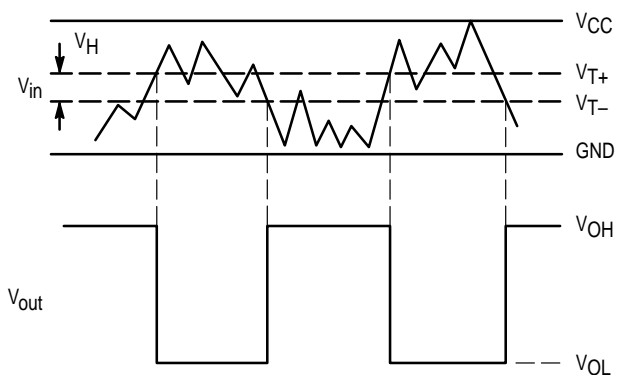
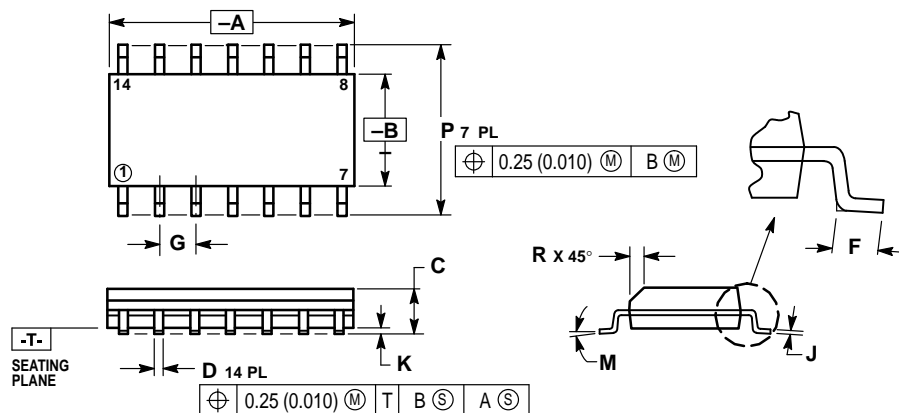


Figure 6. Typical Schmitt-Trigger Applications

## OUTLINE DIMENSIONS

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751A-03**  
**ISSUE F**

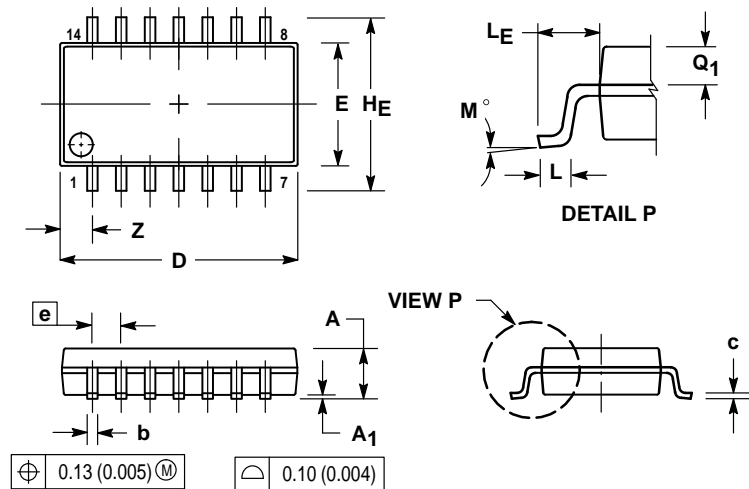


## NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

**M SUFFIX**  
**PLASTIC SOIC EIAJ PACKAGE**  
**CASE 965-01**  
**ISSUE O**



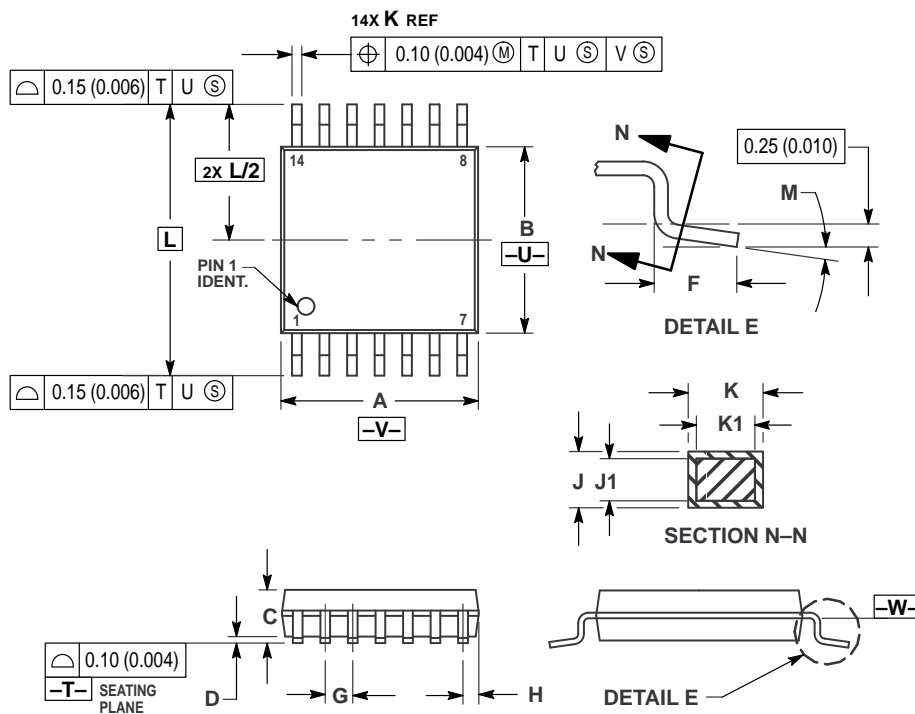
## NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

## OUTLINE DIMENSIONS


**DT SUFFIX**  
**PLASTIC TSSOP PACKAGE**  
**CASE 948G-01**  
**ISSUE O**



## NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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