CS1124

Dual Variable-Reluctance Sensor Interface IC

The CS1124 is a monolithic integrated circuit designed primarily to condition signals used to monitor rotating parts.

The CS1124 is a dual channel device. Each channel interfaces to a Variable Reluctance Sensor, and monitors the signal produced when a metal object is moved past that sensor. An output is generated that is a comparison of the input voltage and the voltage produced at the IN_{Adj} lead. The resulting square–wave is available at the OUT pin.

When the DIAG pin is high, the reference voltage at IN_{Adj} is increased. This then requires a larger signal at the input to trip the comparator, and provides for a procedure to test for an open sensor.

Features

- Dual Channel Capability
- Built–In Test Mode
- On–Chip Input Voltage Clamping
- Works from 5.0 V Supply
- Accurate Built–In Hysteresis

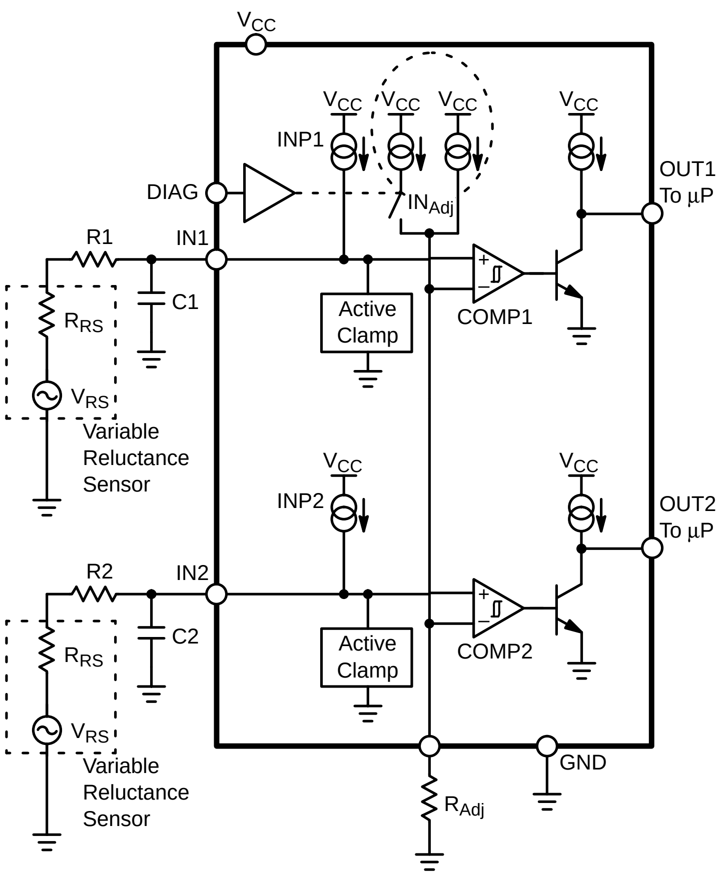

Figure 1. Block Diagram

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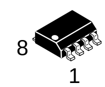
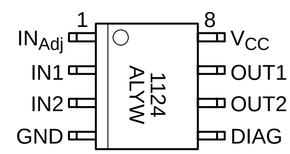


SO–8
D SUFFIX
CASE 751

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS1124YD8	SO–8	95 Units/Rail
CS1124YDR8	SO–8	2500 Tape & Reel

MAXIMUM RATINGS*

Rating		Value	Unit
Storage Temperature Range		–65 to 150	°C
Ambient Operating Temperature		–40 to 125	°C
Supply Voltage Range (continuous)		–0.3 to 7.0	V
Input Voltage Range (at any input, R1 = R2 = 22 k)		–250 to 250	V
Maximum Junction Temperature		150	°C
ESD Susceptibility (Human Body Model)		2.0	kV
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (4.5 V < V_{CC} < 5.5 V, –40°C < T_A < 125°C, V_{DIAG} = 0; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{CC} SUPPLY					
Operating Current Supply	V_{CC} = 5.0 V	–	–	5.0	mA
Sensor Inputs					
Input Threshold – Positive	V_{DIAG} = Low V_{DIAG} = High	135 135	160 160	185 185	mV mV
Input Threshold – Negative	V_{DIAG} = Low V_{DIAG} = High	–185 135	–160 160	–135 185	mV mV
Input Bias Current (INP1, INP2)	V_{IN} = 0.336 V	–16	–11	–6.0	µA
Input Bias Current (DIAG)	V_{DIAG} = 0 V	–	–	1.0	µA
Input Bias Current Factor (K_I) (IN_{Adj} = INP × K_I)	V_{IN} = 0.336 V, V_{DIAG} = Low V_{IN} = 0.336 V, V_{DIAG} = High	– 152	100 155	– 157	%INP %INP
Bias Current Matching	INP1 or INP2 to IN_{Adj}, V_{IN} = 0.336 V	–1.0	0	1.0	µA
Input Clamp – Negative	I_{IN} = –50 µA I_{IN} = –12 mA	–0.5 –0.5	–0.25 –0.30	0 0	V V
Input Clamp – Positive	I_{IN} = +12 mA	5.0	7.0	9.0	V
Output Low Voltage	I_{OUT} = 1.6 mA	–	0.2	0.4	V
Output High Voltage	I_{OUT} = –1.6 mA	V_{CC} – 0.5	V_{CC} – 0.2	–	V
Mode Change Time Delay	–	0	–	20	µs
Input to Output Delay	I_{OUT} = 1.0 mA	–	1.0	20	µs
Output Rise Time	C_{LOAD} = 30 pF	–	0.5	2.0	µs
Output Fall Time	C_{LOAD} = 30 pF	–	0.05	2.0	µs
Open–Sensor Positive Threshold	V_{DIAG} = High, $R_{IN(Adj)}$ = 40 k. Note 2	29.4	54	86.9	kΩ
Logic Inputs					
DIAG Input Low Threshold	–	–	–	0.2 × V_{CC}	V
DIAG Input High Threshold	–	0.7 × V_{CC}	–	–	V
DIAG Input Resistance	V_{IN} = 0.3 × V_{CC} , V_{CC} = 5.0 V V_{IN} = V_{CC}, V_{CC} = 5.0 V	8.0 8.0	22 22	70 70	kΩ kΩ

2. This parameter is guaranteed by design, but not parametrically tested in production.

PACKAGE PIN DESCRIPTION*

PACKAGE PIN #		
SO–8	PIN SYMBOL	FUNCTION
1	IN_{Adj}	External resistor to ground that sets the trip levels of both channels. Functions for both diagnostic and normal mode.
2	IN1	Input to channel 1.
3	IN2	Input to channel 2.
4	GND	Ground.
5	DIAG	Diagnostic mode switch. Normal mode is low.
6	OUT2	Output of channel 2.
7	OUT1	Output of channel 1.
8	V_{CC}	Positive 5.0 volt supply input.

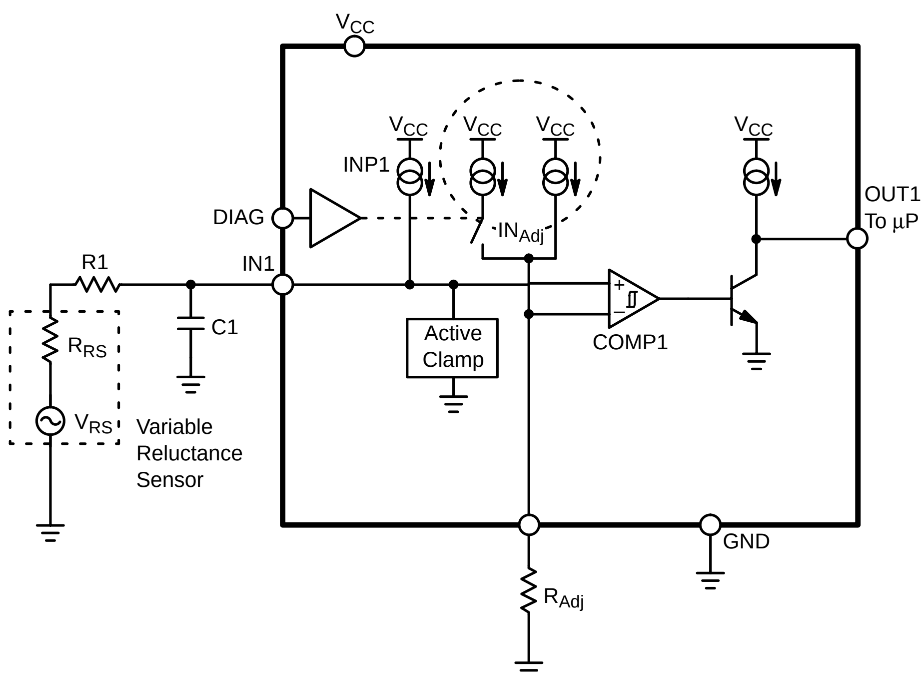


Figure 2. Application Diagram

THEORY OF OPERATION

NORMAL OPERATION

Figure 2 shows one channel of the CS1124 along with the necessary external components. Both channels share the IN_{Adj} pin as the negative input to a comparator. A brief description of the components is as follows:

V_{RS} – Ideal sinusoidal, ground referenced, sensor output – amplitude usually increases with frequency, depending on loading.

R_{RS} – Source impedance of sensor.

$R1/R_{Adj}$ – External resistors for current limiting and biasing.

$INP1/IN_{Adj}$ – Internal current sources that determine trip points via $R1/R_{Adj}$.

COMP1 – Internal comparator with built–in hysteresis set at 160 mV.

OUT1 – Output 0 V – 5.0 V square wave with the same frequency as V_{RS}.

By inspection, the voltage at the (+) and (–) terminals of COMP1 with V_{RS} = 0V are:

$$V^{+} = INP1(R1 + R_{RS}) \qquad (1)$$

$$V^{-} = IN_{Adj} \times R_{Adj} \quad (2)$$

As V_{RS} begins to rise and fall, it will be superimposed on the DC biased voltage at V^{+}.

$$V^{+} = INP1(R1 + R_{RS}) + V_{RS} \quad (3)$$

To get comparator COMP1 to trip, the following condition is needed when crossing in the positive direction,

$$V^{+} > V^{-} + V_{HYS} \quad (4)$$

(V_{HYS} is the built–in hysteresis set to 160 mV), or when crossing in the negative direction,

$$V^{+} < V^{-} - V_{HYS} \quad (5)$$

Combining equations 2, 3, and 4, we get:

$$INP1(R1 + R_{RS}) + V_{RS} > IN_{Adj} \times R_{Adj} + V_{HYS} \quad (6)$$

therefore,

$$V_{RS(+TRP)} < IN_{Adj} \times R_{Adj} - INP1(R1 + R_{RS}) + V_{HYS} \quad (7)$$

It should be evident that tripping on the negative side is:

$$V_{RS(–TRP)} < IN_{Adj} \times R_{Adj} - INP1(R1 + R_{RS}) - V_{HYS} \quad (8)$$

In normal mode,

$$INP1 = IN_{Adj} \quad (9)$$

We can now re–write equation (7) as:

$$V_{RS(+TR)} > INP1(R_{Adj} - R1 - R_{RS}) + V_{HYS} \quad (10)$$

By making

$$R_{Adj} = R1 + R_{RS} \quad (11)$$

you can detect signals with as little amplitude as V_{HYS}.

A design example is given in the applications section.

OPEN SENSOR PROTECTION

The CS1124 has a DIAG pin that when pulled high (5.0 V), will increase the IN_{Adj} current source by roughly 50%.

Equation (7) shows that a larger $V_{RS(+TRP)}$ voltage will be needed to trip comparator COMP1. However, if no V_{RS} signal is present, then we can use equations 1, 2, and 4 (equation 5 does not apply in this mode) to get:

$$INP1(R1 + R_{RS}) > INP1 \times K_{I} \times R_{Adj} + V_{HYS} \quad (12)$$

Since R_{RS} is the only unknown variable we can solve for R_{RS},

$$R_{RS} = \frac{INP1 \times K_{I} \times R_{Adj} + V_{HYS}}{INP1} - R1 \quad (13)$$

Equation (13) shows that if the output switches states when entering the diag mode with $V_{RS} = 0$, the sensor impedance must be greater than the above calculated value. This can be very useful in diagnosing intermittent sensor.

INPUT PROTECTION

As shown in Figure 2, an active clamp is provided on each input to limit the voltage on the input pin and prevent substrate current injection. The clamp is specified to handle ±12 mA. This puts an upper limit on the amplitude of the sensor output. For example, if R1 = 20 k, then

$$V_{RS(MAX)} = 20\ k \times 12\ mA = 240\ V$$

Therefore, the $V_{RS(pk–pk)}$ voltage can be as high as 480 V.

The CS1124 will *typically* run at a frequency up to 1.8 MHz if the input signal does not activate the positive or negative input clamps. Frequency performance will be lower when the positive or negative clamps are active. *Typical* performance will be up to a frequency of 680 kHz with the clamps active.

CIRCUIT DESCRIPTION

Figure 3 shows the part operating near the minimum input thresholds. As the sin wave input threshold is increased, the low side clamps become active (Figure 4). Increasing the amplitude further (Figure 5), the high–side clamp becomes active. These internal clamps allow for voltages up to –250 V and 250 V on the sensor side of the setup (with R1 = R2 = 22 k) (reference the diagram page 1).

Figure 6 shows the effect using the diagnostic (DIAG) function has on the circuit. The input threshold (negative) is switched from a threshold of –160 mV to +160 mV when DIAG goes from a low to a high. There is no hysteresis when DIAG is high.

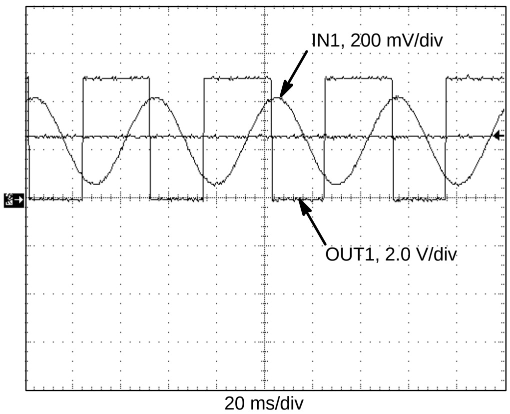


Figure 3. Minimum Threshold Operation

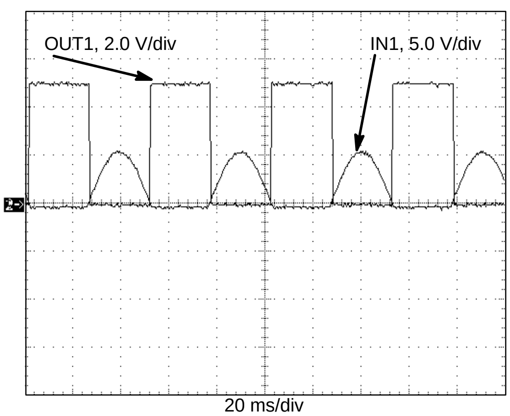


Figure 4. Low–Side Clamp

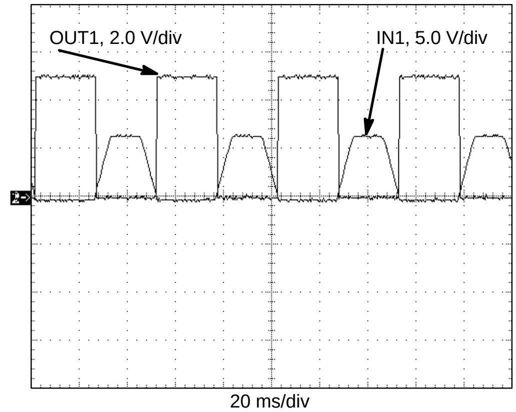


Figure 5. Low– and High–Side Clamps

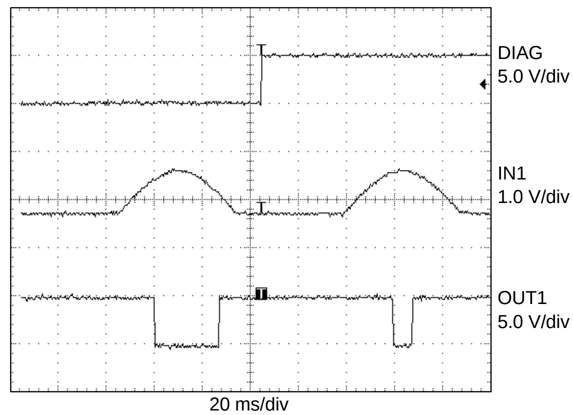


Figure 6. Diagnostic Operation

APPLICATION INFORMATION

Referring to Figure 2, the following will be a design example given these system requirements:

$$R_{RS} = 1.5\ k\Omega\ (> 12\ k\Omega \text{ is considered open})$$

$$V_{RS(MAX)} = 120\ V_{pk}$$

$$V_{RS(MIN)} = 250\ mV_{pk}$$

$$F_{VRS} = 10\ kHz\ @\ V_{RS(MIN)} = 40\ V_{pk-pk}$$

1. Determine tradeoff between R1 value and power rating. (use 1/2 watt package)

$$P_D = \frac{\left(\frac{120}{\sqrt{2}}\right)^2}{R1} < 1/2\ W$$

Set R1 = 15 k. (The clamp current will then be 120/15 k = 8.0 mA, which is less than the 12 mA limit.)

2. Determine R_{Adj}

Set R_{Adj} as close to R1 + R_{RS} as possible.

Therefore, R_{Adj} = 17 k.

3. Determine $V_{RS(+TRP)}$ using equation (7).

$$V_{RS(+TRP)} = 11\mu A \times 17k - 11\mu A(15k + 1.5k) + 160\,mV$$

$$V_{RS(+TRP)} = 166\ mV \text{ typical}$$
(easily meets 250 mV minimum)

4. Calculate worst case $V_{RS(+TRP)}$

Examination of equation (7) and the spec reveals the worst case trip voltage will occur when:

V_{HYS} = 180 mV
IN_{Adj} = 16 µA
INP1 = 15 µA
R1 = 14.25 k (5% low)
R_{Adj} = 17.85 k (5% High)

$$\begin{aligned} V_{RS(+)MAX} &= 16\ \mu A(17.85\ k) \\ &\quad - 15\mu A(14.25\ k + 1.5\ k) + 180\ mV \\ &= 229\ mV \end{aligned}$$

which is still less than the 250 mV minimum amplitude of the input.

5. Calculate C1 for low pass filtering

Since the sensor guarantees 40 V_{pk-pk} @ 10 kHz, a low pass filter using R1 and C1 can be used to eliminate high frequency noise without affecting system performance.

$$\text{Gain Reduction} = \frac{0.29\ V}{20\ V} = 0.0145 = -36.7\ dB$$

Therefore, a cut–off frequency, f_C, of 145 Hz could be used.

$$C1 \le \frac{1}{2\pi f_C R1} \le 0.07\ \mu F$$

Set C1 = 0.047 µF.

6. Calculate the minimum R_{RS} that will be indicated as an open circuit. (DIAG = 5.0 V)

Rearranging equation (7) gives

$$R_{RS} = \frac{\left[\begin{array}{l} V_{HYS} + [INP1 \times K_I \times R_{Adj}] \\ - V_{RS(+TRP)} \end{array}\right]}{INP1} - R1$$

But, V_{RS} = 0 during this test, so it drops out.

Using the following as worst case Low and High:

	Worst Case Low (R_{RS})	Worst Case High (R_{RS})
IN_{Adj}	23.6 µA = 15 µA × 1.57	10.7 µA = 7.0 µA × 1.53
R_{Adj}	16.15 k	17.85 k
V_{HYS}	135 mV	185 mV
INP1	16 µA	6.0 µA
R1	15.75 k	14.25 k
K_I	1.57	1.53

$$\begin{aligned} R_{RS} &= \frac{135\ mV + 23.6\ \mu A \times 16.15\ k}{16\ \mu A} - 15.75\ k \\ &= 16.5\ k \end{aligned}$$

Therefore,

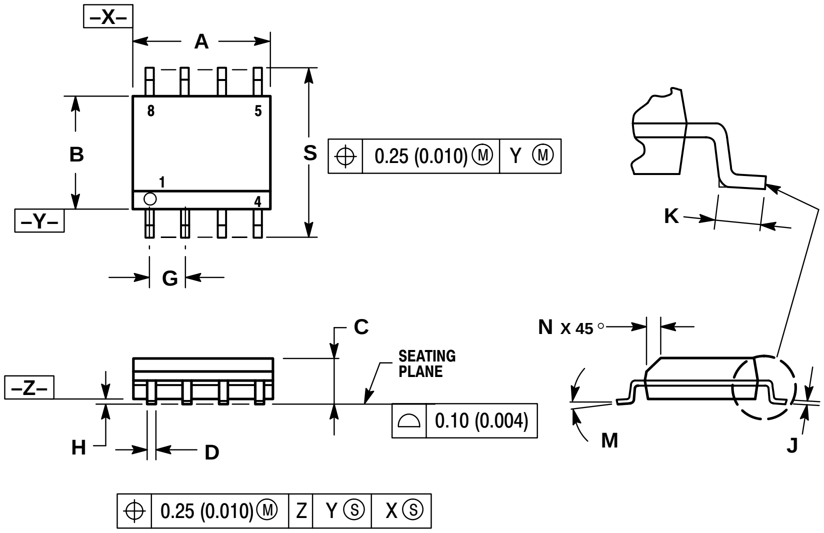
$$R_{RS(MIN)} = 16.5\ k \text{ (meets 12 k system spec)}$$

and,

$$\begin{aligned} R_{RS(MAX)} &= \frac{185\ mV + 10.7\ \mu A \times 17.85\ k}{6.0\mu A} - 14.25\ k \\ &= 48.4\ k \end{aligned}$$

PACKAGE DIMENSIONS

SO–8
D SUFFIX
CASE 751–07
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

PACKAGE THERMAL DATA

Parameter		SO–8	Unit
$R_{\Theta JC}$	Typical	45	°C/W
$R_{\Theta JA}$	Typical	165	°C/W

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

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JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

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