

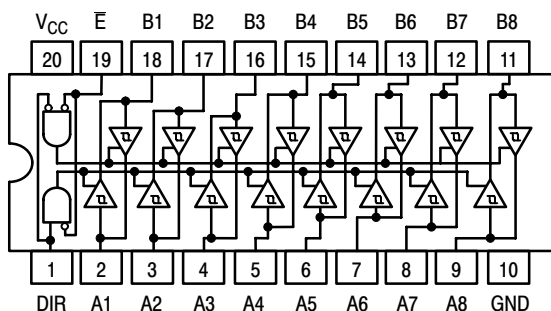
SN74LS245

Octal Bus Transceiver

The SN74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DIR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input (\bar{E}) can be used to isolate the buses.

- Hysteresis Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)



TRUTH TABLE

INPUTS		OUTPUT
\bar{E}	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–3.0	mA
				–15	mA
I_{OL}	Output Current – Low			24	mA

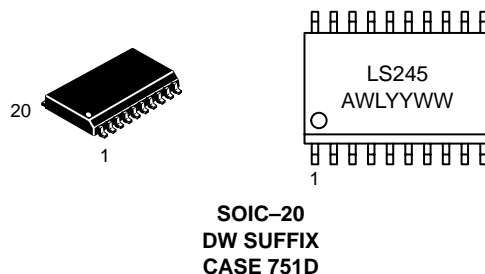
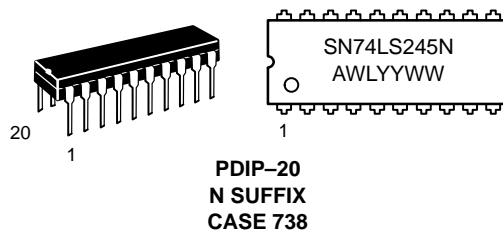


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LOW POWER SCHOTTKY

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
SN74LS245N	PDIP-20	1440 Units/Box
SN74LS245DW	SOIC-20	2500/Tape & Reel

SN74LS245

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{T+}-V_{T-}$	Hysteresis	0.2	0.4		V	$V_{CC} = \text{MIN}$
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.4	3.4		V	$V_{CC} = \text{MIN}$, $I_{OH} = -3.0 \text{ mA}$
		2.0			V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$, $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table
			0.35	0.5	V	$I_{OL} = 24 \text{ mA}$
I_{OZH}	Output Off Current HIGH			20	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 2.7 \text{ V}$
I_{OZL}	Output Off Current LOW			-200	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.4 \text{ V}$
I_{IH}	Input HIGH Current	A or B, DR or \bar{E}		20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
		DR or \bar{E}		0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
		A or B		0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 5.5 \text{ V}$
I_{IL}	Input LOW Current			-0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Output Short Circuit Current (Note 1.)	-40		-225	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current Total, Output HIGH			70	mA	$V_{CC} = \text{MAX}$
	Total, Output LOW			90		
	Total at HIGH Z			95		

1. Not more than one output should be shorted at a time, nor for more than 1 second.

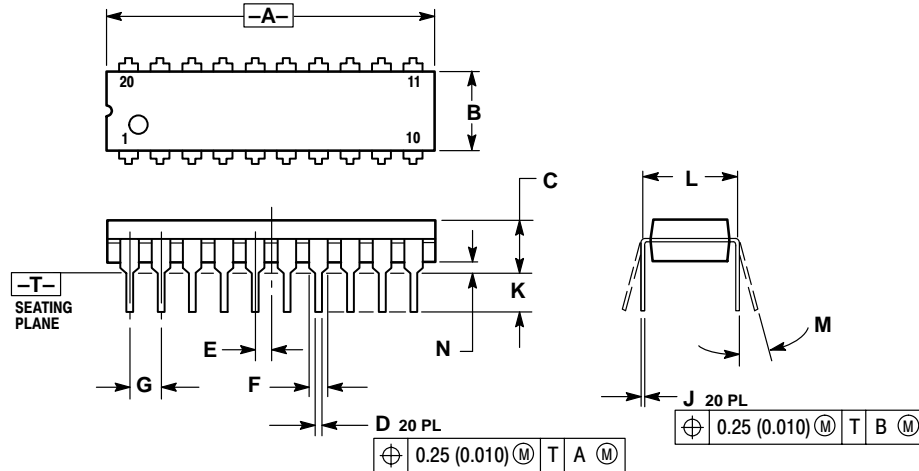
AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$, $T_{RISE}/T_{FALL} \leq 6.0 \text{ ns}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		8.0 8.0	12 12	ns	$C_L = 45 \text{ pF}$, $R_L = 667 \Omega$
t_{PZH}	Output Enable Time to HIGH Level		25	40	ns	
t_{PZL}	Output Enable Time to LOW Level		27	40	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25	ns	$C_L = 5.0 \text{ pF}$, $R_L = 667 \Omega$
t_{PHZ}	Output Disable Time from HIGH Level		15	25	ns	

SN74LS245

PACKAGE DIMENSIONS

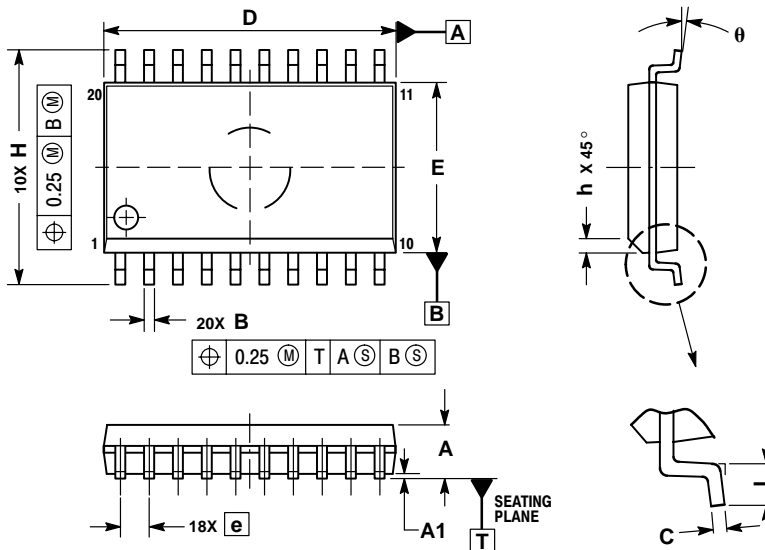
N SUFFIX PLASTIC PACKAGE CASE 738-03 ISSUE E



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

D SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

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