

# MC100E193

## 5V ECL Error Detection/ Correction Circuit

The MC100E193 is an error detection and correction (EDAC) circuit. Modified Hamming parity codes are generated on an 8-bit word according to the pattern shown in the logic symbol. The P5 output gives the parity of the whole word. The word parity is also provided at the PGEN pin, after Odd/Even parity control and gating with the BPAR input. This output also feeds to a 1-bit shiftable register, for use as part of a scan ring.

Used in conjunction with 12-bit parity generators such as the E160, a SECCDED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

The 100 Series contains temperature compensation.

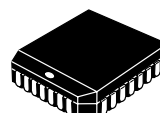
- Hamming Code Generation
- 8-Bit Word, Expandable
- Provides Parity of Whole Word
- Scannable Parity Register
- PECL Mode Operating Range:  $V_{CC} = 4.2\text{ V}$  to  $5.7\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -4.2\text{ V}$  to  $-5.7\text{ V}$
- Internal Input Pulldown Resistors
- ESD Protection:  $> 1\text{ KV HBM}$ ,  $> 75\text{ V MM}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 368 devices



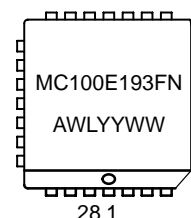
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### MARKING DIAGRAM



**PLCC-28  
FN SUFFIX  
CASE 776**

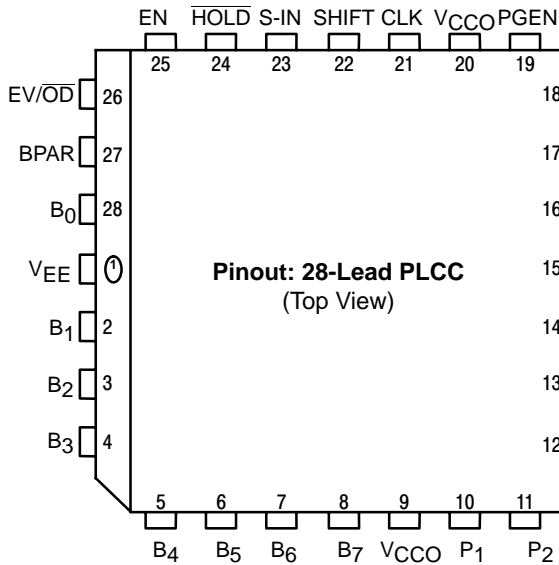


A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC100E193FN	PLCC-28	37 Units/Rail
MC100E193FNR2	PLCC-28	500 Units/Reel

# MC100E193



\* All VCC and VCCO pins are tied together on the die.

Warning: All VCC, VCCO, and VEE pins must be externally connected to Power Supply to guarantee proper operation.

## PIN DESCRIPTION

PIN	FUNCTION
B0–B6	ECL Bit Inputs
P1–P5	ECL Parity Outputs
PARERR, $\overline{\text{PARERR}}$	ECL Parity Error Outputs
PGEN	ECL Word Parity Generator Output
CLK	ECL Clock Input
SHIFT	ECL Shift Input (Active–High)
S–IN	ECL Serial Data Input
$\overline{\text{HOLD}}$	ECL Hold (Active–Low)
EN	ECL Enable (Active–Low)
EV/ $\overline{\text{DD}}$	ECL Even/Odd Contact
BPAR	ECL Bit Parity Gate Input
VCC, VCCO	Positive Supply
VEE	Negative Supply
NC	No Connect

Figure 1. Pinout Assignment

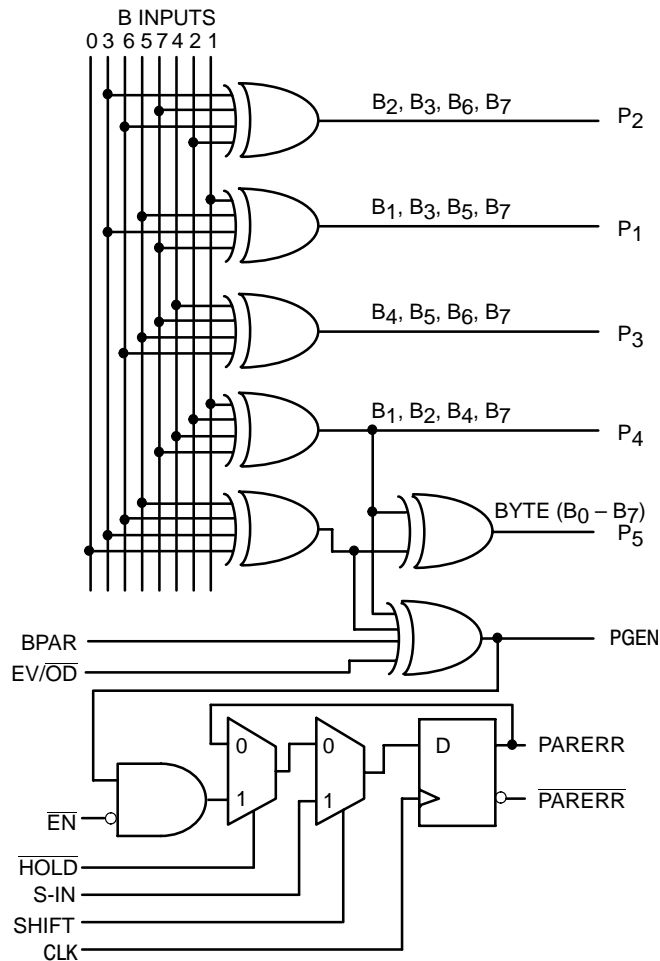


Figure 2. Logic Diagram

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## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		−8	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 −6	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			0 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			−65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	28 PLCC	22 to 26	°C/W
V <sub>EE</sub>	PECL Operating Range NECL Operating Range			4.2 to 5.7 −5.7 to −4.2	V V
T <sub>sol</sub>	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## 100E SERIES PECL DC CHARACTERISTICS V<sub>CCx</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 2)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		112	134		112	134		129	155	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 3)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V <sub>OL</sub>	Output LOW Voltage (Note 3)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V <sub>IH</sub>	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V <sub>IL</sub>	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / −0.8 V.

3. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> − 2.0 V.

## 100E SERIES NECL DC CHARACTERISTICS V<sub>CCx</sub> = 0.0 V; V<sub>EE</sub> = −5.0 V (Note 4)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		112	134		112	134		129	155	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 5)	−1025	−950	−880	−1025	−950	−880	−1025	−950	−880	mV
V <sub>OL</sub>	Output LOW Voltage (Note 5)	−1810	−1705	−1620	−1810	−1745	−1620	−1810	−1740	−1620	mV
V <sub>IH</sub>	Input HIGH Voltage	−1165	−950	−880	−1165	−880	−880	−1165	−880	−880	mV
V <sub>IL</sub>	Input LOW Voltage	−1810	−1700	−1475	−1810	−1475	−1475	−1810	−1475	−1475	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / −0.8 V.

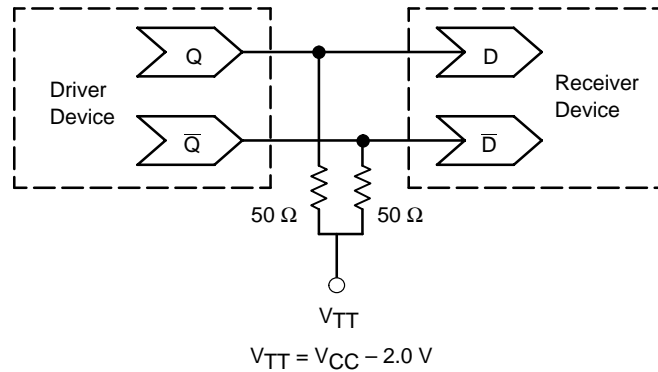
5. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> − 2.0 V.

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## AC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$ ; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ (Note 6)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output B to P1, P2, P3, P4 B to P5 EV/ $\overline{OD}$ , BPAR to PGEN B to PGEN CLK to PARERR	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	ps
$t_s$	Setup Time SHIFT S-IN $\overline{HOLD}$ $\overline{EN}$ EV/ $\overline{OD}$ BPAR B	400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100		400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100		400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100		ps
$t_h$	Hold Time SHIFT S-IN $\overline{HOLD}$ $\overline{EN}$ EV/ $\overline{OD}$ BPAR B	200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100		200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100		200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r$ $t_f$	Rise/Fall Times (20 - 80%)	300	700	1100	300	700	1100	300	700	1100	ps

6. 100 Series:  $V_{EE}$  can vary  $+0.46\text{ V}$  /  $-0.8\text{ V}$ .



**Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

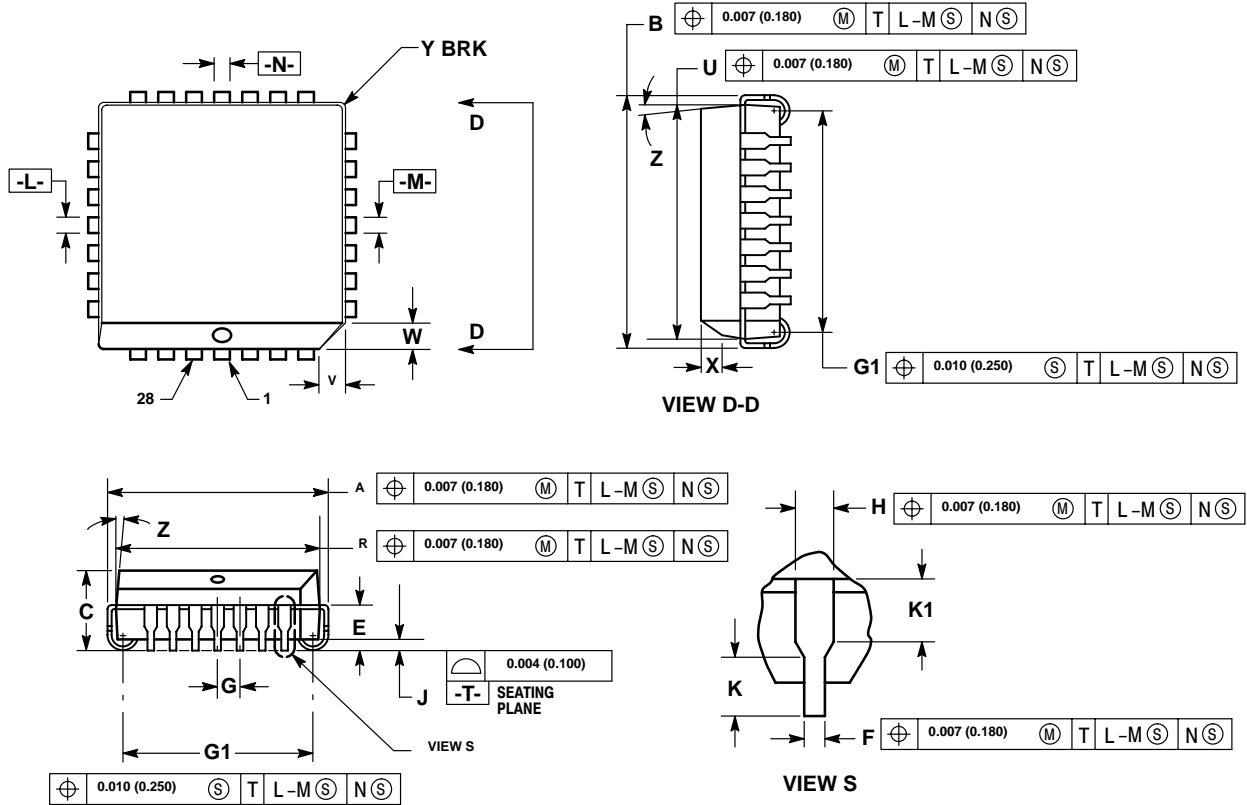
**Resource Reference of Application Notes**

- AN1404** – ECLinPS Circuit Performance at Non–Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire–OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC100E193

## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

## **Notes**

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