

MC100LVEL38

3.3V ECL $\div 2$, $\div 4/6$ Clock Generation Chip

The MC100LVEL38 is a low skew $\div 2$, $\div 4/6$ clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal.

The common enable (\overline{EN}) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the $\div 2$ and the $\div 4/6$ outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the $\div 2$ and the $\div 4/6$ outputs of a single device.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

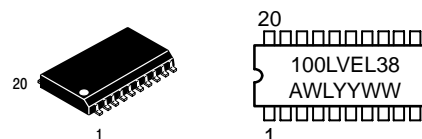
- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.0 V to -3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 388 devices



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MARKING DIAGRAM



SO-20
DW SUFFIX
CASE 751D

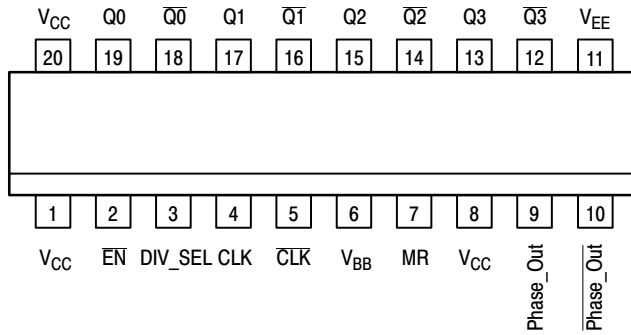
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL38DW	SOIC-20	38 Units/Rail
MC100LVEL38DWR2	SOIC-20	1000 Units/Reel

MC100LVEL38

Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLE

CLK	\overline{EN}	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

Z = Low-to-High Transition

ZZ = High-to-Low Transition

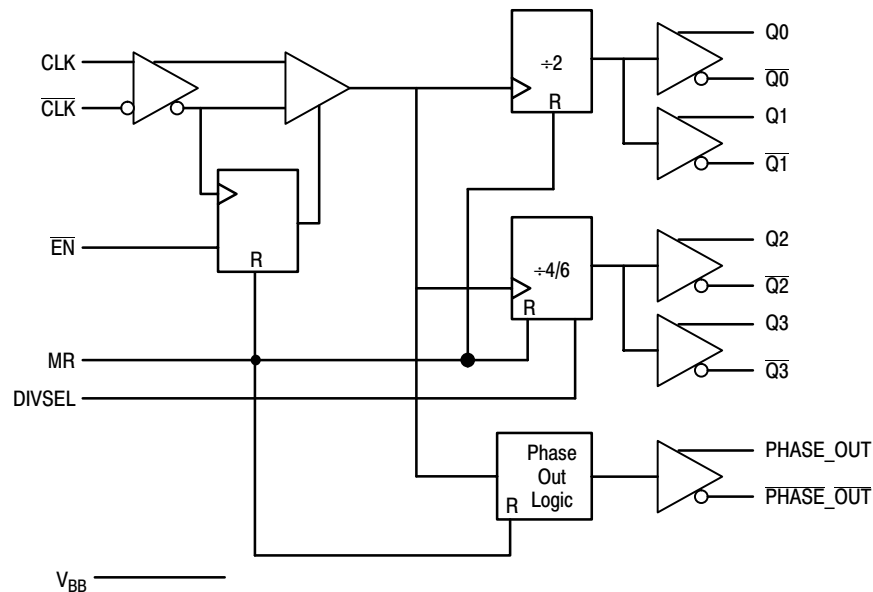
X = Don't Care

DIVSEL	Q_2, Q_3 OUTPUTS
L	Divide by 4
H	Divide by 6

PIN DESCRIPTION

PIN	FUNCTION
CLK, \overline{CLK}	ECL Diff Clock Inputs
$Q_0, Q_1, \overline{Q_0}, \overline{Q_1}$	ECL Diff $\div 2$ Outputs
$Q_2, Q_3, \overline{Q_2}, \overline{Q_3}$	ECL Diff $\div 4/6$ Outputs
\overline{EN}	ECL Sync Enable Input
MR	ECL Master Reset Input
DIVSEL	ECL Frequency Select Input
Phase_Out, $\overline{Phase_Out}$	ECL Phase Sync Diff. Signal Output
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

LOGIC DIAGRAM



MC100LEVEL38

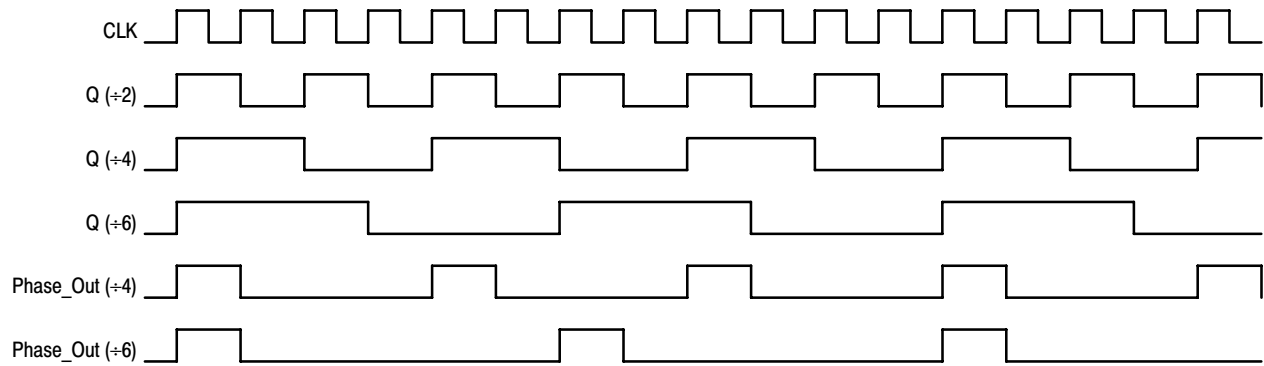


Figure 1. Timing Diagrams

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8 to 0	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 -6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

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LVPECL DC CHARACTERISTICS $V_{CC}=3.3\text{ V}$; $V_{EE}=0.0\text{ V}$ (Note 2)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)	1.65		2.75	1.65		2.75	1.65		2.75	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2\text{ volts}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\text{ Min}}$ and 1.0 V .

LVNECL DC CHARACTERISTICS $V_{CC}=0.0\text{ V}$; $V_{EE}=-3.3\text{ V}$ (Note 5)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 6)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 6)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1 165		-880	-1 165		-880	-1 165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)	-1.65		-0.55	-1.65		-0.55	-1.65		-0.55	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC}-2\text{ volts}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\text{ Min}}$ and 1.0 V .

MC100LEVEL38

AC CHARACTERISTICS $V_{CC}= 3.3\text{ V}$; $V_{EE}= 0.0\text{ V}$ or $V_{CC}= 0.0\text{ V}$; $V_{EE}= -3.3\text{ V}$ (Note 8)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{max}	Maximum Toggle Frequency (Divide by 2)	1.0	1.2		1.0	1.2		1.0	1.2		GHz
t _{PLH} t _{PHL}	Propagation Delay to Output CLK to Q (Diff) CLK to Q (S.E.) CLK to Phase_Out (Diff) CLK to Phase_Out (S.E.) MR to Q	760 710 800 750 510		960 1010 1000 1050 810	800 750 840 790 540		1000 1050 1040 1090 840	850 800 890 840 570		1050 1100 1090 1140 870	ps
t _{SKEW}	Within-Device Skew (Note 9) Q ₀ - Q ₃ All			50 75			50 75			50 75	ps
	Part-to-Part Q ₀ - Q ₃ (Diff) All			200 240			200 240			200 240	ps
t _S	Setup Time $\overline{\text{EN}}$ to $\overline{\text{CLK}}$ DIVSEL to CLK	150			150			150			ps
t _H	Hold Time $\overline{\text{CLK}}$ to $\overline{\text{EN}}$ CLK to Div_Sel	150 200			150 200			150 200			ps
V _{PP}	Input Swing (Note 10) CLK	250		1000	250		1000	250		1000	mV
t _{RR}	Reset Recovery Time			100			100			100	ps
t _{PW}	Minimum Pulse Width CLK MR	800 700			800 700			800 700			ps
t _r , t _f	Output Rise/Fall Times Q (20% - 80%)	280		550	280		550	280		550	ps

8. V_{EE} can vary $\pm 0.3\text{ V}$.

9. Skew is measured between outputs under identical transitions.

10. $V_{PP}(\text{min})$ is minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100 mV.

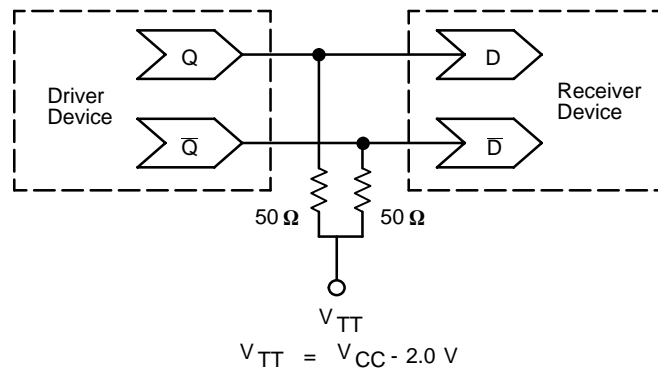


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 - Termination of ECL Logic Devices.)

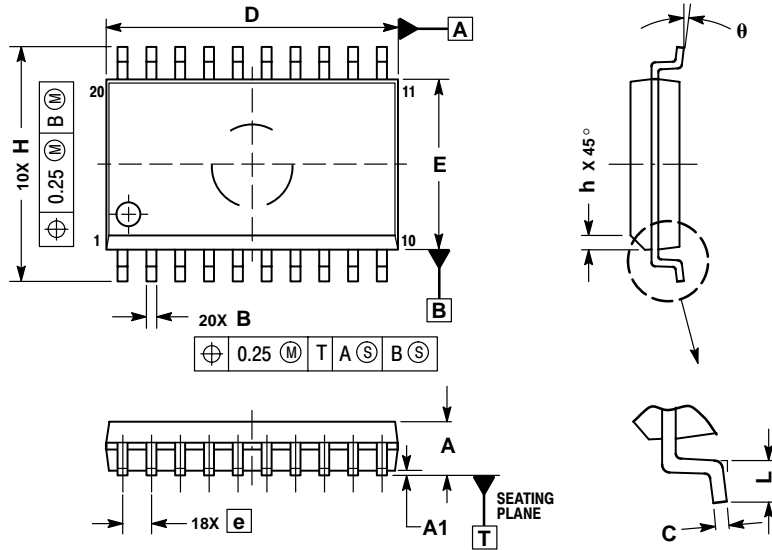
Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices

MC100LVEL38

PACKAGE DIMENSIONS


SOIC-20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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