

MC14528B

Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X .

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

| Symbol | Parameter | Value | Unit |
|----------------------|---------------------------------------------------|------------------------|------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in} , V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in} , I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 3.) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |
| T_L | Lead Temperature (8-Second Soldering) | 260 | °C |

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

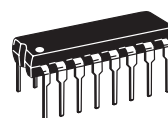
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



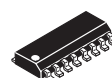
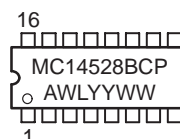
ON Semiconductor

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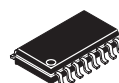
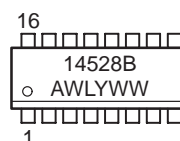
MARKING DIAGRAMS



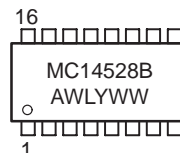
PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

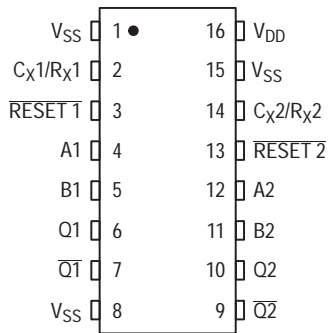
ORDERING INFORMATION

| Device | Package | Shipping |
|-------------|-----------|------------------|
| MC14528BCP | PDIP-16 | 2000/Box |
| MC14528BD | SOIC-16 | 48/Rail |
| MC14528BDR2 | SOIC-16 | 2500/Tape & Reel |
| MC14528BF | SOEIAJ-16 | See Note 1. |
| MC14528BFEL | SOEIAJ-16 | See Note 1. |

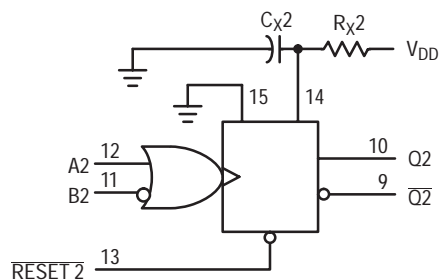
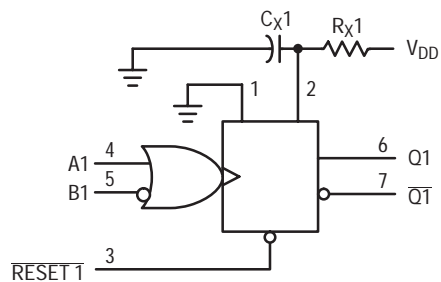
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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PIN ASSIGNMENT

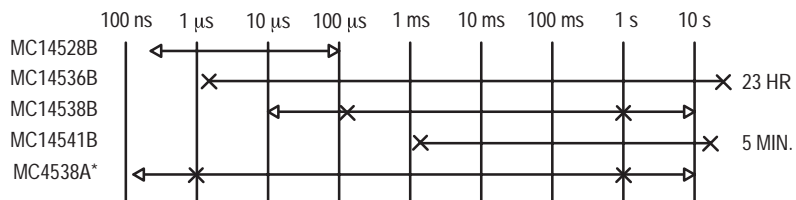


BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 1, PIN 8, PIN 15
R_X AND C_X ARE EXTERNAL COMPONENTS

ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2-6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ←-----→
RECOMMENDED PULSE WIDTH RANGE X-----X

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-----------|-------|--------|-------|------------------|
| | | | Min | Max | Min | Typ (4.) | Max | Min | Max | |
| Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD} | V _{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | V _{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | V _{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| | V _{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) | Source I _{OH} | 5.0 | - 1.2 | — | - 1.0 | - 1.7 | — | - 0.7 | — | mA _{dc} |
| | | 5.0 | - 0.64 | — | - 0.51 | - 0.88 | — | - 0.36 | — | |
| | | 10 | - 1.6 | — | - 1.3 | - 2.25 | — | - 0.9 | — | |
| | | 15 | - 4.2 | — | - 3.4 | - 8.8 | — | - 2.4 | — | |
| | Sink I _{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mA _{dc} |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Input Current | I _{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | μA _{dc} |
| Input Capacitance (V _{in} = 0) | C _{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μA _{dc} |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |
| Total Supply Current at an external load Capacitance (C _L) and at external timing capacitance (C _X), use the formula — (5.) | I _T | — | $I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2 \times 10^{-8} R_X C_X (V_{DD}^{-2})^2] \times 10^{-3}$ where: I _T in μA (per circuit), C _L and C _X in pF, R _X in megohms, V _{DD} in Vdc, f in kHz is input frequency. | | | | | | | μA _{dc} |

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

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SWITCHING CHARACTERISTICS ^(8.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | C_X pF | R_X k Ω | V_{DD} Vdc | Min | Typ ^(9.) | Max | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-------------|---------------------|-----------------|---------------------------|---------------------|-------------------|---------------|
| Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | $t_{TLH},$ t_{THL} | — | — | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 15 | 5.0 | 5.0 10 15 | — — — | 325 120 90 | 650 240 180 | ns |
| Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 1000 | 10 | 5.0 10 15 | — — — | 705 290 210 | — — — | ns |
| Input Pulse Width — A or B | t_{WH} | 15 | 5.0 | 5.0 10 15 | 150 75 55 | 70 30 30 | — — — | ns |
| | t_{WL} | 1000 | 10 | 5.0 10 15 | — — — | 70 30 30 | — — — | ns |
| Output Pulse Width — Q or \bar{Q} (For $C_X < 0.01 \mu\text{F}$ use graph for appropriate V_{DD} level.) | t_W | 15 | 5.0 | 5.0 10 15 | — — — | 550 350 300 | — — — | ns |
| Output Pulse Width — Q or \bar{Q} (For $C_X > 0.01 \mu\text{F}$ use formula: $t_W = 0.2 R_X C_X \ln [V_{DD} - V_{SS}]$ ^(6.)) | t_W | 10,000 | 10 | 5.0 10 15 | 15 10 15 | 30 50 55 | 45 90 95 | μs |
| Pulse Width Match between Circuits in the same package | $t_1 - t_2$ | 10,000 | 10 | 5.0 10 15 | — — — | 6.0 8.0 8.0 | 25 35 35 | % |
| Reset Propagation Delay — Reset to Q or \bar{Q} | $t_{PLH},$ t_{PHL} | 15 | 5.0 | 5.0 10 15 | — — — | 325 90 60 | 600 225 170 | ns |
| | | 1000 | 10 | 5.0 10 15 | — — — | 1000 300 250 | — — — | ns |
| Retrigger Time | t_{rr} | 15 | 5.0 | 5.0 10 15 | 0 0 0 | — — — | — — — | ns |
| | | 1000 | 10 | 5.0 10 15 | 0 0 0 | — — — | — — — | ns |
| External Timing Resistance | R_X | — | — | — | 5.0 | — | 1000 | k Ω |
| External Timing Capacitance | C_X | — | — | — | No Limits ^(7.) | | | μF |

6. R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.















7. If $C_X > 15 \mu\text{F}$, Use Discharge Protection Diode D_X , per Fig. 9.

8. The formulas given are for the typical characteristics only at 25°C .

9. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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FUNCTION TABLE

| Inputs | | | Outputs | |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reset | A | B | Q | \bar{Q} |
| H H |  L | H  |   |   |
| H H |   H | L   | Not Triggered Not Triggered | |
| H H | L, H,  L | H L, H,  | Not Triggered Not Triggered | |
| L   | X X | X X | L H Not Triggered | |

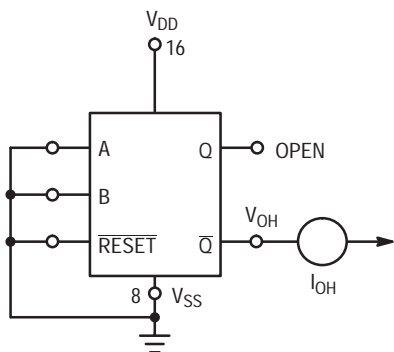


Figure 1. Output Source Current Test Circuit

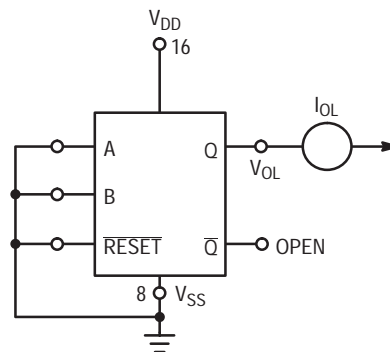


Figure 2. Output Sink Current Test Circuit

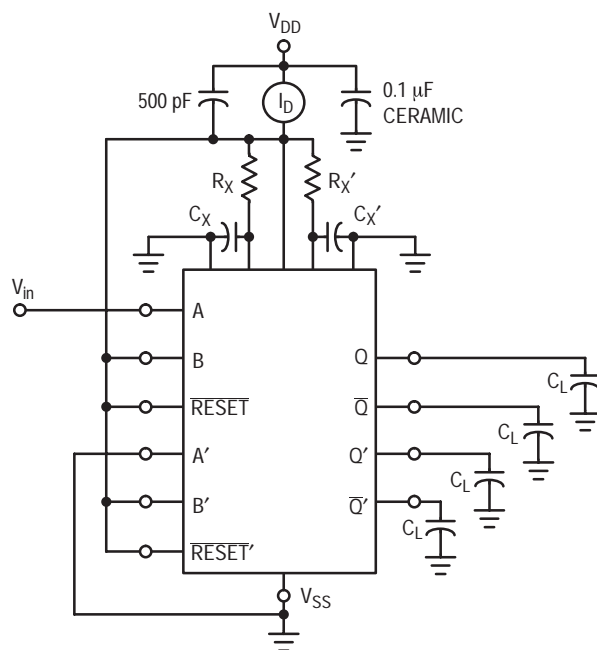
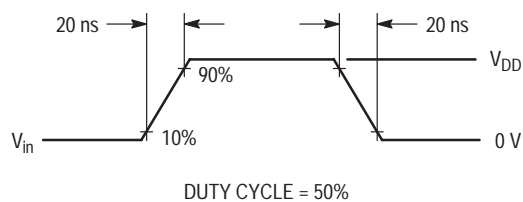
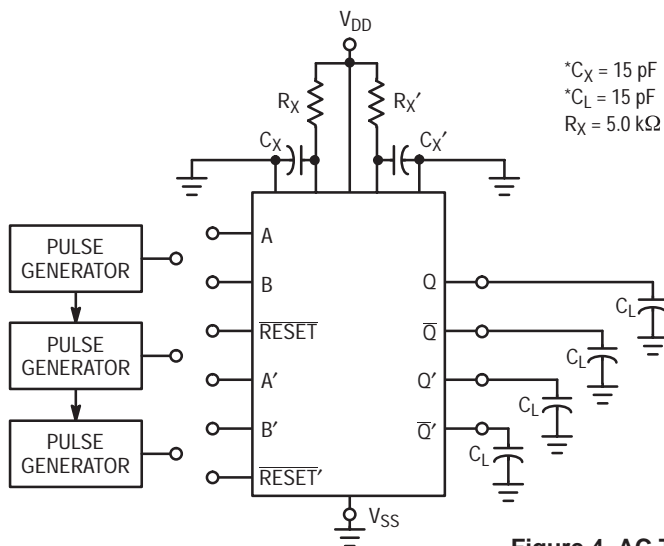


Figure 3. Power Dissipation Test Circuit and Waveforms



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INPUT CONNECTIONS

| Characteristics | Reset | A | B |
|--------------------------------------------------------|----------|----------|----------|
| t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} t_W | V_{DD} | PG1 | V_{DD} |
| t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} t_W | V_{DD} | V_{SS} | PG2 |
| $t_{PLH(R)}$, $t_{PHL(R)}$, t_W | PG3 | PG1 | PG2 |

* Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

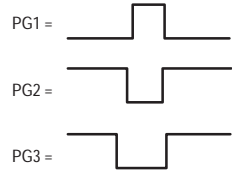


Figure 4. AC Test Circuit

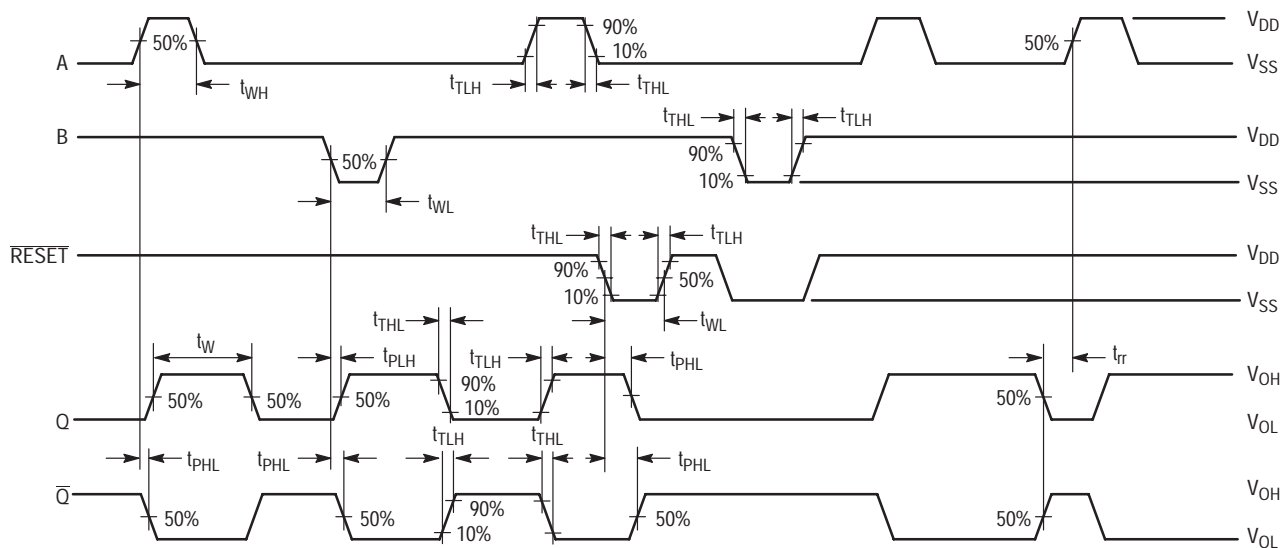


Figure 5. AC Test Waveforms

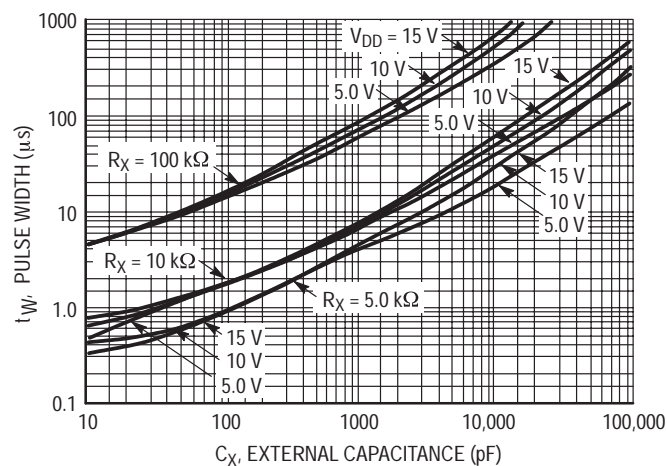


Figure 6. Pulse Width versus C_X

TYPICAL APPLICATIONS

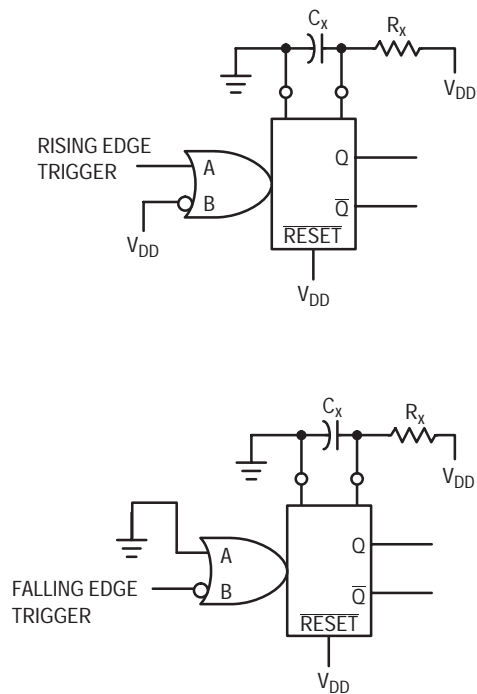


Figure 7. Retriggerable Monostables Circuitry

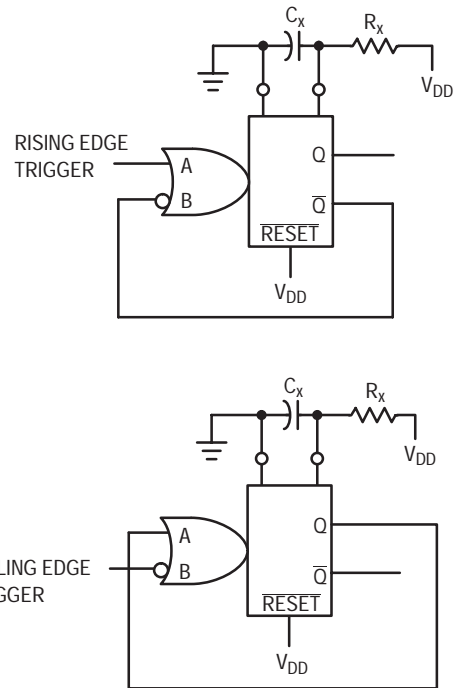


Figure 8. Non-Retriggerable Monostables Circuitry

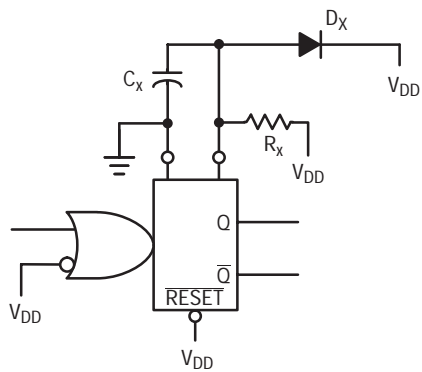


Figure 9. Use of a Diode to Limit Power Down Current Surge

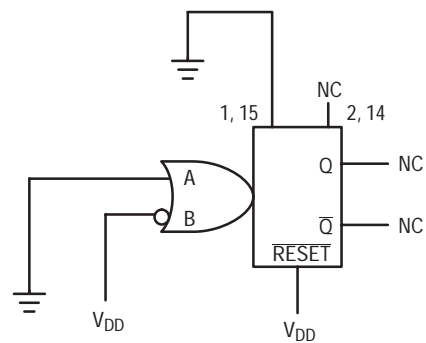
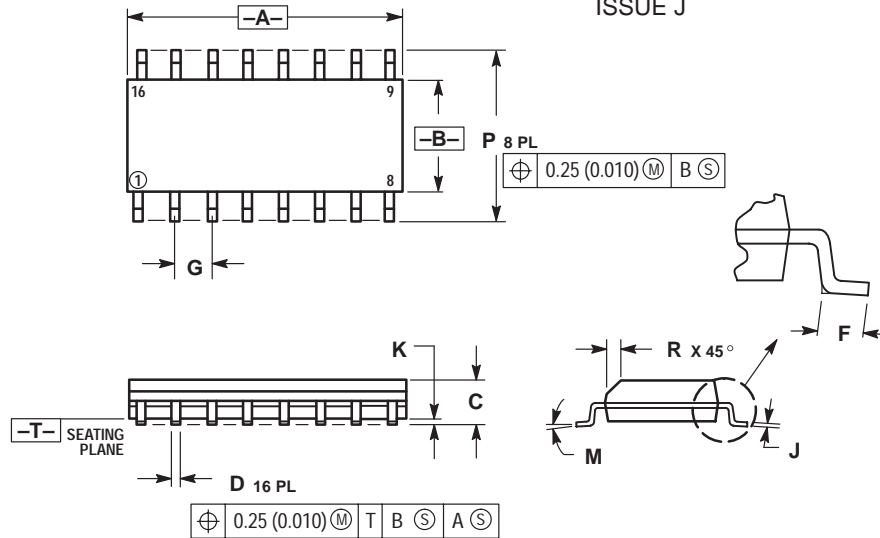


Figure 10. Connection of Unused Sections

MC14528B

PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



NOTES:

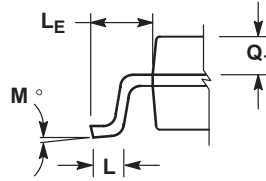
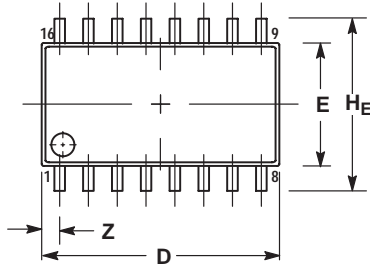
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

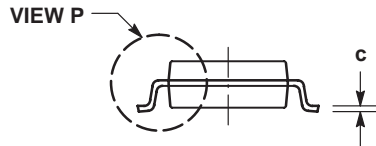
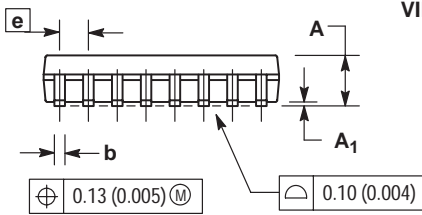
MC14528B

PACKAGE DIMENSIONS

SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



DETAIL P




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

Notes

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JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549
Phone: 81-3-5740-2745
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.