

NBSG111

2.5V/3.3V SiGe Differential 1:10 Clock/Data Driver with RSECL* Outputs

*Reduced Swing ECL

The NBSG111 is a 1-to-10 differential clock/data driver. The device is functionally equivalent to the LVEP111 device with much higher bandwidth and lower EMI capabilities.

Inputs incorporate internal 50 Ω termination resistors (input to VT pad) and accept NECL (Negative ECL), PECL (Positive ECL), LVTTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

The Q[0:9] / \overline{Q} [0:9] outputs have a differential synchronous enable (EN/ \overline{EN}) pin. The synchronous enable pin is used to avoid a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of selected clock (CLK0/ $\overline{CLK0}$ or CLK1/ $\overline{CLK1}$), therefore all associated specification limits are referenced to the negative edge of the selected clock input.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used for single-ended NECL or PECL inputs and the V_{MM} pin is used for LVCMOS inputs. For single-ended input operation, the unused differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

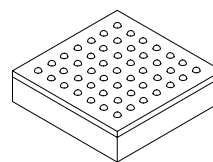
- Maximum Input Clock Frequency > 6 GHz Typical
- Maximum Input Data Rate > 6 Gb/s Typical
- 300 ps Typical Propagation Delay
- 60 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range: $V_{CC} = 2.375$ V to 3.465 V with $V_{EE} = 0$ V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP and EP Devices
- V_{BB} and V_{MM} Reference Voltage Output



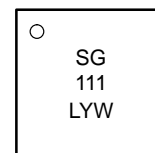
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MARKING DIAGRAM*



FCBGA-49
BA SUFFIX
CASE 489A



SG111 = Device Code
L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG111BA	8x8 mm FCBGA-49	100 Units/Tray
NBSG111BAR2	8x8 mm FCBGA-49	500/Tape & Reel

Board	Description
NBSG111BAEVB	NBSG111BA Evaluation Board

NBSG111

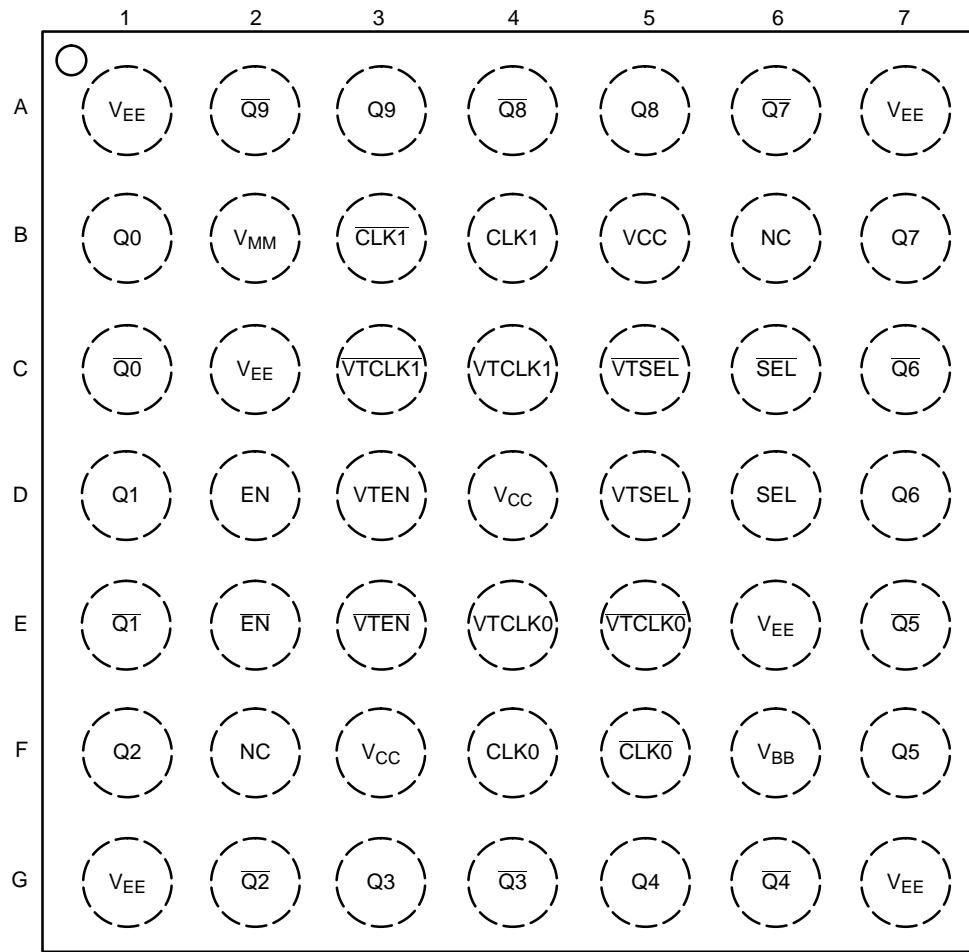


Figure 1. BGA-49 Pinout (Top View)

Table 1. Pin Description

Pin	Name	I/O	Description
A1,A7,G1,G7,C2,E6	V _{EE}	-	Negative Supply Voltage. All V _{EE} Pins Must be Externally Connected to Power Supply to Guarantee Proper Operation.
F3,D4,B5	V _{CC}	-	Positive Supply Voltage. All V _{CC} Pins Must be Externally Connected to Power Supply to Guarantee Proper Operation.
B2	V _{MM}	-	LVC MOS Reference Voltage Output (V _{CC} - V _{EE}) / 2.
F6	V _{BB}	-	ECL Reference Voltage Output
E4	VTCLK0	-	Internal 50 Ω Termination Pin for CLK0. See Table 4. (Note 1)
F4	CLK0	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input CLK0. Internal 75 kΩ to V _{EE} .
E5	VTCLK0	-	Internal 50 Ω Termination Pin for CLK0. See Table 4. (Note 1)
F5	CLK0	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input CLK0. Internal 75 kΩ to V _{EE} and 36.5 kΩ to V _{CC} .
C4	VTCLK1	-	Internal 50 Ω Termination Pin 1. See Table 4. (Note 1)
B4	CLK1	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input CLK1. Internal 75 kΩ to V _{EE} .
C3	VTCLK1	-	Internal 50 Ω Termination Pin for CLK1. See Table 4. (Note 1)
B3	CLK1	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input CLK1. Internal 75 kΩ to V _{EE} and 36.5 kΩ to V _{CC} .
B1,D1,F1,G3,G5,F7,D7,B7,A5,A3	Q[0:9]	RSECL Output	Noninverted Differential Outputs [0:9]. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 1.5 V
C1,E1,G2,G4,G6,E7,C7,A6,A4,A2	Q[0:9]	RSECL Output	Inverted Differential Outputs [0:9]. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 1.5 V
D5	VTSEL	-	Internal 50 Ω Termination Pin for SEL. See Table 4. (Note 1)
D6	SEL	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Select Logic Input. Internal 75 kΩ to V _{EE} .
C5	VTSEL	-	Internal 50 Ω Termination Pin for SEL. See Table 4. (Note 1)
C6	SEL	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Select Logic Input. Internal 75 kΩ to V _{EE} and 36.5 kΩ to V _{CC} .
D3	VTEN	-	Internal 50 Ω Termination Pin for EN. See Table 4. (Note 1)
D2	EN	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Output Enable Pin. Internal 75 kΩ to V _{EE} .
E3	VTEN	-	Internal 50 Ω termination Pin for EN. See Table 4. (Note 1)
E2	EN	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Output Enable Pin. Internal 75 kΩ to V _{EE} and 36.5 kΩ to V _{CC} .
F2,B6	NC	-	No Connect. The NC Pins are Electrically Connected to the Die and "MUST BE" Left Open.

1. In the differential configuration when the input termination pins (VTCLK, VTCLK) are connected to a common termination voltage and if no signal is applied, then the device will be susceptible to self-oscillation.

Table 2. FUNCTION TABLE

SEL	EN	Active Input
L	L	Disabled Outputs
L	H	CLK0, $\overline{\text{CLK0}}$
H	L	Disabled Outputs
H	H	CLK1, $\overline{\text{CLK1}}$

2. $\overline{\text{SEL}}$ / $\overline{\text{EN}}$ are the inverse of SEL/EN unless specified otherwise.

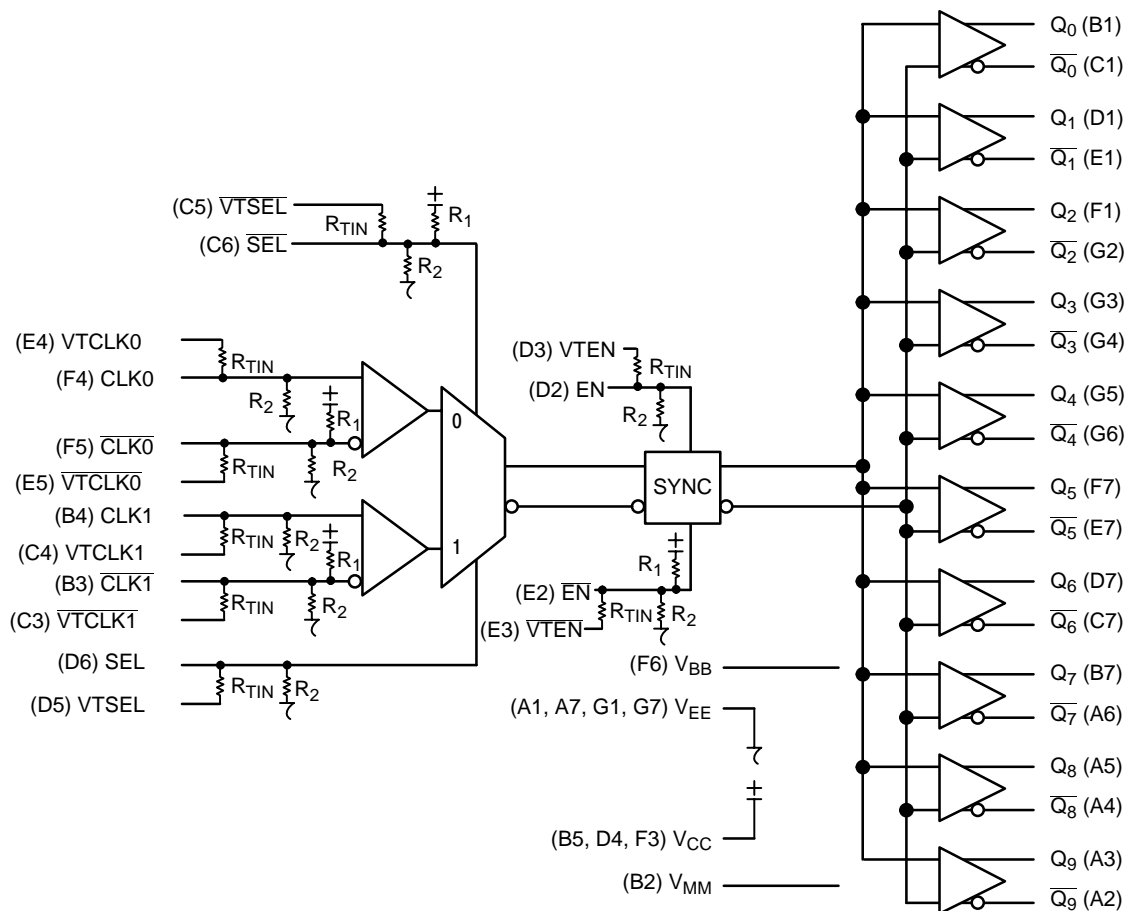


Figure 2. Logic Diagram

Table 3. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK0, VTCLK1, VTEN, VTSEL and VTCLK0, VTCLK1, VTEN, VTSEL to V _{CC}
LVDS	Connect VTCLK0, VTCLK1, VTEN, VTSEL and VTCLK0, VTCLK1, VTEN, VTSEL Together
AC-COUPLED	Bias VTCLK0, VTCLK1, VTEN, VTSEL and VTCLK0, VTCLK1, VTEN, VTSEL Inputs within Common Mode Range (V _{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	See Text on Page 1. Unused Differential Input Switching Voltage Reference Range is from V _{EE} + 1125 mV to V _{CC} - 75 mV

Table 4. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor, R2 (CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$, SEL, $\overline{\text{SEL}}$, EN, $\overline{\text{EN}}$)	75 k Ω
Internal Input Pullup Resistor, R1 ($\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$, $\overline{\text{SEL}}$, $\overline{\text{EN}}$)	36.5 k Ω
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 1 kV
Moisture Sensitivity (Note 3)	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	479
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Positive Power Supply	V _{EE} = 0 V		3.6	V
V _I	Positive Input Negative Input	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	3.6 -3.6	V V
V _{EE}	Negative Power Supply	V _{CC} = 0 V		-3.6	V
V _{INPP}	Differential Input Voltage CLK - $\overline{\text{CLK}}$	V _{CC} - V _{EE} ≥ 2.8 V V _{CC} - V _{EE} < 2.8 V		2.8 V _{CC} - V _{EE}	V V
I _{OUT}	Output Current	Continuous Surge		25 50	mA mA
I _{IN}	Input Current Through R _T (50 Ω Resistor)	Static Surge		45 80	mA mA
I _{BB}	V _{BB} Sink/Source			1	mA
I _{MM}	V _{MM} Sink/Source			1	mA
T _A	Operating Temperature Range			-40 to +70	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 5)	0 LFPM 500 LFPM	49 FCBGA 49 FCBGA	67 57	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 5)	49 FCBGA	2 to 4	°C/W
T _{sol}	Wave Solder	< 15 sec.		225	°C

4. Maximum Ratings are those values beyond which device damage may occur.

5. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 2.5 \text{ V}$; $V_{EE} = 0 \text{ V}$ (Note 6)

Symbol	Characteristic	-40 °C			25 °C			70 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	70	85	100	70	85	100	70	85	100	mA
V_{OH}	Output HIGH Voltage (Note 7)	1490	1540	1590	1510	1560	1610	1520	1570	1620	mV
V_{OUTPP}	Output Voltage Amplitude	300	370	450	300	370	450	300	370	450	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 9 and 10)	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 9 and 11)	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	mV
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8)	1.2		2.5	1.2		2.5	1.2		2.5	V
V_{MM}	LVC MOS Output Voltage Reference ($V_{CC} - V_{EE}$) / 2	1100	1250	1400	1100	1250	1400	1100	1250	1400	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

Table 7. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 3.3 \text{ V}$; $V_{EE} = 0 \text{ V}$ (Note 12)

Symbol	Characteristic	-40 °C			25 °C			70 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	70	85	100	70	85	100	70	85	100	mA
V_{OH}	Output HIGH Voltage (Note 7)	2290	2340	2390	2310	2360	2410	2320	2370	2420	mV
V_{OUTPP}	Output Voltage Amplitude	300	370	450	300	370	450	300	370	450	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 9 and 10)	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 9 and 11)	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	mV
V_{BB}	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8)	1.2		3.3	1.2		3.3	1.2		3.3	V
V_{MM}	LVC MOS Output Voltage Reference ($V_{CC} - V_{EE}$)/2	1500	1650	1800	1500	1650	1800	1500	1650	1800	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above tables after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -0.965 V.

7. All outputs loaded with 50 Ω to $V_{CC} - 1.5 \text{ V}$. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).

8. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

9. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM} . $V_{THR(MIN)} = V_{IHCMR} + 75 \text{ mV}$. $V_{THR(MAX)} = V_{IHCMR} - 75 \text{ mV}$.

10. V_{IH} cannot exceed V_{CC} .

11. V_{IL} always $\geq V_{EE}$.

12. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.165 V.

*Typicals used for testing purposes.

Table 8. DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT

$V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V (Note 13)

Symbol	Characteristic	-40 °C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	70	85	100	70	85	100	70	85	100	mA
V_{OH}	Output HIGH Voltage (Note 14)	-1010	-960	-910	-990	-940	-890	-980	-930	-880	mV
V_{OUTPP}	Output Voltage Amplitude	300	370	450	300	370	450	300	370	450	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 16 and 17)	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	$V_{THR} + 75$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 16 and 18)	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{THR} - 75$	mV
V_{BB}	NECL Output Voltage Reference	-1420	-1360	-1300	-1420	-1360	-1300	-1420	-1360	-1300	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 15)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
V_{MM}	LVC MOS Output Voltage Reference ($V_{CC} - V_{EE}$)/2 (Note 19)	$V_{MMT} - 150$	V_{MMT}	$V_{MMT} + 150$	$V_{MMT} - 150$	V_{MMT}	$V_{MMT} + 150$	$V_{MMT} - 150$	V_{MMT}	$V_{MMT} + 150$	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

13. Input and output parameters vary 1:1 with V_{CC} .

14. All outputs loaded with $50\ \Omega$ to $V_{CC} - 1.5\text{ V}$. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).

15. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

16. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM} . $V_{THR(MIN)} = V_{IHCMR} + 75\text{ mV}$. $V_{THR(MAX)} = V_{IHCMR} - 75\text{ mV}$.

17. V_{IH} cannot exceed V_{CC} .

18. V_{IL} always $\geq V_{EE}$.

19. V_{MM} Typical = $|V_{CC} - V_{EE}| / 2 + V_{EE} = V_{MMT}$.

*Typicals used for testing purposes.

Table 9. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.465 V ; $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40 °C			25 °C			70 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (See Figure 3) (Note 20) $f_{in} < 3\text{ GHz}$ $f_{in} = 5.5\text{ GHz}$	320 180	420 250		300 150	400 220		300 100	400 200		mV
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential Output Enable Clock Select	250 430 400	300 550 450	350 700 500	250 430 400	300 550 450	350 700 500	250 430 400	300 600 480	350 750 550	ps
t_{SKEW}	Duty Cycle Skew (Note 21) Within-Device Skew (Note 22) Device-to-Device Skew (Note 23)		2 5 15	15 20 85		2 5 15	15 20 85		2 5 15	15 20 85	ps
t_S	Setup Time to CLK (EN to Selected CLK0:1)	110	70		110	70		115	80		ps
t_H	Hold Time (EN to Selected CLK0:1)	110	70		110	70		115	80		ps
t_{JITTER}	RMS Random Clock Jitter(Figure 3) (Note 25) Peak-to-Peak Data Dependent Jitter (Note 26) $f_{in} = 5\text{ GHz}$ $f_{in} = 5\text{ Gb/s}$		0.5	2.0		0.5 14	2.0		0.5	2.0	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 24)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% - 80%) @ 1 GHz Q, \bar{Q}	40	60	80	40	60	80	40	60	80	ps

20. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with $50\ \Omega$ to $V_{CC} - 1.5\text{ V}$. Input edge rates 40 ps (20% - 80%).

21. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform (Figure 4).

22. Within-Device skew is measured between outputs under identical transitions and conditions on any one device.

23. Device-to-Device skew for identical transitions at identical V_{CC} levels.

24. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$ (applicable only when $V_{CC} - V_{EE} < 2600\text{ mV}$).

25. Additive RMS jitter with 50% duty cycle clock signal at 5 GHz.

26. Additive Peak-to-Peak jitter with input NRZ data at PRBS $2^{31}-1$ at 5 Gb/s.

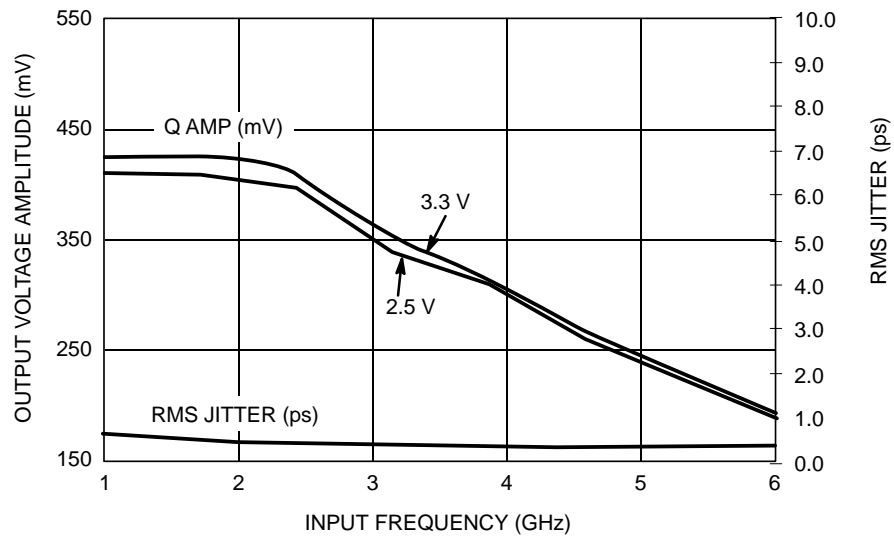


Figure 3. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

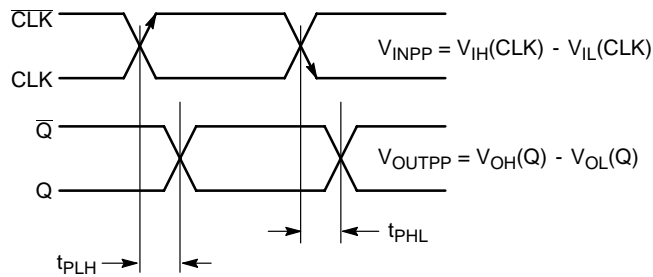


Figure 4. AC Reference Measurement

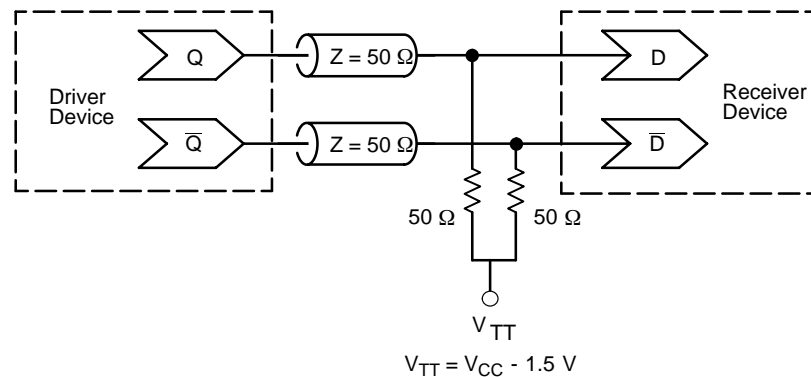
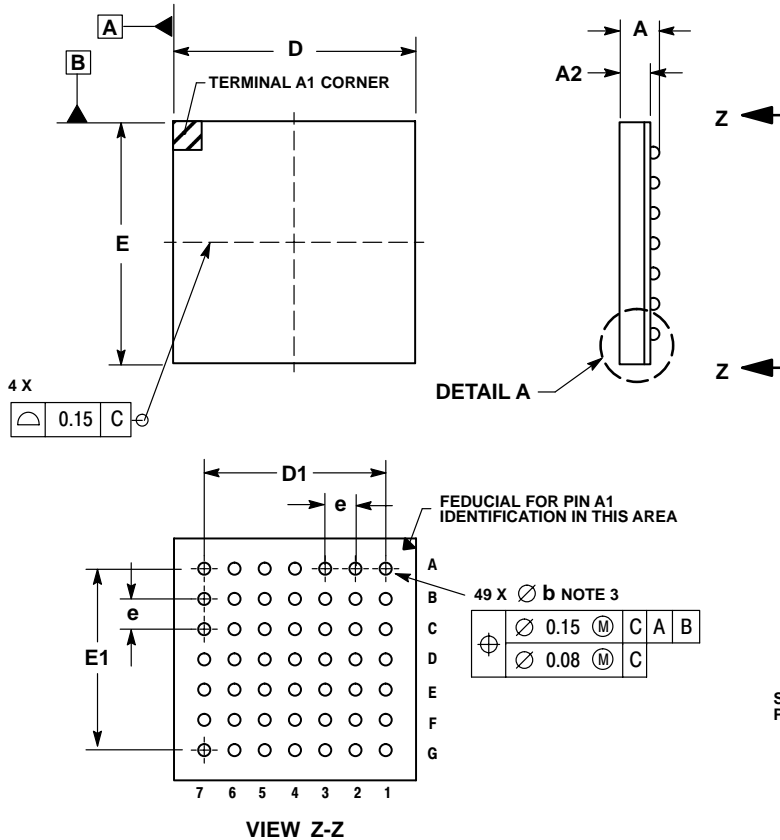


Figure 5. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 - Termination of ECL Logic Devices)

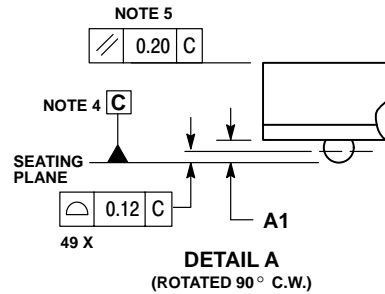
PACKAGE DIMENSIONS

FCBGA-49
BA SUFFIX
PLASTIC 8x8 mm (1.0 mm pitch) BGA FLIP CHIP PACKAGE
CASE 489A-02
ISSUE A



- NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
 2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
 4. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
 6. 489A-01 OBSOLETE, NEW STANDARD 489A-02.

MILLIMETERS		
DIM	MIN	MAX
A	---	1.40
A1	0.3	0.5
A2	0.91	REF
b	0.40	0.60
D	8.00	BSC
D1	6.00	BSC
E	8.00	BSC
E1	6.00	BSC
e	1.00	BSC



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