

NTHD3100C

Power MOSFET

Complementary, 20 V, +2.9 A / -3.2 A,
ChipFET™

Features

- Complementary N Channel and P Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Trench P-Channel for Low On Resistance
- Low Gate Charge N-Channel for Test Switching
- Pb-Free Package is Available

Applications

- DC-to-DC Conversion Circuits
- Load Switch Applications Requiring Level Shift
- Drive Small Brushless DC Motors
- Ideal for Power Management Applications in Portable, Battery Powered Products

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	20	V
Gate-to-Source Voltage	N-Ch		V _{GS}	± 12	V
	P-Ch			± 8.0	
N-Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	2.9	A
		T _A = 85°C		2.1	
	t≤10s	T _A = 25°C		3.9	
P-Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	-3.2	A
		T _A = 85°C		-2.3	
	t≤10s	T _A = 25°C		-4.4	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.1	W
Pulsed Drain Current (Note 1)	N-Ch	t = 10 μs	I _{DM}	12	A
	P-Ch	t = 10 μs		-13	
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to 150	°C
Source Current (Body Diode)			I _S	1.1	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T _L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	R _{θJA}	113	°C/W
Junction-to-Ambient – t ≤ 10 s (Note 1)	R _{θJA}	60	°C/W

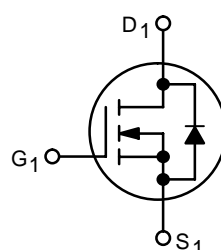
1. Surface-mounted on FR4 board using 1 in. sq. pad size (Cu area = 1.127 in. sq. [1 oz] including traces).



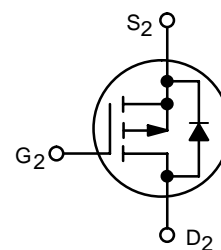
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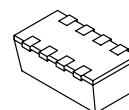
V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
N-Channel 20 V	58 mΩ @ 4.5 V	2.9 A
	77 mΩ @ 2.5 V	
P-Channel -20 V	64 mΩ @ -4.5 V	-3.2 A
	85 mΩ @ -2.5 V	



N-Channel MOSFET

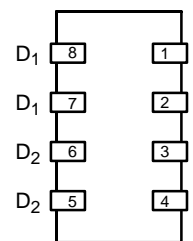


P-Channel MOSFET



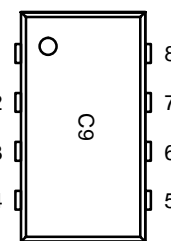
ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



Bottom View

MARKING DIAGRAM



Top View

C9 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTHD3100CT1	ChipFET	3000/Tape & Reel
NTHD3100CT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD3100C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	N	V _{GS} = 0 V	I _D = 250 μA	20		V
		P		I _D = -250 μA	-20		
Zero Gate Voltage Drain Current	I _{DSS}	N	V _{GS} = 0 V, V _{DS} = 16 V	T _J = 25 °C		1.0	μA
		P	V _{GS} = 0 V, V _{DS} = -16 V			-1.0	
		N	V _{GS} = 0 V, V _{DS} = 16 V	T _J = 125 °C		5.0	
		P	V _{GS} = 0 V, V _{DS} = -16 V			-5.0	
Gate-to-Source Leakage Current	I _{GSS}	N	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
		P	V _{DS} = 0 V, V _{GS} = ±8.0 V			±100	

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	N	V _{GS} = V _{DS}	I _D = 250 μA	0.6	1.2	V
		P		I _D = -250 μA	-.45	-1.5	
Drain-to-Source On Resistance	R _{DS(on)}	N	V _{GS} = 4.5 V, I _D = 2.9 A		58	80	mΩ
		P	V _{GS} = -4.5 V, I _D = -3.2 A		64	80	
		N	V _{GS} = 2.5 V, I _D = 2.3 A		77	115	
		P	V _{GS} = -2.5 V, I _D = -2.2 A		85	110	
Forward Transconductance	g _{FS}	N	V _{DS} = 10 V, I _D = 2.9 A		6.0		S
		P	V _{DS} = -10 V, I _D = -3.2 A		8.0		

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	N	f = 1 MHz, V _{GS} = 0 V	V _{DS} = 10 V		165	pF
		P		V _{DS} = -10 V		680	
Output Capacitance	C _{OSS}	N		V _{DS} = 10 V		80	
		P		V _{DS} = -10 V		100	
Reverse Transfer Capacitance	C _{RSS}	N		V _{DS} = 10 V		25	
		P		V _{DS} = -10 V		70	
Total Gate Charge	Q _{G(TOT)}	N		V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 2.9 A		2.3	nC
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -3.2 A		7.4	
Threshold Gate Charge	Q _{G(TH)}	N		V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 2.9 A		0.2	
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -3.2 A		0.6	
Gate-to-Source Gate Charge	Q _{GS}	N		V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 2.9 A		0.4	
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -3.2 A		1.4	
Gate-to-Drain "Miller" Charge	Q _{GD}	N		V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 2.9 A		0.7	
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -3.2 A		2.5	

2. Pulse Test: pulse width ≤ 250 μs, duty cycle ≤ 2%.

NTHD3100C

ELECTRICAL CHARACTERISTICS (continued) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	N	$V_{GS} = 4.5\text{ V}, V_{DD} = 10\text{ V},$ $I_D = 2.9\text{ A}, R_G = 2.5\ \Omega$		6.3		ns
Rise Time	t_r				10.7		
Turn-Off Delay Time	$t_{d(OFF)}$				9.6		
Fall Time	t_f				1.5		
Turn-On Delay Time	$t_{d(ON)}$	P	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V},$ $I_D = -3.2\text{ A}, R_G = 2.5\ \Omega$		5.8		
Rise Time	t_r				11.7		
Turn-Off Delay Time	$t_{d(OFF)}$				16		
Fall Time	t_f				12.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	N	$V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	$I_S = 2.9\text{ A}$		0.8	1.15	V
		P		$I_S = -3.2\text{ A}$		-0.8	-1.2	
Reverse Recovery Time	t_{RR}	N	$V_{GS} = 0\text{ V},$ $dI_S / dt = 100\text{ A}/\mu\text{s}$	$I_S = 1.5\text{ A}$		12.5		ns
		P		$I_S = -1.5\text{ A}$		13.5		
Charge Time	t_a	N		$I_S = 1.5\text{ A}$		9.0		
		P		$I_S = -1.5\text{ A}$		9.5		
Discharge Time	t_b	N		$I_S = 1.5\text{ A}$		3.5		
		P		$I_S = -1.5\text{ A}$		4.0		
Reverse Recovery Charge	Q_{RR}	N		$I_S = 1.5\text{ A}$		6.0		nC
		P		$I_S = -1.5\text{ A}$		6.5		

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

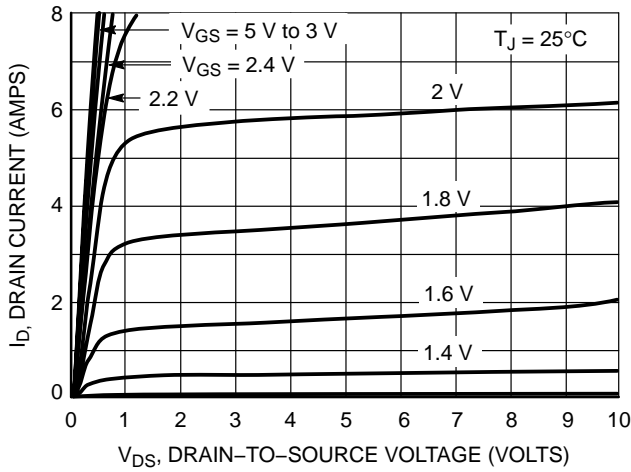


Figure 1. On-Region Characteristics

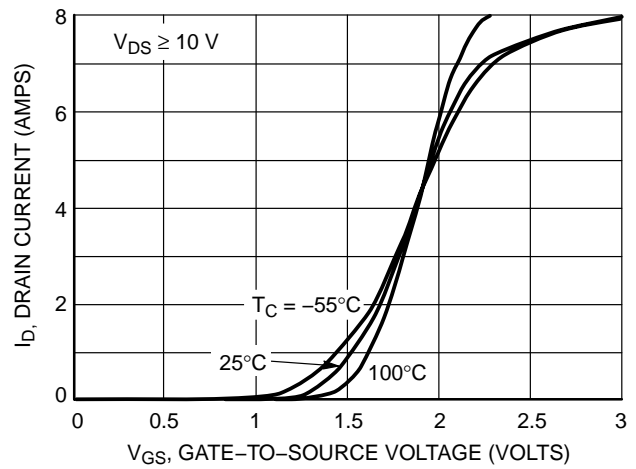


Figure 2. Transfer Characteristics

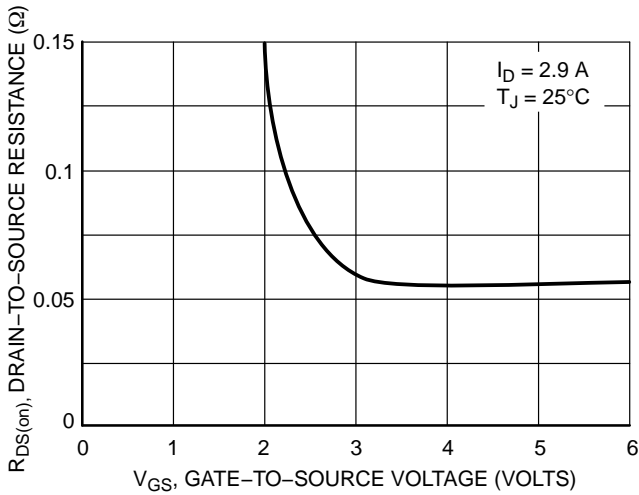


Figure 3. On-Resistance vs. Gate-to-Source Voltage

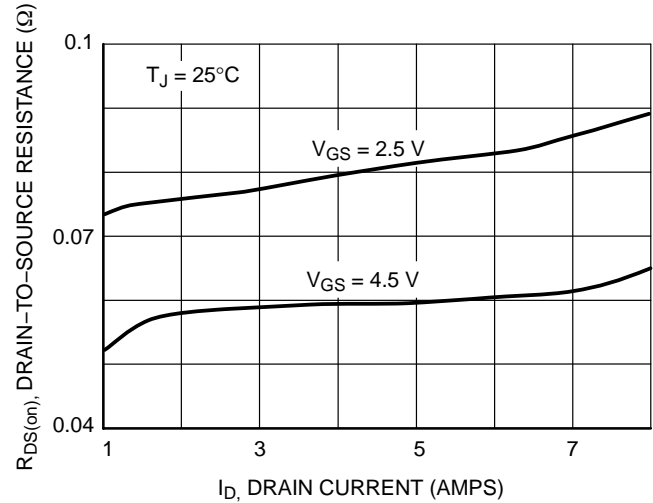


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

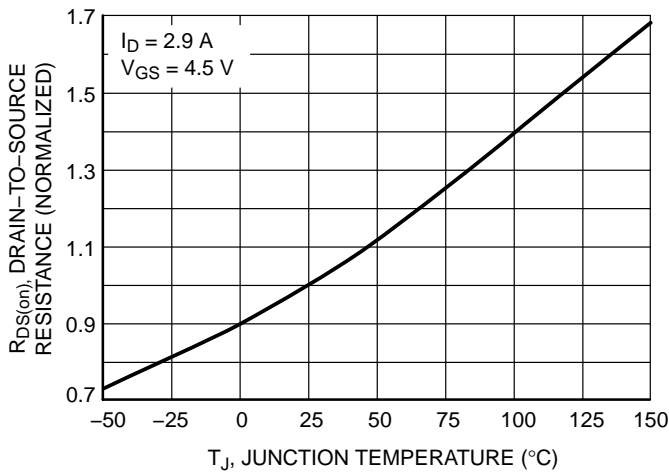


Figure 5. On-Resistance Variation with Temperature

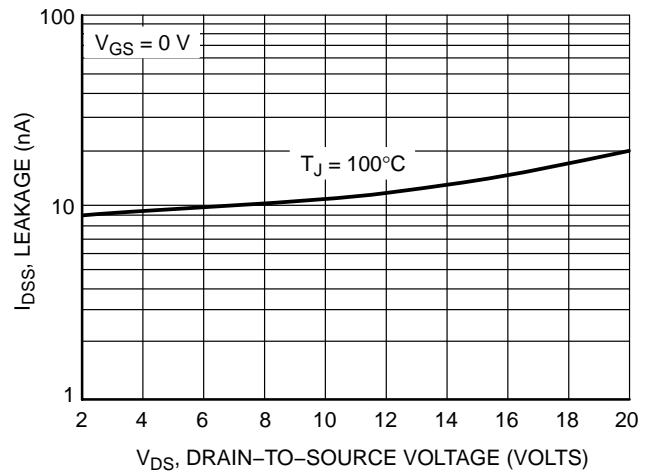


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

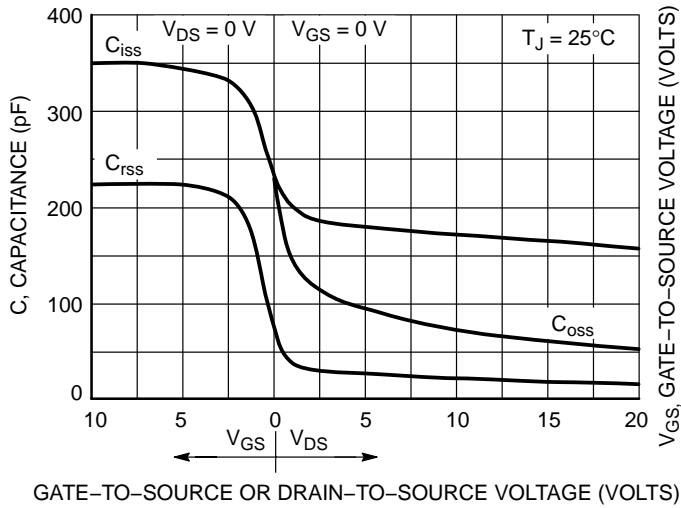


Figure 7. Capacitance Variation

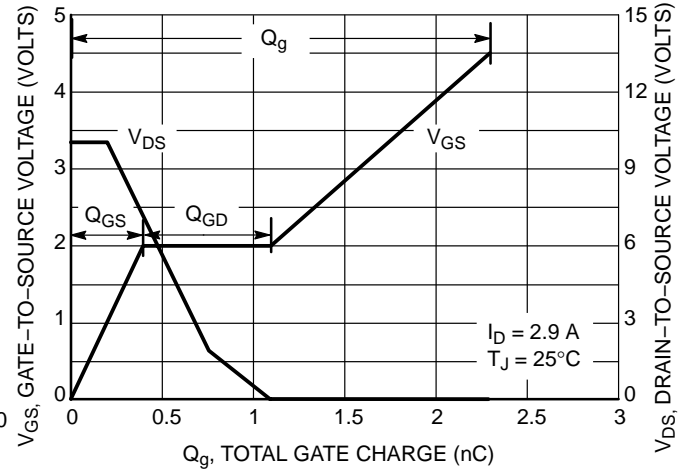


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

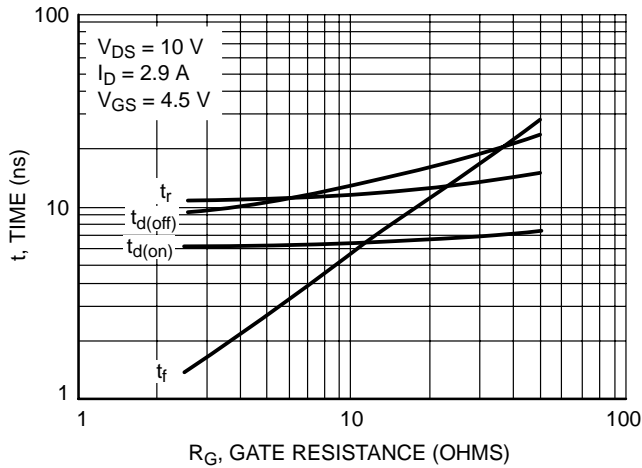


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

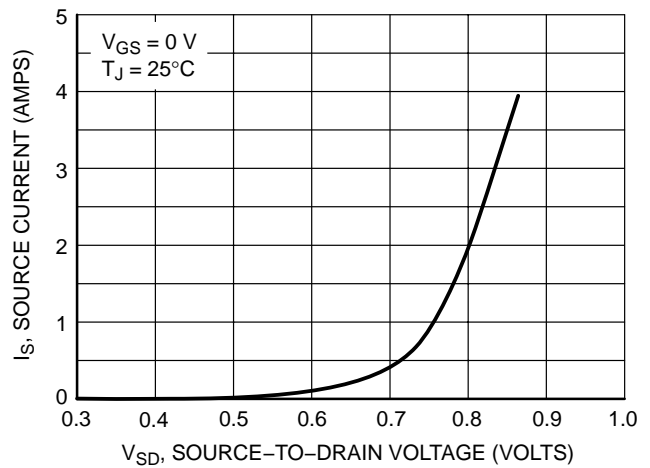


Figure 10. Diode Forward Voltage vs. Current

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

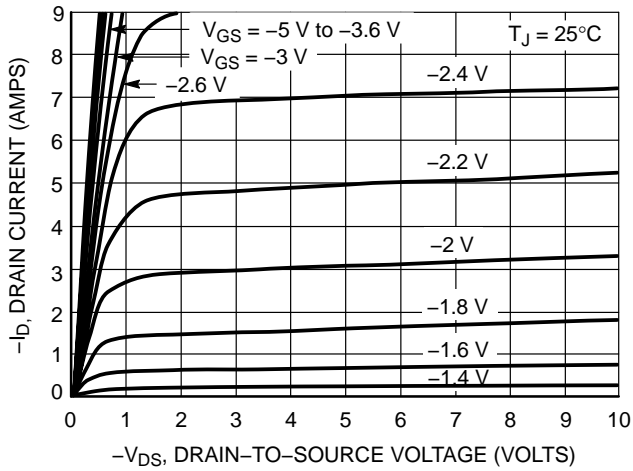


Figure 11. On-Region Characteristics

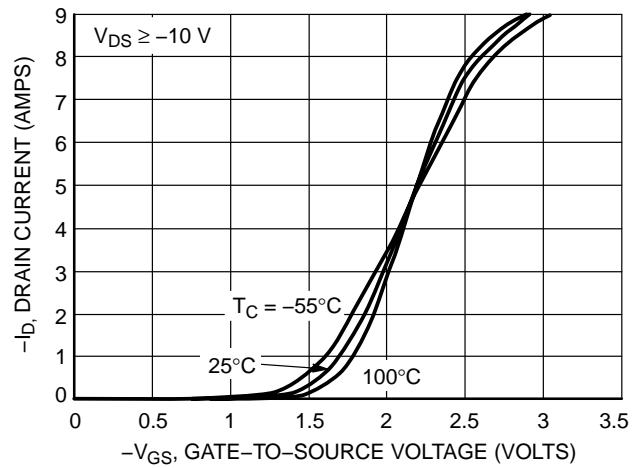


Figure 12. Transfer Characteristics

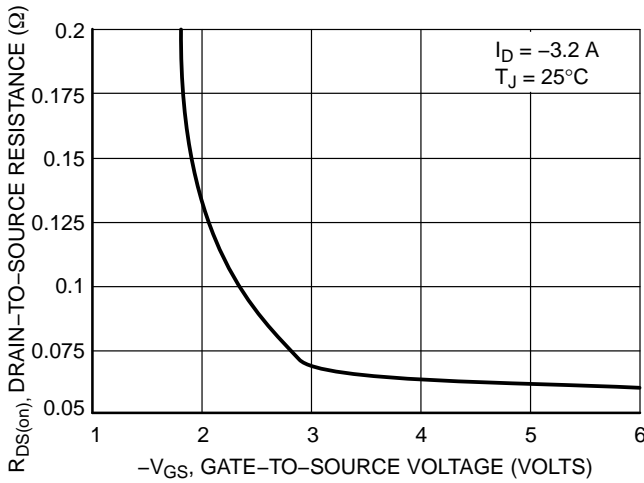


Figure 13. On-Resistance vs. Gate-to-Source Voltage

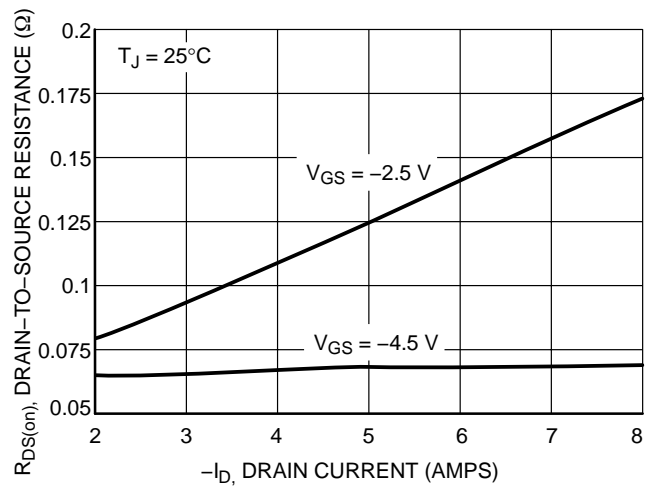


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

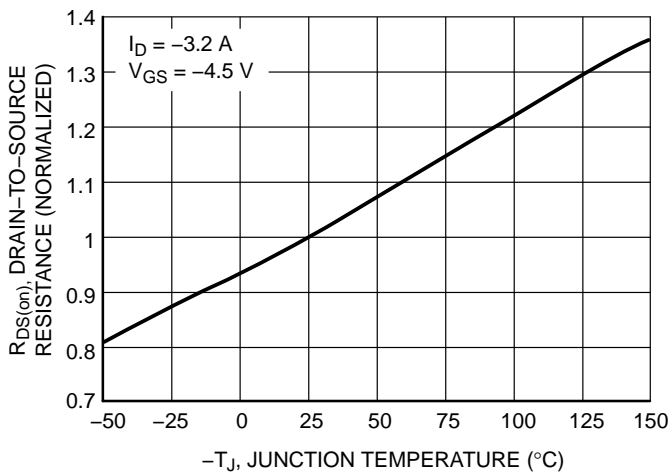


Figure 15. On-Resistance Variation with Temperature

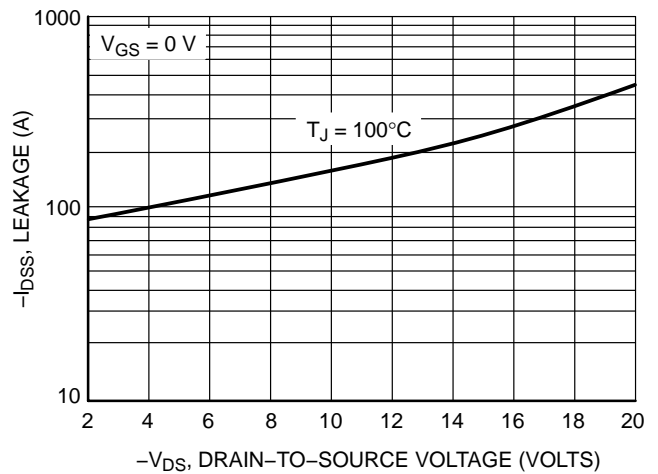
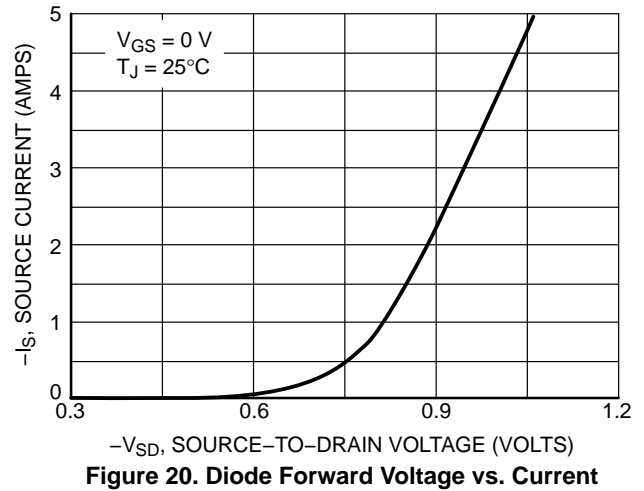
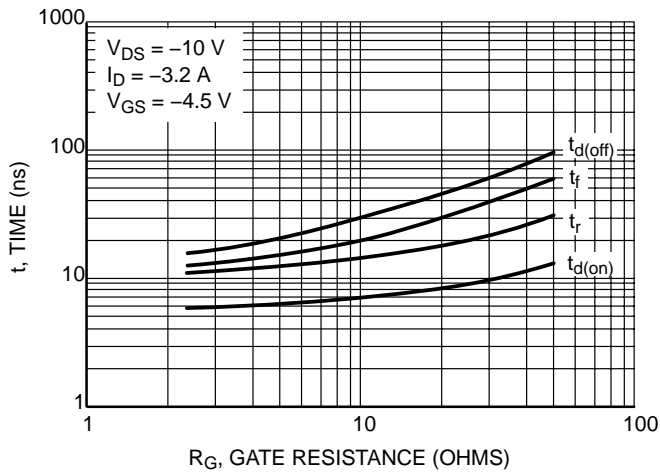
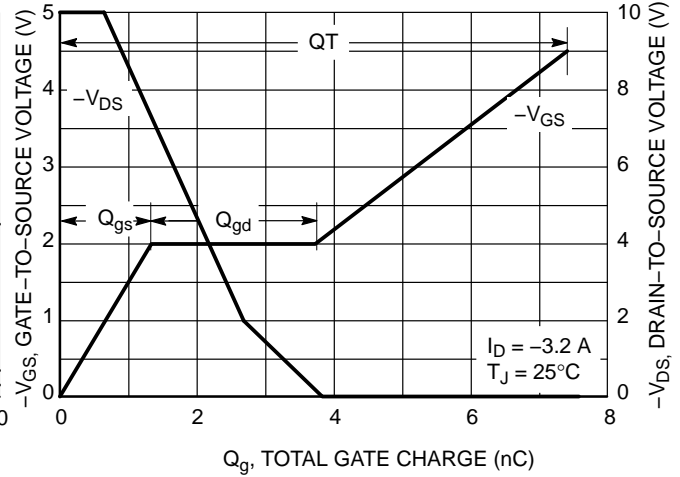
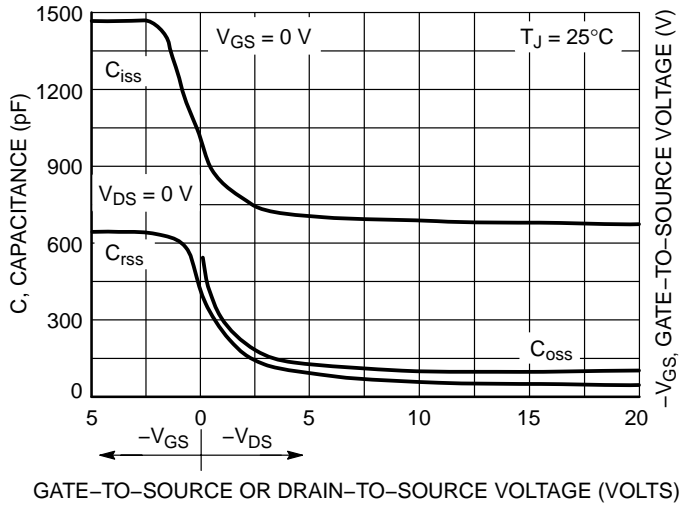


Figure 16. Drain-to-Source Leakage Current vs. Voltage

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)



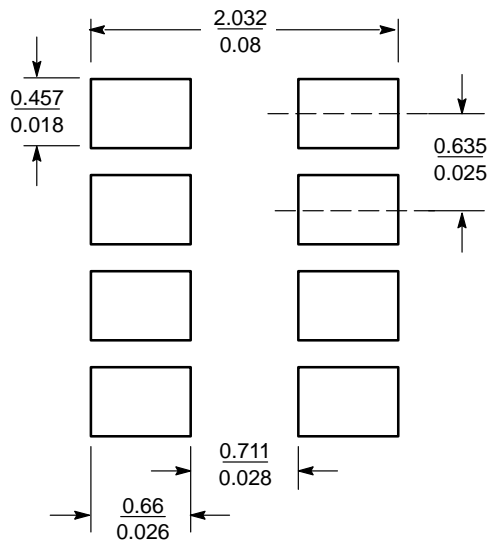


Figure 21. Basic

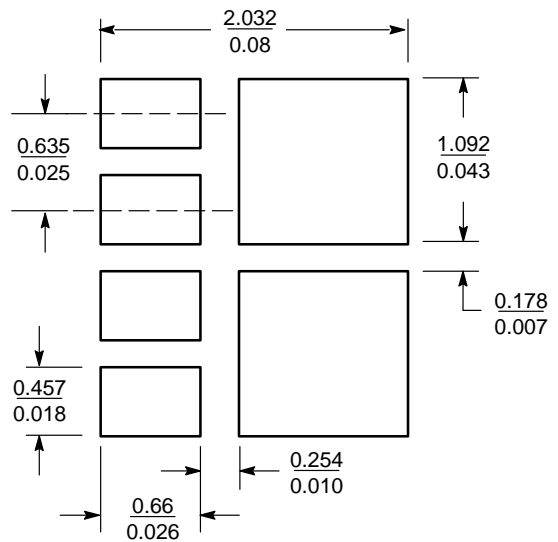


Figure 22. Style 2

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 21. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

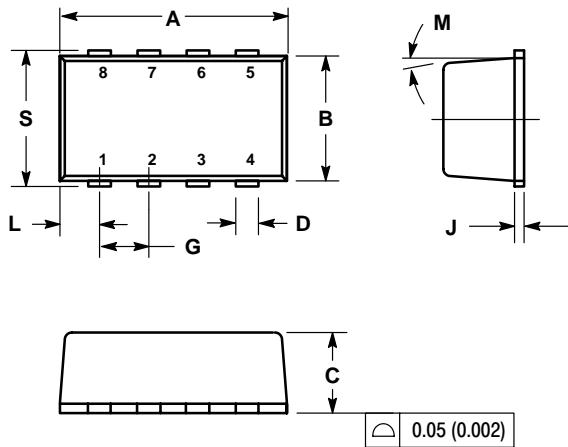
The minimum recommended pad pattern shown in Figure 22 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

NTHD3100C

PACKAGE DIMENSIONS

ChipFET CASE 1206A-03 ISSUE E




STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

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