

Octal registered transceiver, inverting (3-State)

74ABT2953

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT2953 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2953 device is an 8-bit registered inverting transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{\text{CEXX}}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable (OEXX) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

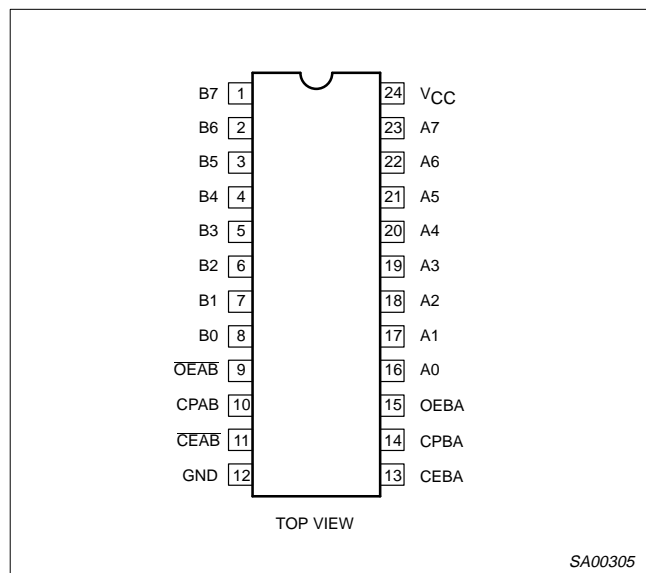
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to $\overline{\text{A}}_n$ or CPAB to $\overline{\text{B}}_n$	$C_L = 50\text{pF}$; $V_{\text{CC}} = 5\text{V}$	5.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
$C_{\text{I/O}}$	I/O capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	−40°C to +85°C	74ABT9253 N	74ABT2953 N	SOT222-1
24-Pin plastic SO	−40°C to +85°C	74ABT2953 D	74ABT2953 D	SOT137-1
24-Pin Plastic SSOP Type II	−40°C to +85°C	74ABT2953 DB	74ABT2953 DB	SOT340-1
24-Pin Plastic TSSOP Type I	−40°C to +85°C	74ABT2953 PW	74ABT2953PW DH	SOT355-1

PIN CONFIGURATION



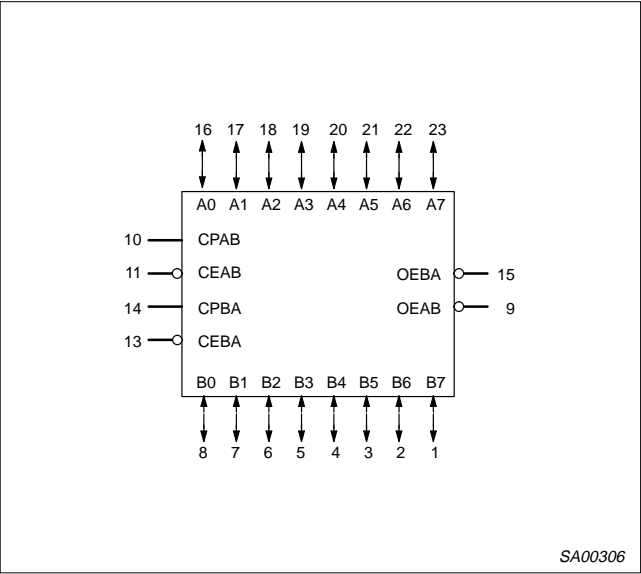
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{\text{CEAB}}$ / $\overline{\text{CEBA}}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
1, 2, 3, 4, 5, 6, 7, 8	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{\text{OEAB}}$ / $\overline{\text{OEBA}}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

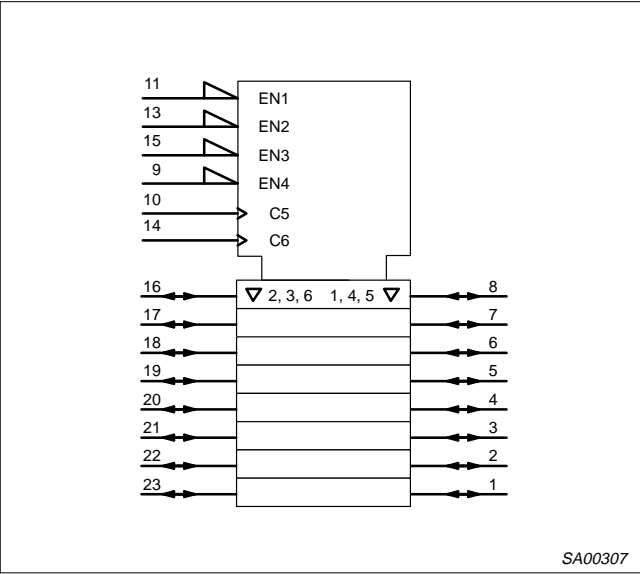
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL	OPERATING
An or Bn	CPXX	CEXX		
			Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX= AB or BA
NC= No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	An or Bn	OPERATING
OEXX		OUTPUTS	
H	X	Z	Disable outputs
L	L	H	Enable outputs
L	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
XX= AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	−50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		−65 to 150	°C

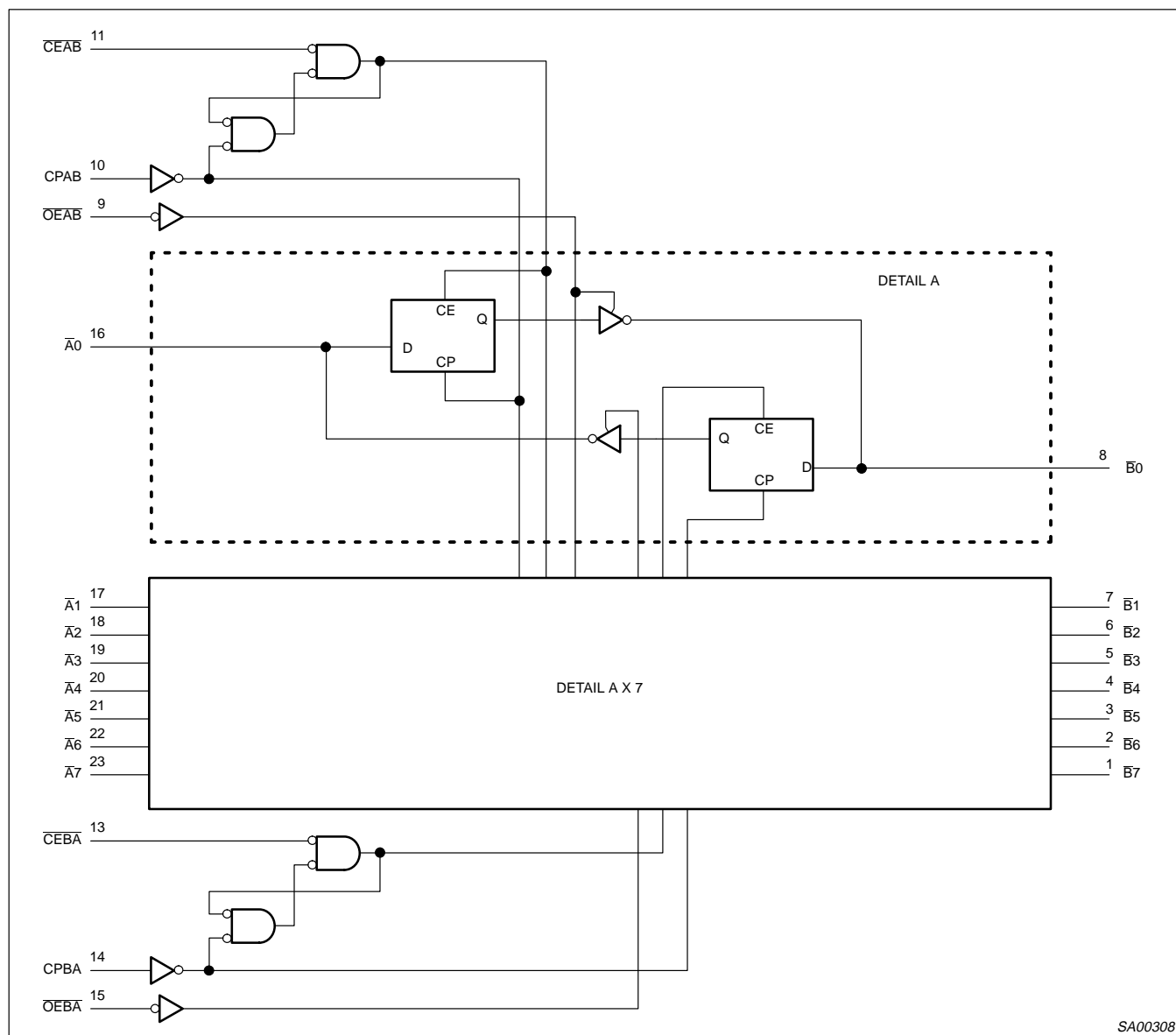
NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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LOGIC DIAGRAM



SA00308

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage		V _{CC} = 4.5V; I _{IK} = −18mA		−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage		V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	2.5	3.2		2.5		V
			V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	3.0	3.7		3.0		V
			V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}	2.0	2.3		2.0		V
V _{OL}	Low-level output voltage		V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³		V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
		Data pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±5	±100		±100	μA
I _{OFF}	Power-off leakage current		V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU/IPD}	Power-up/down 3-State output current ⁴		V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA
I _{OZH}	3-State output High current		V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current		V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		−5.0	−50		−50	μA
I _{CEX}	Output High leakage current		V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹		V _{CC} = 5.5V; V _O = 2.5V	−50	−65	−180	−50	−180	mA
I _{CCH}	Quiescent supply current		V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		110	250		250	μA
I _{CCL}			V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		20	30		30	mA
I _{CCZ}			V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		110	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²		V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.3	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$ a transition time of up to 100 μsec is permitted.

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AC CHARACTERISTICS

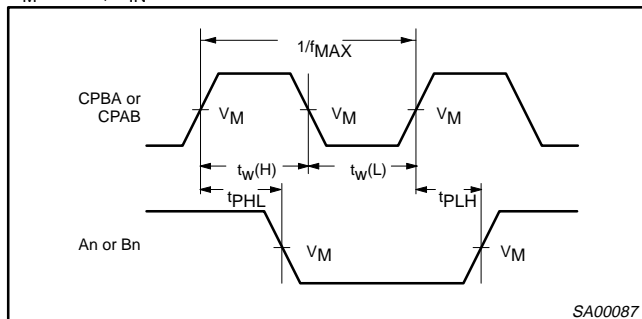
GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40°C to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	150	200		150		MHz
t _{PLH} t _{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	2.0 2.5	5.1 5.7	6.6 7.2	2.0 2.5	7.6 8.2	ns
t _{PZH} t _{PZL}	Output enable time OEBA to An, OEAB to Bn	3 4	1.0 2.2	4.0 5.3	4.8 6.2	1.0 2.2	5.8 7.5	ns
t _{PHZ} t _{PLZ}	Output disable time OEBA to An, OEAB to Bn	3 4	2.0 1.5	6.1 5.6	7.6 7.1	2.0 1.5	8.1 7.6	ns

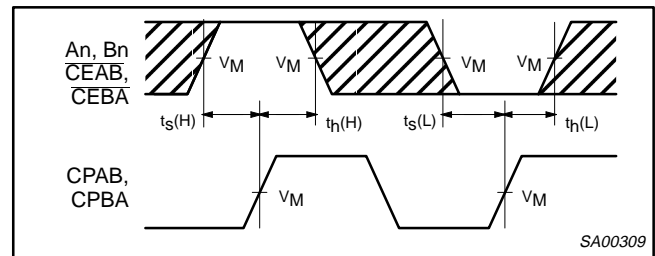
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time An to CPAB or Bn to CPBA	2	4.0 3.0	2.5 1.1	4.0 3.0	ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time An to CPAB or Bn to CPBA	2	0.0 0.0	-1.0 -2.0	0.0 0.0	ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time $\overline{\text{CEAB}}$ to CPAB, $\overline{\text{CEBA}}$ to CPBA	2	3.5 2.5	2.0 0.9	3.5 2.5	ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time $\overline{\text{CEAB}}$ to CPAB, $\overline{\text{CEBA}}$ to CPBA	2	0.0 0.0	-0.5 -1.0	0.0 0.0	ns
$t_{\text{W}}(\text{H})$ $t_{\text{W}}(\text{L})$	CPAB or CPBA pulse width, High or Low	1	3.0 3.5	2.0 1.1	3.0 3.5	ns

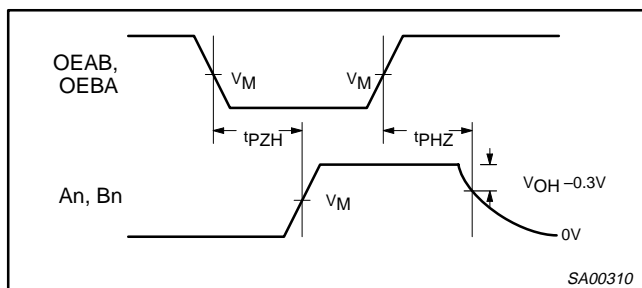
AC WAVEFORMS

 $V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$ 

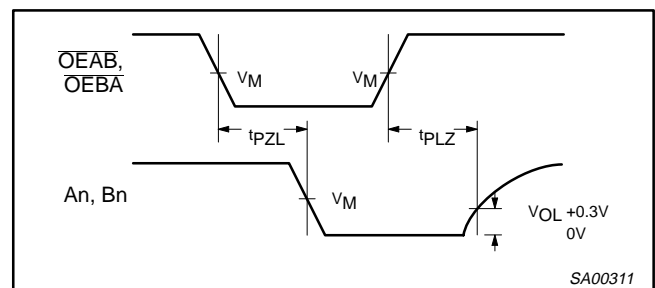
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORMS

