DATA SHEET

74AHC164; 74AHCT164
8-bit serial-in/parallel-out shift register

Product specification
2000 Aug 15
File under Integrated Circuits, IC06

Philips Semiconductors

PHILIPS

8-bit serial-in/parallel-out shift register — 74AHC164; 74AHCT164

FEATURES

- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V
  CDM EIA/JESD22-C101 exceeds 1000 V
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from –40 to +85 °C and from –40 to +125 °C.

DESCRIPTION

The 74AHC/AHCT164 shift registers are high-speed silicon-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT164 input signals are 8-bit serial through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is a logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	CP to Q_n		4.5	3.4	ns
	$\overline{MR}$ to Q_n		4.0	3.5	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND	3	3	pF
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	175	175	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	48	51	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts.

2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1-Q_7
reset (clear)	L	X	X	X	L	L-L
shift	H	↑	l	l	L	q_0-q_6
	H	↑	l	h	L	q_0-q_6
	H	↑	h	l	L	q_0-q_6
	H	↑	h	h	H	q_0-q_6

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
   ↑ = LOW-to-HIGH transition;
   X = don't care;
   q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AHC164D	–40 to +125 °C	14	SO	plastic	SOT108-1
74AHC164PW		14	TSSOP	plastic	SOT402-1
74AHCT164D		14	SO	plastic	SOT108-1
74AHCT164PW		14	TSSOP	plastic	SOT402-1

PINNING

PIN	SYMBOL	DESCRIPTION
1, 2	D_{sa}, D_{sb}	data input
3, 4, 5, 6, 10, 11, 12, 13	Q_0 to Q_7	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
14	V_{CC}	DC supply voltage

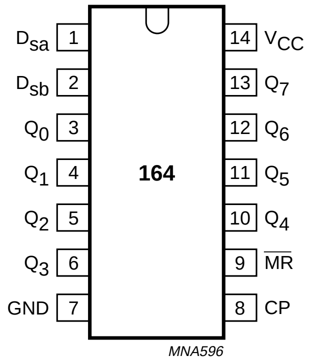


Fig.1 Pin configuration.

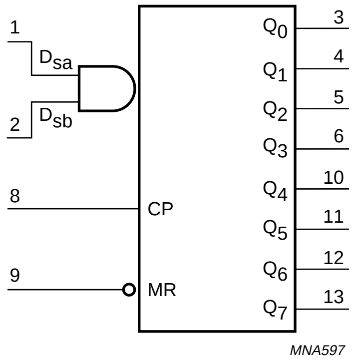


Fig.2 Logic symbol.

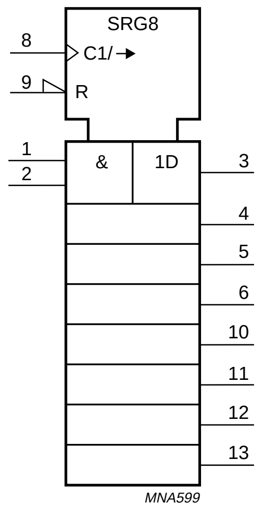


Fig.3 IEC logic symbol.

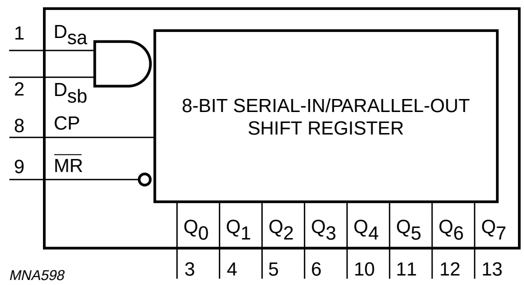


Fig.4 Functional diagram.

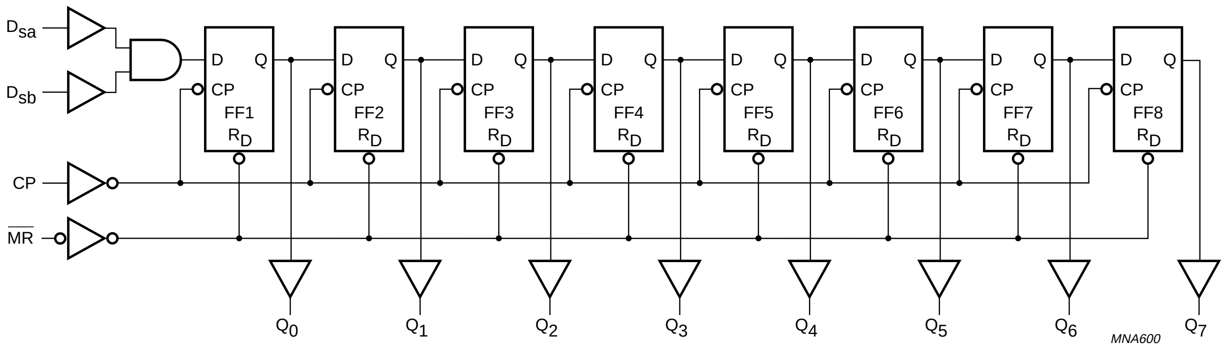


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall ratios (Δt/ΔV)	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ±0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	DC input diode current	V_I < –0.5 V; note 1	–	–20	mA
I_{OK}	DC output clamping diode current	–0.5 > V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	DC output sink current	–0.5 < V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}	DC V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO packages: above 70 °C the value of P_D derates linearly by 8 mW/K.
   For TSSOP packages: above 60 °C the value of P_D derates linearly by 5.5 mW/K.

DC CHARACTERISTICS

74AHC family

With regard to recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	V
			5.5	3.85	–	–	3.85	–	3.85	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	V
			5.5	–	–	1.65	–	1.65	–	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ μA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	V
			4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -4.0$ mA	3.0	2.58	–	–	2.48	–	2.40	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ μA	2.0	–	0	0.1	–	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	–	0.1	V
			4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	μA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

74AHCT family

With regard to recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ µA	4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL}	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V other inputs at V_{CC} or GND; $I_O = 0$	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

AC CHARACTERISTICS

Type 74AHC164

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 3.0 to 3.6 V; typical values at V_{CC} = 3.3 V											
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 9	15 pF	–	6.5	12.8	1.0	15.0	1.0	16.0	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	see Figs 7 and 9		–	5.3	12.8	1.0	15.0	1.0	16.0	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 9		80	125	–	65	–	50	–	MHz
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 9	50 pF	–	9.3	16.3	1.0	18.5	1.0	20.5	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	see Figs 7 and 9		–	7.6	16.3	1.0	18.5	1.0	20.5	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 9		5.0	–	–	5.0	–	5.0	–	ns
	master reset pulse width LOW	see Figs 7 and 9		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time D_{sa}, D_{sb} to CP	see Figs 8 and 9		5.0	–	–	6.0	–	6.0	–	ns
t_h	hold time D_{sa}, D_{sb} to CP	see Figs 8 and 9		1.5	–	–	1.5	–	1.5	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 7 and 9		2.5	–	–	2.5	–	2.5	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 9		50	75	–	45	–	35	–	MHz

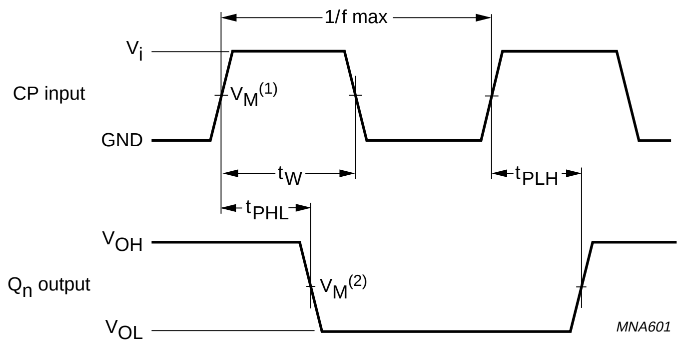
SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; typical values at V_{CC} = 5.0 V											
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 9	15 pF	–	4.5	9.0	1.0	10.5	1.0	11.5	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	see Figs 7 and 9		–	4.0	8.6	1.0	10.0	1.0	11.0	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 9		125	175	–	105	–	85	–	MHz
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 9	50 pF	–	6.4	11.0	1.0	12.5	1.0	14.0	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	see Figs 7 and 9		–	5.8	10.6	1.0	12.0	1.0	13.5	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 9		5.0	–	–	5.0	–	5.0	–	ns
	master reset pulse width LOW	see Figs 7 and 9		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time D_{sa}, D_{sb} to CP	see Figs 8 and 9		4.5	–	–	4.5	–	4.5	–	ns
t_h	hold time D_{sa}, D_{sb} to CP	see Figs 8 and 9		2.0	–	–	2.0	–	2.0	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 7 and 9		2.5	–	–	2.5	–	2.5	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 9		85	115	–	75	–	65	–	MHz

Type 74AHCT164

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

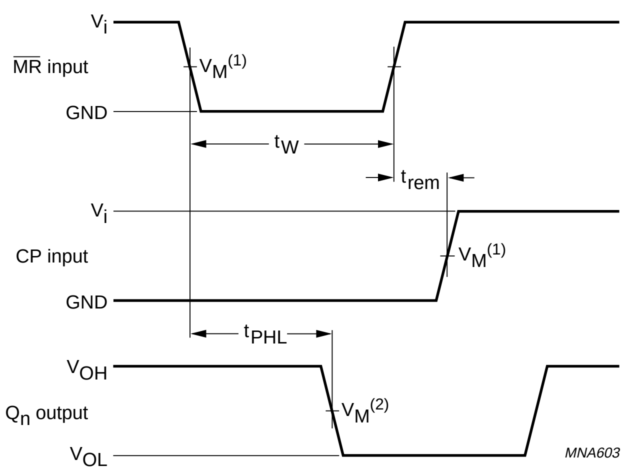
SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; typical values at V_{CC} = 5.0 V											
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 9	15 pF	–	3.4	9.0	1.0	10.5	1.0	11.5	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	see Figs 7 and 9		–	3.5	8.6	1.0	10.0	1.0	11.0	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 9		125	175	–	105	–	85	–	MHz
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	see Figs 6 and 9	50 pF	–	4.9	11.0	1.0	12.5	1.0	14.0	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	see Figs 7 and 9		–	5.0	10.6	1.0	12.0	1.0	13.5	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 9		5.0	–	–	5.0	–	5.0	–	ns
	master reset pulse width LOW	see Figs 7 and 9		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time D_{sa}, D_{sb} to CP	see Figs 8 and 9		4.5	–	–	4.5	–	4.5	–	ns
t_h	hold time D_{sa}, D_{sb} to CP	see Figs 8 and 9		2.0	–	–	2.0	–	2.0	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 7 and 9		2.5	–	–	2.5	–	2.5	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 9		85	115	–	75	–	65	–	MHz

AC WAVEFORMS



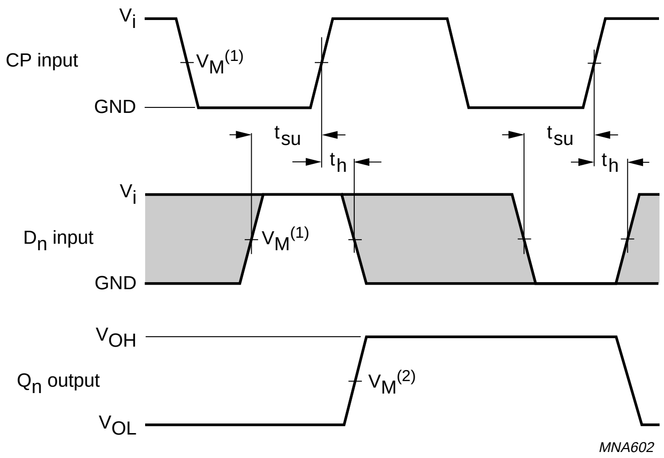
FAMILY	V_I INPUT REQUIREMENTS	V_M(1) INPUT	V_M(2) OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.6 The clock (CP) to output (Q_n) propagation delays, the shift clock pulse width (t_W) and maximum shift clock frequency (f_{max}).



FAMILY	V_I INPUT REQUIREMENTS	V_M(1) INPUT	V_M(2) OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

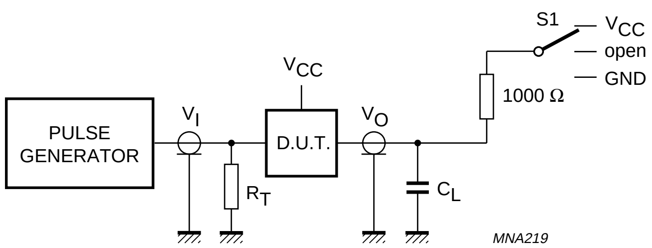
Fig.7 The master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n), propagation delays and the master reset clock (CP) removal time (t_{rem}).



FAMILY	V_I INPUT REQUIREMENTS	V_M(1) INPUT	V_M(2) OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.8 The data set-up (t_{su}) and hold (t_h) times for the (D_n) input.



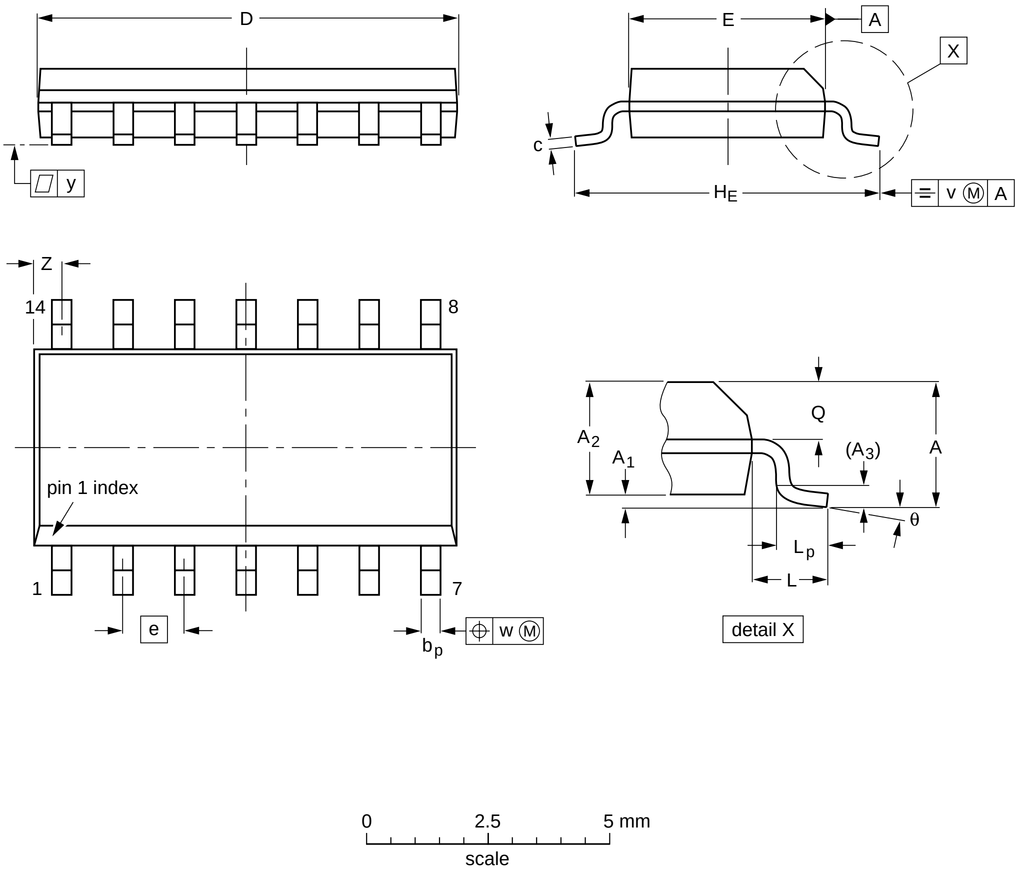
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit.
C_L = load capacitance including jig and probe capacitance (see Chapter "AC characteristics").
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuit for switching times.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

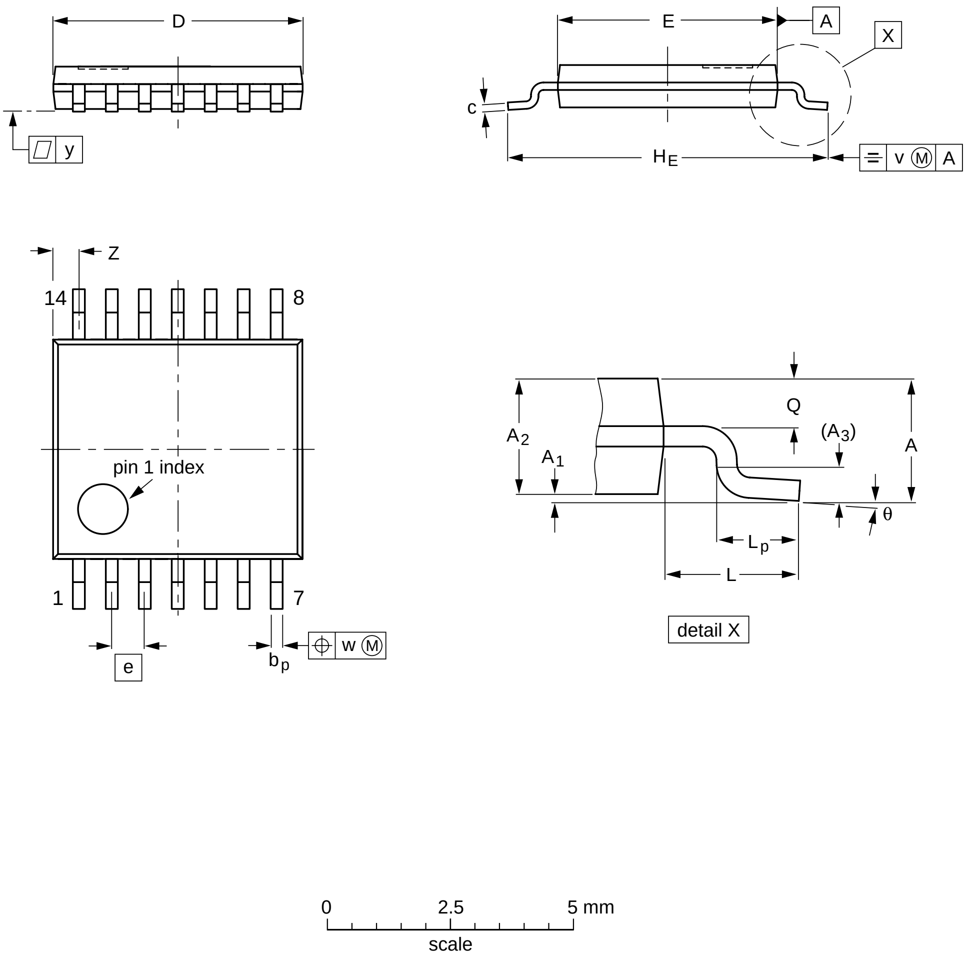
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**[(1)]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[(2)]	suitable
PLCC[(3)], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[(3)(4)]	suitable
SSOP, TSSOP, VSO	not recommended[(5)]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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