

DATA SHEET

74HCT1284

Parallel printer interface transceiver/buffer

Product specification
Supersedes data of 1995 Jun 27
IC06 Data Handbook

1998 Jul 10

Parallel printer interface transceiver/buffer

74HCT1284

FEATURES

- Asynchronous operation
- 4-Bit transceivers
- 3 additional buffer/driver lines
- TTL compatible inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Input Hysteresis
- Low Noise Operation
- Center Pin V_{CC} & GND
- IEEE 1284 Compliant Level 1 & 2
- Overvoltage Protection on B side

DESCRIPTION

The 74HCT1284 parallel interface chip is designed to provide an asynchronous, 4-bit, bi-directional, parallel printer interface for personal computers. Three additional lines are included to provide handshaking signals between the host and the peripheral. The part is designed to match IEEE 1284 standard.

The 4 transceiver pins (A/B 1-4) allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending on the state of the direction pin DIR.

The B bus and the Y5-Y7 lines have totem pole or open drain style outputs depending on the state of the high drive enable pin HD. The A bus only has totem pole style outputs. All inputs are TTL compatible with at least 400mV of input hysteresis at $V_{CC} = 5.0V$.

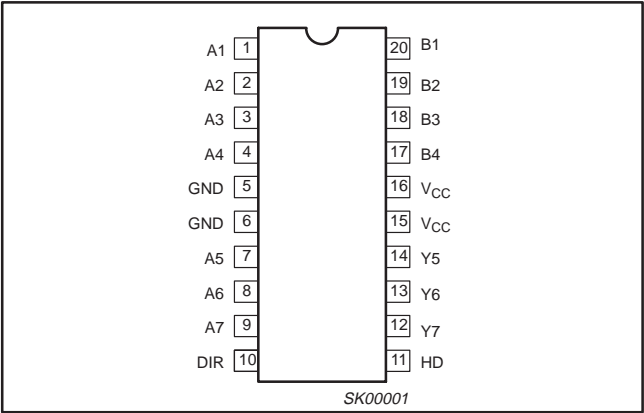
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Bn to An	$C_L = 50pF$; $V_{CC} = 5V$	5.3 5.6	ns ns
C_{IN}	Input capacitance A_n , DIR, HD	$V_I = 0V$ or V_{CC}	5	pF
C_{OUT}	Output capacitance B_n , Y_n	$V_O = 0V$ or V_{CC} ; 3-State	14	pF
I_{CC}	Total supply current	$V_{CC} = 5.5V$	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	0°C to +70°C	74HCT1284N	SOT146-1
20-pin plastic SOL	0°C to +70°C	7HCT1284D	SOT163-1
20-pin plastic SSOP Type II	0°C to +70°C	74HCT1284DB	SOT339-1
20-pin plastic TSSOP Type I	0°C to +70°C	74HCT1284PW	SOT360-1

PIN CONFIGURATION



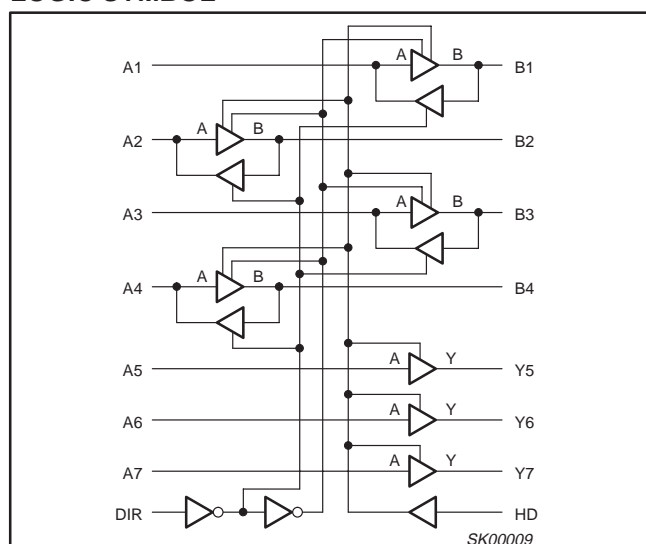
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,2,3,4 20,19,18,17	A1 - A4 B1 - B4	Data inputs/outputs
7,8,9 14,13,12	A5 - A7 Y5 - Y7	Buffer/Driver lines
10,11	DIR,HIGH DRIVE	Direction, Drive
5,6	GND	Ground (0V)
15,16	V_{CC}	Positive supply voltage

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LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	INPUTS/OUTPUTS	
DIR	HD	A5-7	Y5-7	A1-4	B1-4
L	L	L	L	A = B	Inputs
L	L	H	Z	A = B	Inputs
L	H	L	L	A = B	Inputs
L	H	H	H	A = B	Inputs
H	L	L	L	Inputs Low	Outputs Low
H	L	H	Z	Inputs High	Outputs Z
H	H	L	L	Inputs	B = A
H	H	H	H	Inputs	B = A

H = High Voltage

L = Low Voltage

Z = High Impedance, Off-State

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	± 20	mA
V_I	DC input voltage ³		-2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	± 50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	± 50	mA
T_{stg}	Storage temperature range		-65 to 150	°C
I_{CC}/I_{GND}	Continuous current through V_{CC} or GND		± 200	mA

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.7	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-14	mA
I_{OL}	Low-level output current		14	mA
T_{amb}	Operating free-air temperature range	0	+70	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T _{amb} = 25°C			T _{amb} = 0°C to +70°C		
				MIN	TYP	MAX	MIN	MAX	
V _{OH}	High-level output voltage	A _n	V _{CC} = Min to Max; I _{OH} = −50μA	V _{CC} −0.2	V _{CC}		V _{CC} −0.2		V
			V _{CC} = 4.7V; I _{OH} = −4mA	4.3	4.6		3.7		V
		B _n or Y _n	V _{CC} = 4.7V; I _{OH} = −14mA	2.6	2.9		2.4		V
V _{OL}	Low-level output voltage	A _n	V _{CC} = Min to Max; I _{OL} = 50μA; V _I = V _{IL} or V _{IH}		0	0.2		0.2	V
			V _{CC} = 4.7V; I _{OL} = 4mA; V _I = V _{IL} or V _{IH}		0.1	0.25		0.4	V
		B _n or Y _n	V _{CC} = 4.7V; I _{OL} = 14mA; V _I = V _{IL} or V _{IH}		0.15	0.3		0.4	V
V _{HYS}	Input Hysteresis		V _{CC} = 5.0V	0.4	0.50		0.4		V
R _D	B/Y side Output Impedance		See Figure 1	8	15	22	8	22	Ω
I _I	Input leakage current (A5–A7)		V _{CC} = 5.5V; V _O = V _{CC} or GND		±0.5	±1.0		±5.0	μA
I _{OFF}	B/Y Side Power-off leakage current		V _{CC} = 0.0V; V _O = 0 to 7V		±1	±10		±100	μA
I _{OZH}	3-State output High current Y _n		V _{CC} = 5.5V; V _O = V _{CC} ; V _I = V _{IL} or V _{IH}		1	5		20	μA
I _{OZL}	3-State output Low current Y _n		V _{CC} = 5.5V; V _O = GND; V _I = V _{IL} or V _{IH}		−1	−5		−20	μA
I _{IH} +I _{OZH}	current (A ₁ – A ₄ , B _n)		V _{CC} = 5.5V; V _{I/O} = V _{CC}		1	5		25	μA
I _{IL} +I _{OZL}	current (A ₁ – A ₄ , B _n)		V _{CC} = 5.5V; V _{I/O} = GND		−1	−5		−25	μA
I _{CC}	Quiescent Supply Current		V _{CC} = 5.5V; I _O = 0; V _I = GND or V _{CC}		0.5	250		400	μA

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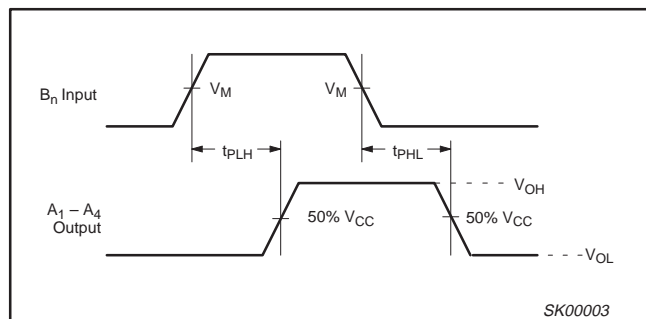
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AC CHARACTERISTICS

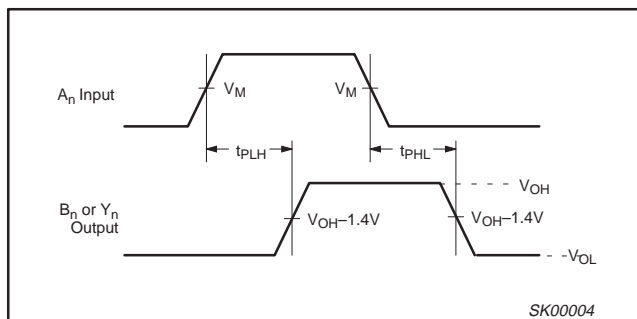
GND = 0V, $t_R = t_F = 3.0\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = 25°C V _{CC} = 5.0V			T _{amb} = 0 to + 70°C V _{CC} = Min to Max		
			MIN	TYP	MAX	MIN	MAX	
SR	B-Side Slew Rate		0.05	0.11	0.4	0.05	0.4	V/ns
t _{PLH} t _{PHL}	Propagation delay A to Y or A to B	2	5.0 5.0	13.9 21.0	17.1 25.7	5.0 5.0	22 31	ns
t _{PLH} t _{PHL}	Propagation delay B to A	1	1.5 1.5	5.3 5.6	7.5 7.9	1.5 1.5	9.0 10.0	ns
t _{PZH} t _{PHZ}	Output enable/disable time to/from High level HD to Y or HD to B	3	4.0 2.0	12.0 6.5	16.0 9.1	4.0 2.0	20.0 11.0	ns
t _{PZL} t _{PLZ}	Output enable/disable time to/from Low level A to Y or A to B	4	5.0 1.5	12.7 5.0	16.3 7.1	5.0 1.5	20.0 9.0	ns

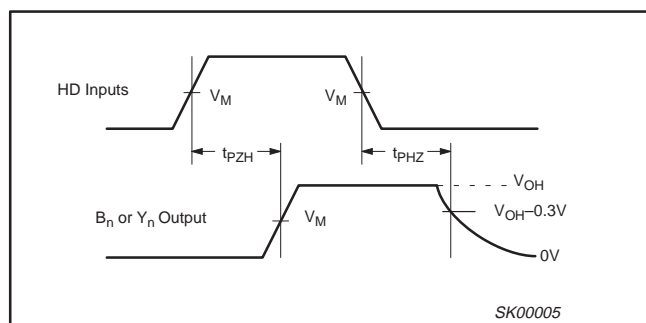
AC WAVEFORMS

For all waveforms, $V_M = 1.5\text{V}$.

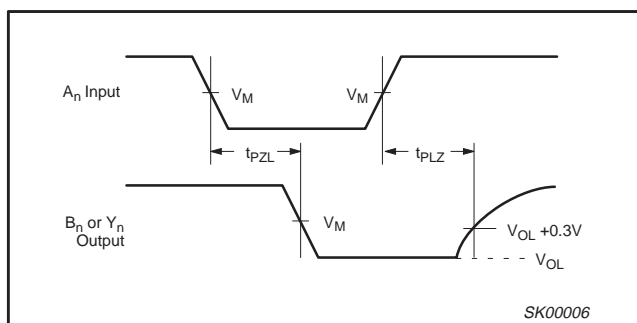
Waveform 1. Propagation Delay for Bn to A1-A4



Waveform 2. Propagation Delay for An to Bn or Yn Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output enable Time to Low Level and Output disable Time from Low Level

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TEST CIRCUITS AND WAVEFORM

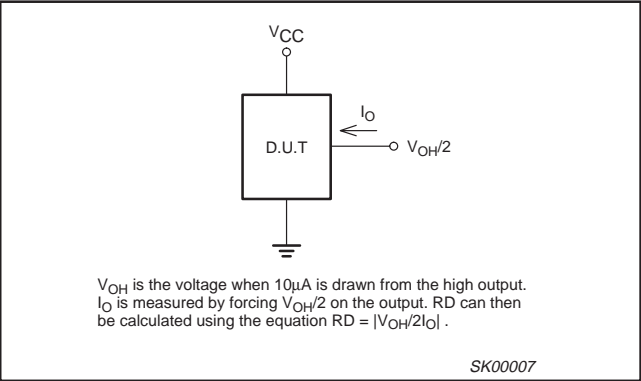


Figure 1. Output Impedance R_D

Test Circuit for B_n or Y_n Outputs

SWITCH POSITION B_n or Y_n Outputs	
TEST	SWITCH
t_{PLH}	GND
t_{PHL}	V_{CC}
t_{PZH}	GND
t_{PHZ}	GND
t_{PZL}	V_{CC}
t_{PLZ}	V_{CC}

Test Circuit for A_n Outputs

Input Pulse Definition

$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_r	t_f
74HCT	3.0V	1MHz	500ns	3ns	3ns

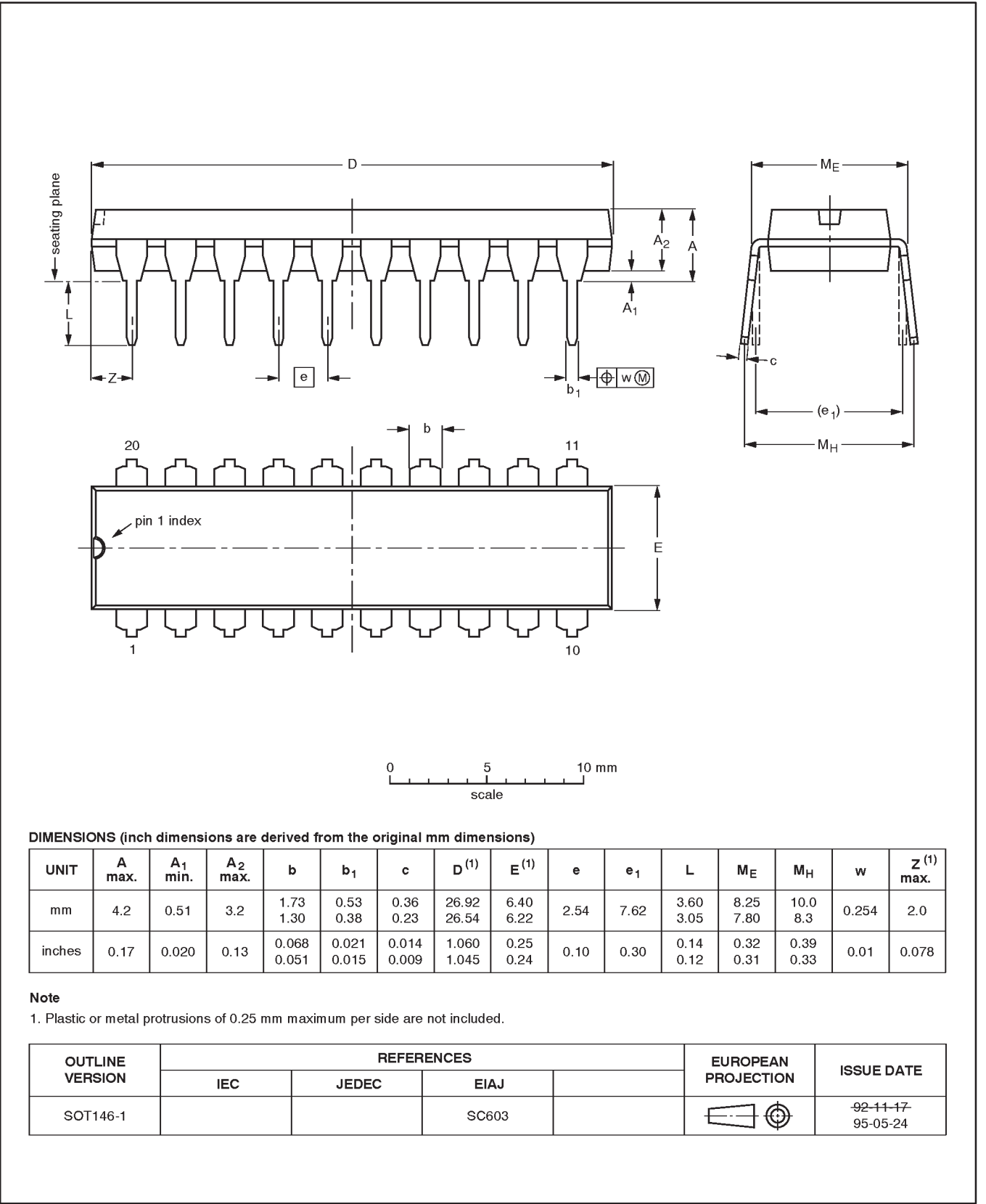
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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

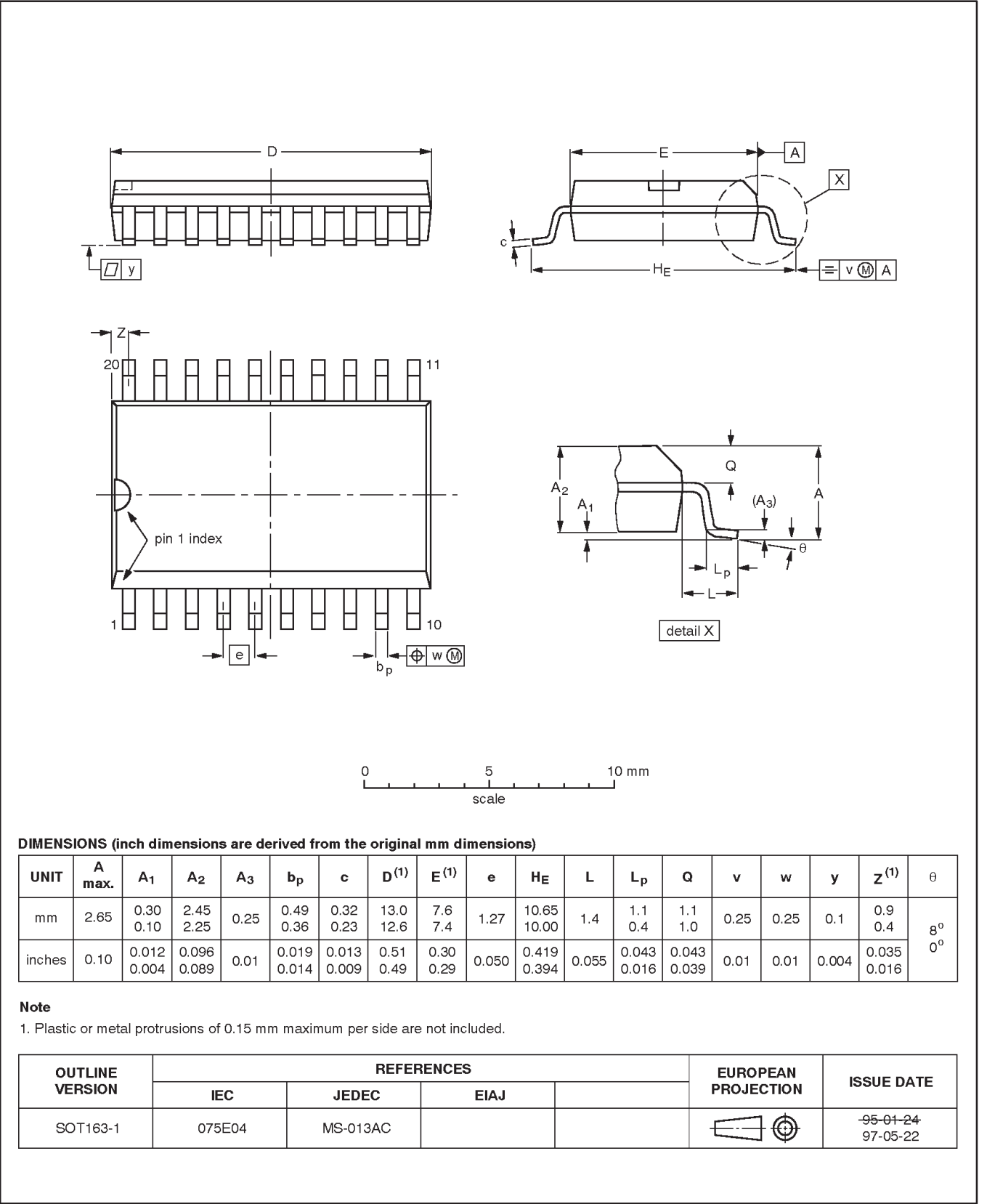


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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

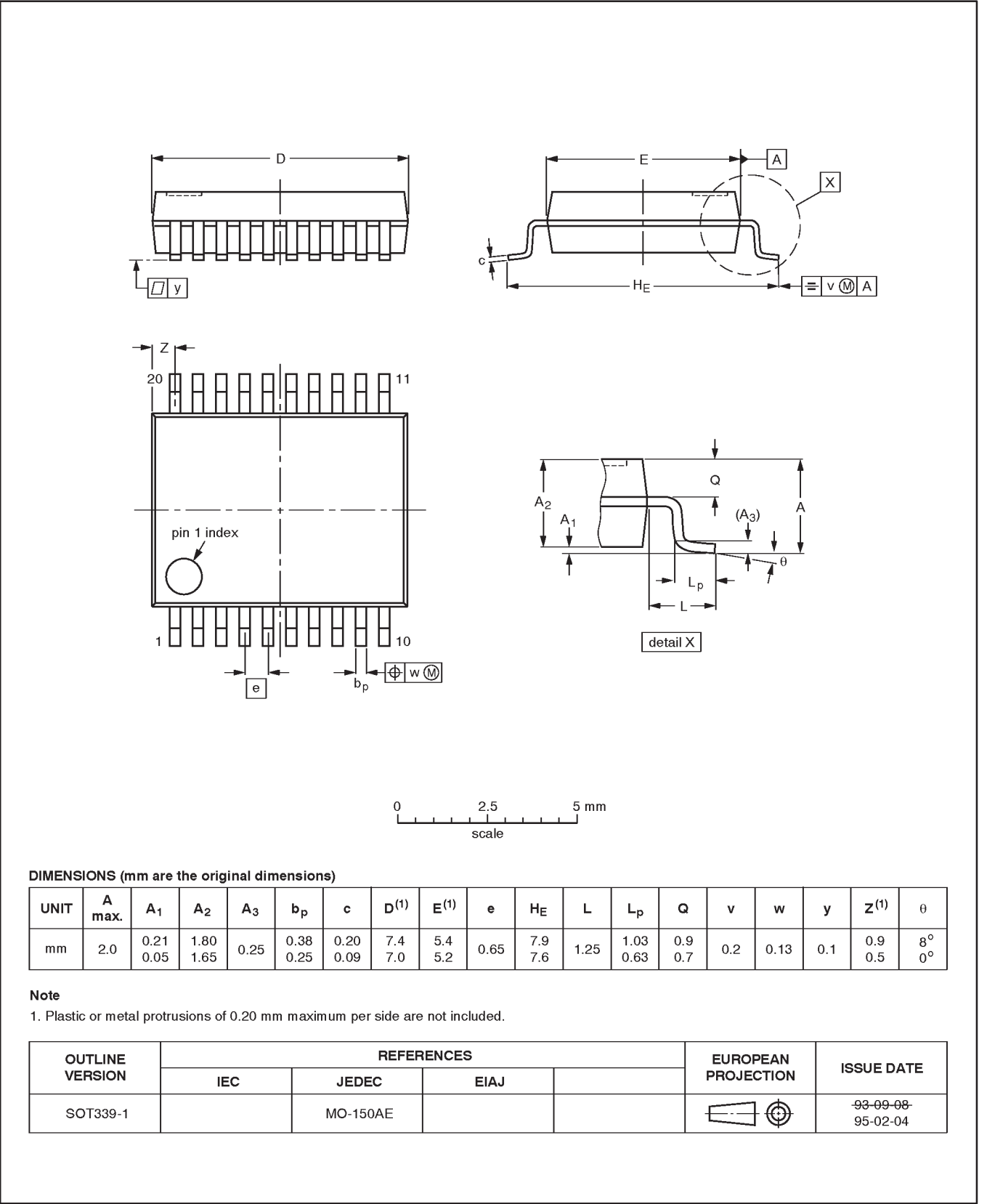


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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

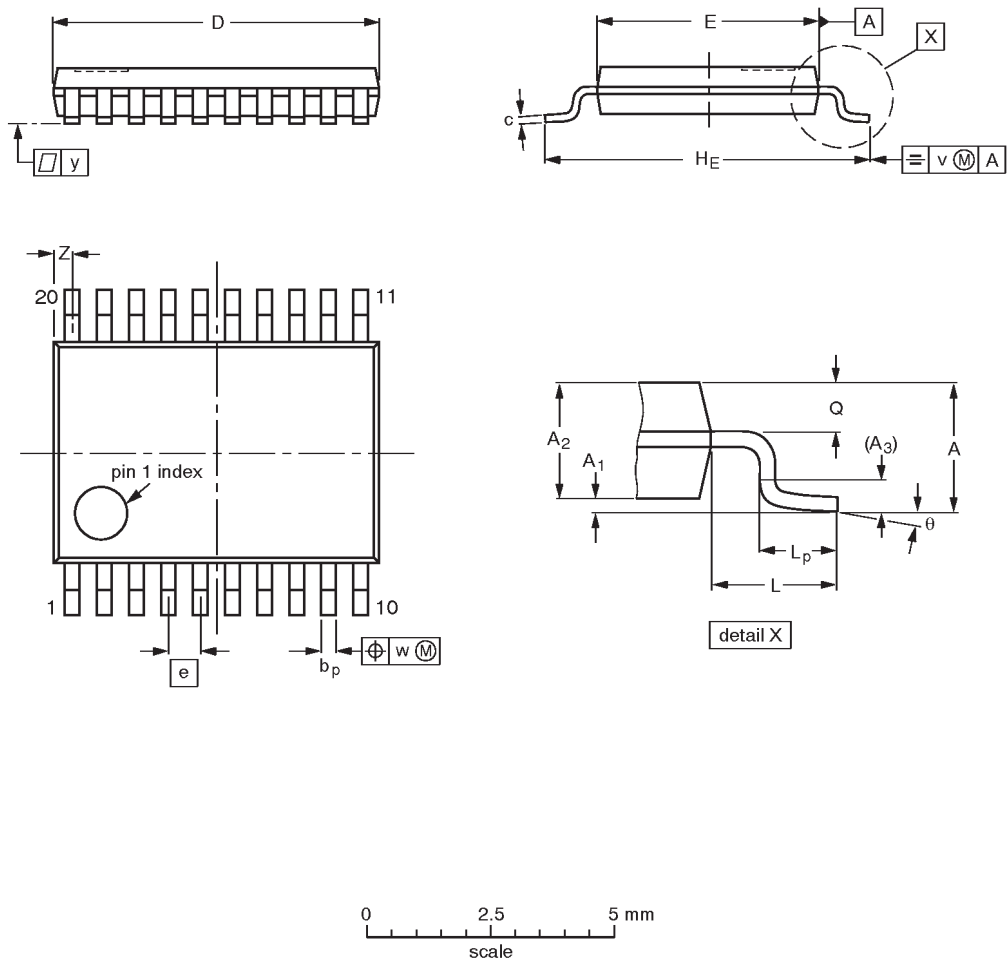


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

- Notes
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 - 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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