

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT73

Dual JK flip-flop with reset;
negative-edge trigger

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT73

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT73 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT73 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock (\overline{nCP}) and reset (\overline{nR}) inputs; also complementary Q and \overline{Q} outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset (\overline{nR}) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the \overline{Q} output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|--|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay | $C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$ | | | |
| | \overline{nCP} to nQ | | 16 | 15 | ns |
| | \overline{nCP} to \overline{nQ} | | 16 | 18 | ns |
| | \overline{nR} to nQ, \overline{nQ} | | 15 | 15 | ns |
| f_{max} | maximum clock frequency | | 77 | 79 | MHz |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per flip-flop | notes 1 and 2 | 30 | 30 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

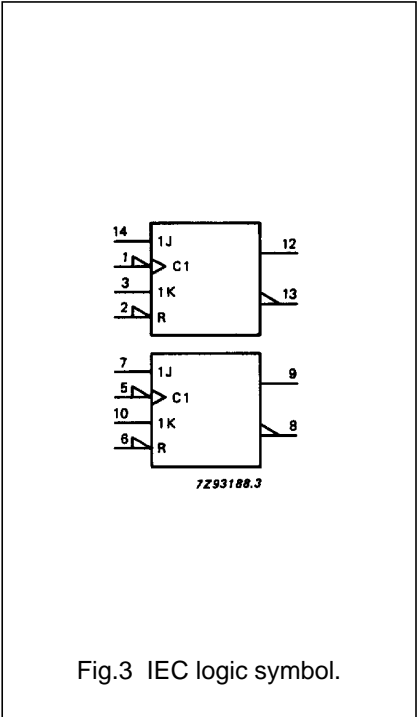
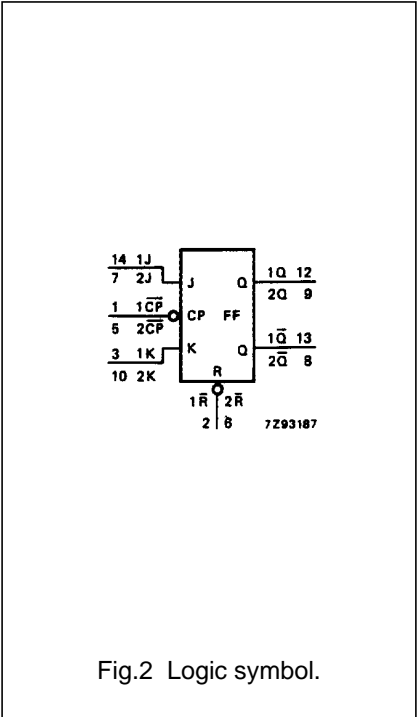
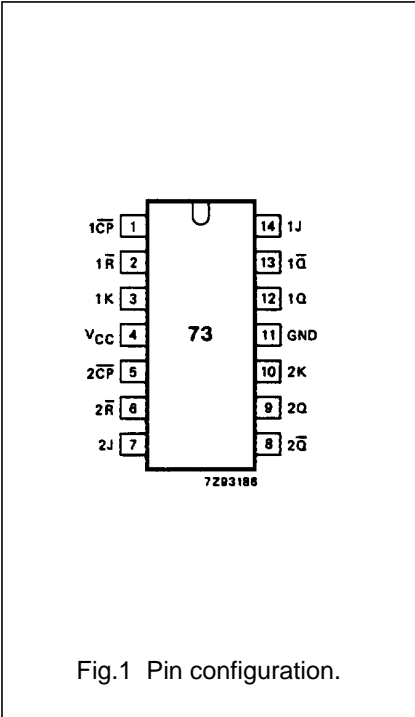
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Dual JK flip-flop with reset; negative-edge trigger

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------|----------------------------------|---|
| 1, 5 | $\overline{1CP}, \overline{2CP}$ | clock input (HIGH-to-LOW, edge-triggered) |
| 2, 6 | $\overline{1R}, \overline{2R}$ | asynchronous reset inputs (active LOW) |
| 4 | V_{CC} | positive supply voltage |
| 11 | GND | ground (0 V) |
| 12, 9 | 1Q, 2Q | true flip-flop outputs |
| 13, 8 | $\overline{1Q}, \overline{2Q}$ | complement flip-flop outputs |
| 14, 7, 3, 10 | 1J, 2J, 1K, 2K | synchronous inputs; flip-flops 1 and 2 |



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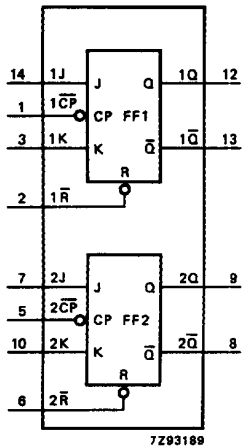


Fig.4 Functional diagram.

FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|--------------------|--------|-----|---|---|---------|---|
| | nR | nCP | J | K | Q | Q |
| asynchronous reset | L | X | X | X | L | H |
| toggle | H | ↓ | h | h | q | q |
| load "0" (reset) | H | ↓ | l | h | L | H |
| load "1" (set) | H | ↓ | h | l | H | L |
| hold "no change" | H | ↓ | l | l | q | q |

Notes

- 1. H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
- q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
- X = don't care
- ↓ = HIGH-to-LOW CP transition

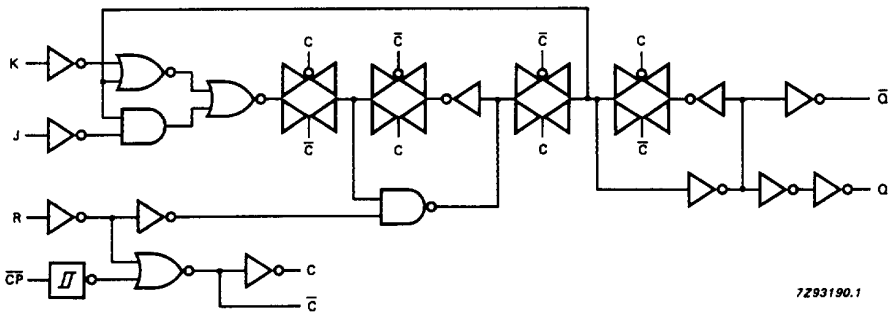


Fig.5 Logic diagram (one flip-flop).

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|-------------------------------------|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay nCP to nQ | | 52 19 15 | 160 32 27 | | 200 40 34 | | 240 48 41 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay nCP to nQ̄ | | 52 19 15 | 160 32 27 | | 200 40 34 | | 240 48 41 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay nR̄ to nQ, nQ̄ | | 50 18 14 | 145 29 25 | | 180 36 31 | | 220 44 38 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _W | clock pulse width HIGH or LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _W | reset pulse width HIGH or LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{rem} | removal time nR̄ to nCP | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{su} | set-up time nJ, nK to nCP̄ | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _h | hold time nJ, nK to nCP̄ | 3 3 3 | −8 −3 −2 | | 3 3 3 | | 3 3 3 | | ns | 2.0 4.5 6.0 | Fig.6 |
| f _{max} | maximum clock pulse frequency | 6.0 30 35 | 23 70 83 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig.6 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|------------------------|-----------------------|
| nK | 0.60 |
| n \overline{R} | 0.65 |
| n \overline{CP} , nJ | 1.00 |

AC CHARACTERISTICS FOR 74HCT

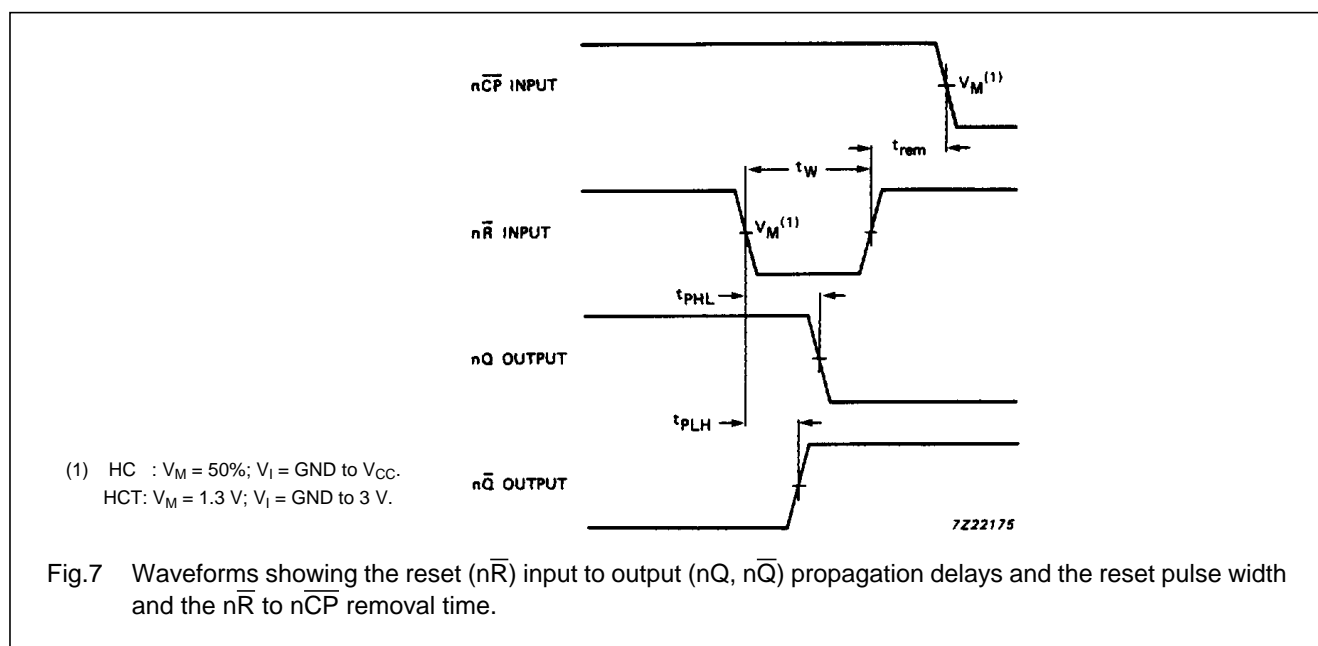
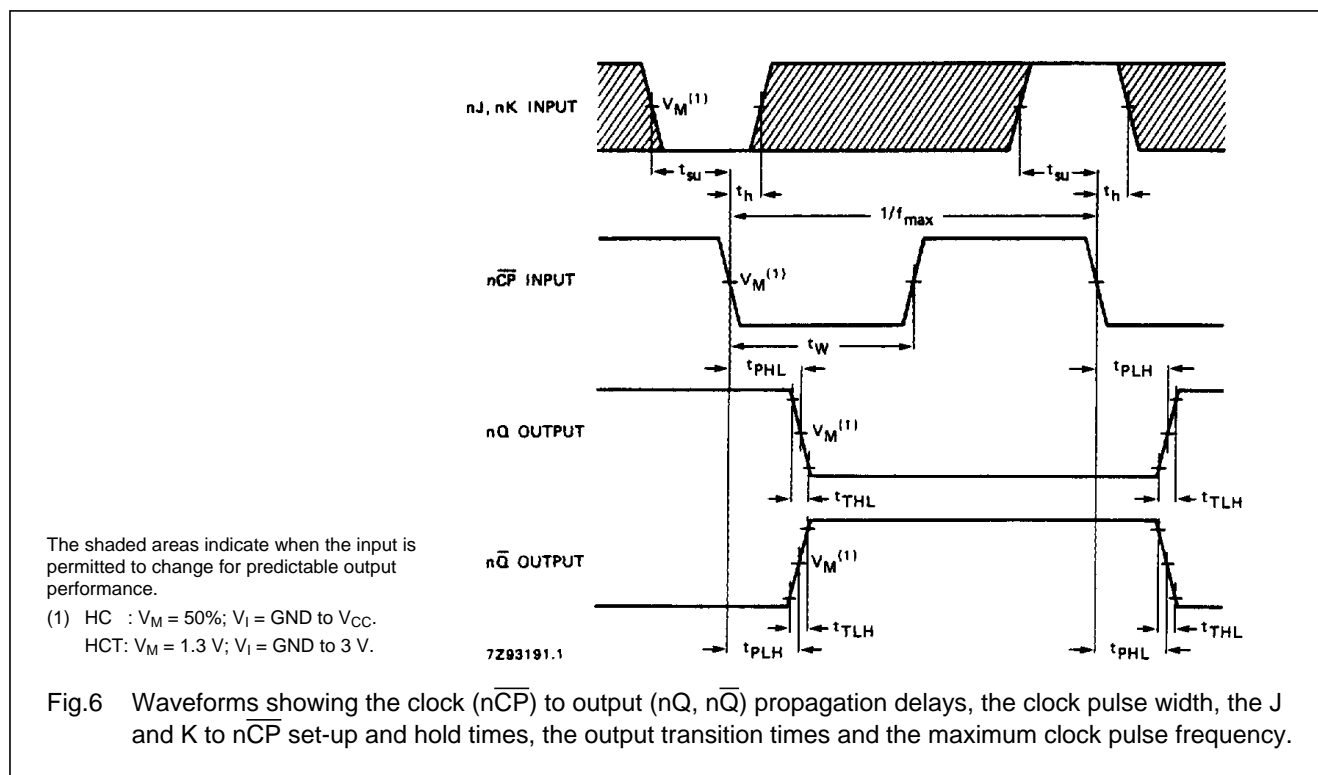
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|-------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
| | | 74 HCT | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay nCP to nQ | | 18 | 38 | | 48 | | 57 | ns | 4.5 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay nCP to nQ̄ | | 21 | 36 | | 45 | | 54 | ns | 4.5 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay nR̄ to nQ, nQ̄ | | 20 | 34 | | 43 | | 51 | ns | 4.5 | Fig.7 |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 |
| t _W | clock pulse width HIGH or LOW | 16 | 8 | | 20 | | 24 | | ns | 4.5 | Fig.6 |
| t _W | reset pulse width HIGH or LOW | 18 | 9 | | 23 | | 27 | | ns | 4.5 | Fig.7 |
| t _{rem} | removal time nR̄ to nCP̄ | 14 | 8 | | 18 | | 21 | | ns | 4.5 | Fig.7 |
| t _{su} | set-up time nJ, nK to nCP̄ | 12 | 6 | | 15 | | 18 | | ns | 4.5 | Fig.6 |
| t _h | hold time nJ, nK to nCP̄ | 3 | −2 | | 3 | | 3 | | ns | 4.5 | Fig.6 |
| f _{max} | maximum clock pulse frequency | 30 | 72 | | 24 | | 20 | | MHz | 4.5 | Fig.6 |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".