

DATA SHEET

74LVC841A

10-bit transparent latch with 5-volt
tolerant inputs/outputs (3-State)

Product specification
IC24 Data Handbook

1998 Jun 17

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC standard no. 8-1 A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC841A is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-State operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment. The 74LVC841A is a 10-bit transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all internal latches. The 74LVC841A consists of ten transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the ten latches are available at the outputs.

When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n ; LE to Q_n	$C_L = 50$ pF; $V_{CC} = 3.3$ V	4.5 5.0	ns
C_i	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	$V_i = \text{GND to } V_{CC}^1$	22	pF

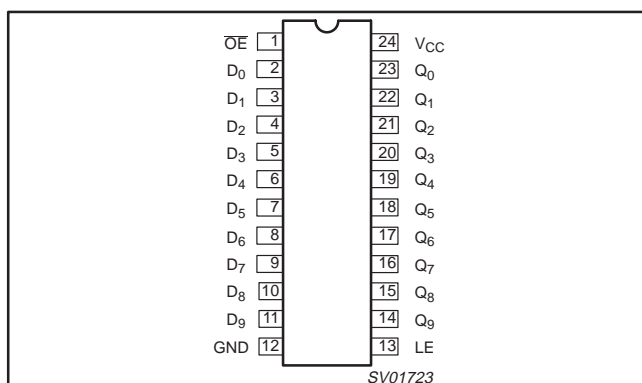
NOTE:

- 1 C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	-40°C to $+125^\circ\text{C}$	74LVC841A D	74LVC841A D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to $+125^\circ\text{C}$	74LVC841A DB	74LVC841A DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to $+125^\circ\text{C}$	74LVC841A PW	74LVC841APW DH	SOT355-1

PIN CONFIGURATION



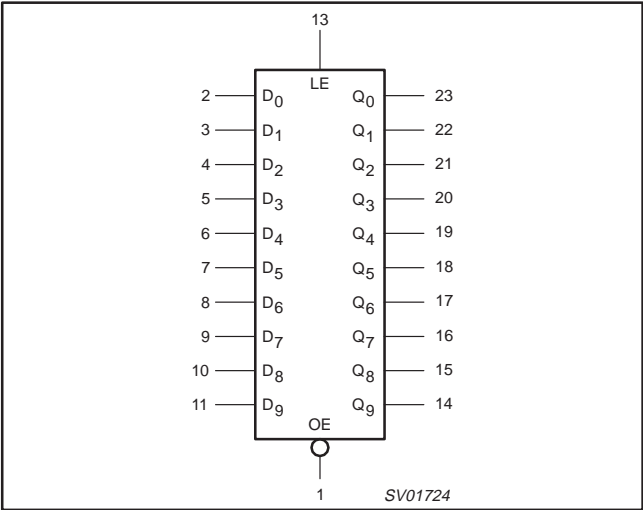
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	\overline{OE}	Output enable input (active Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D_0 to D_9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q_0 to Q_9	3-state latch outputs
12	GND	Ground (0 V)
13	LE	Latch enable input (active HIGH)
24	V_{CC}	Positive supply voltage

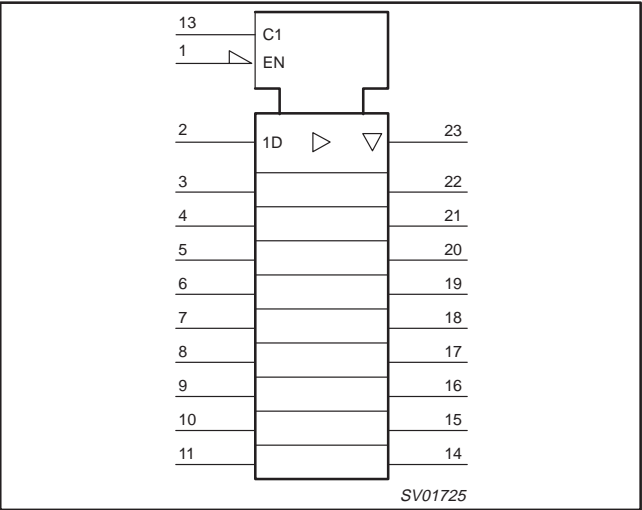
10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

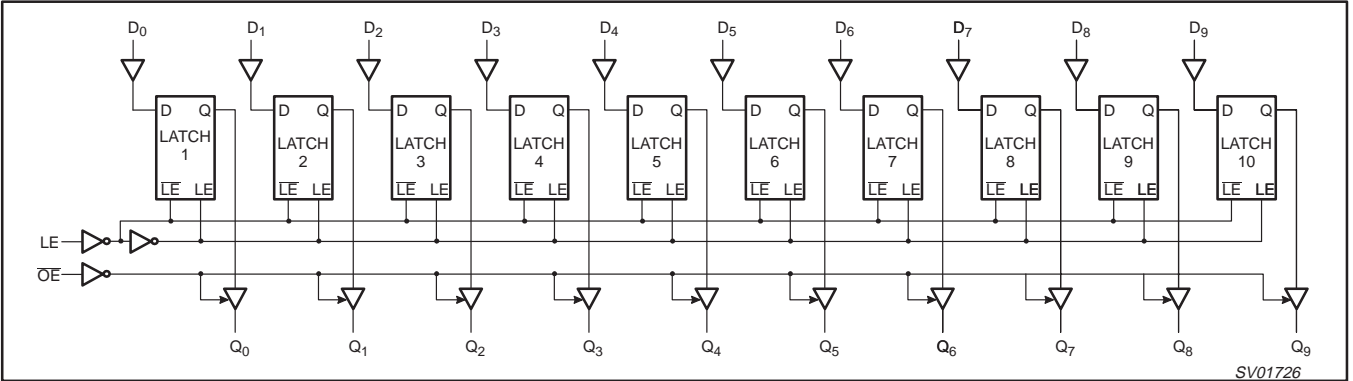
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE for register A_n or B_n

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	\overline{OE}	LE	D_n		Q_0 TO Q_9
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	↓ ↓	l h	L H	L H
latch register and disable outputs	H H	X X	l h	L H	Z Z
Hold	L	L	X	NC	NC

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state
NC = no change

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	Note 2	-0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package			
	– plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 1.0			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		± 0.1	± 5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	± 5	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA

NOTE:

1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = -40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V		
			MIN	TYP ¹	MAX	MIN	MAX	
t _{PHL} /t _{PLH}	Propagation delay D _n to Q _n	Figures 1, 5	1.5	4.5	6.7	1.5	7.5	ns
t _{PHL} /t _{PLH}	Propagation delay LE to Q _n	Figures 2, 5	1.5	4.9	7.6	1.5	8.6	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Q _n	Figures 3, 5	1.5	5.4	7.9	1.5	8.9	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Q _n	Figures 3, 5	1.5	3.8	5.9	1.5	6.9	ns
t _w	LE pulse width, HIGH	Figure 4	2.0	0.7	—	2.0		ns
t _{su}	Set-up time D _n to LE	Figure 4	2.0	0.5	—	2.0		ns
t _h	Hold time D _n to LE	Figure 4	1.0	−0.5	—	1.0		ns

NOTE:

1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

AC WAVEFORMS

 $V_M = 1.5 \text{ V at } V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \text{ V} \times V_{CC} \text{ at } V_{CC} < 2.7 \text{ V}$
 $V_M = 1.5 \text{ V at } V_{CC} = 3.0 \text{ V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

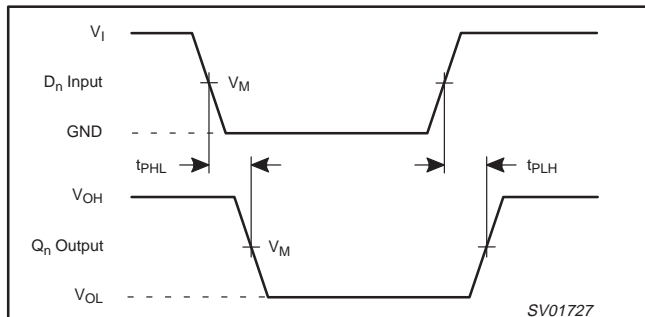
 $V_X = V_{OL} + 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \times V_{CC} \text{ at } V_{CC} < 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \times V_{CC} \text{ at } V_{CC} < 2.7 \text{ V}$


Figure 1. Input (D_n) to output (Q_n) propagation delays.

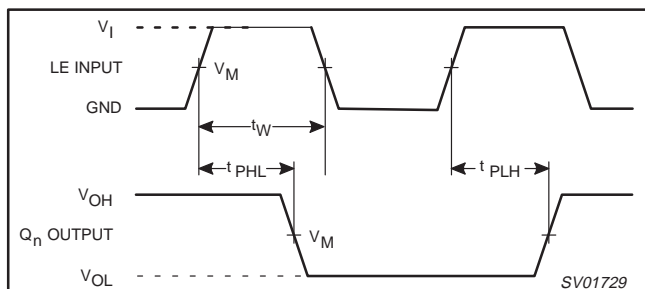


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

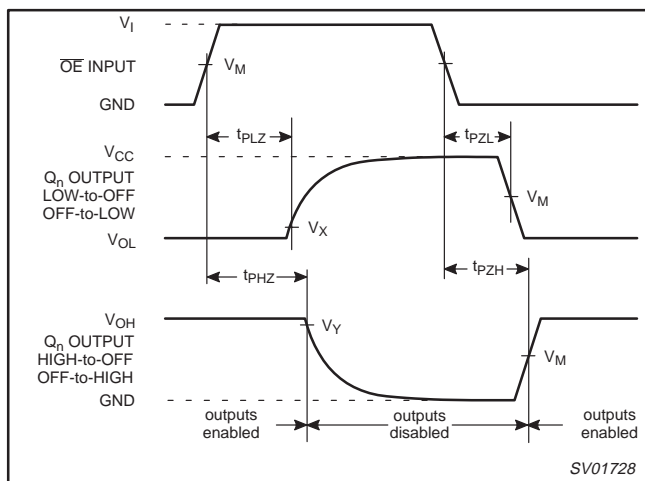


Figure 3. 3-State enable and disable times.

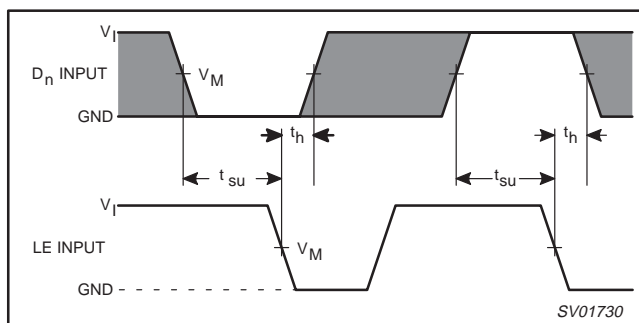


Figure 4. Data set-up and hold times for the D_n input to LE input.

Note to Figure 4: The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT

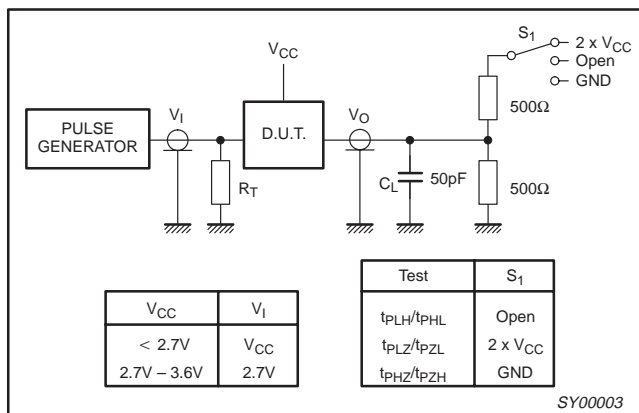


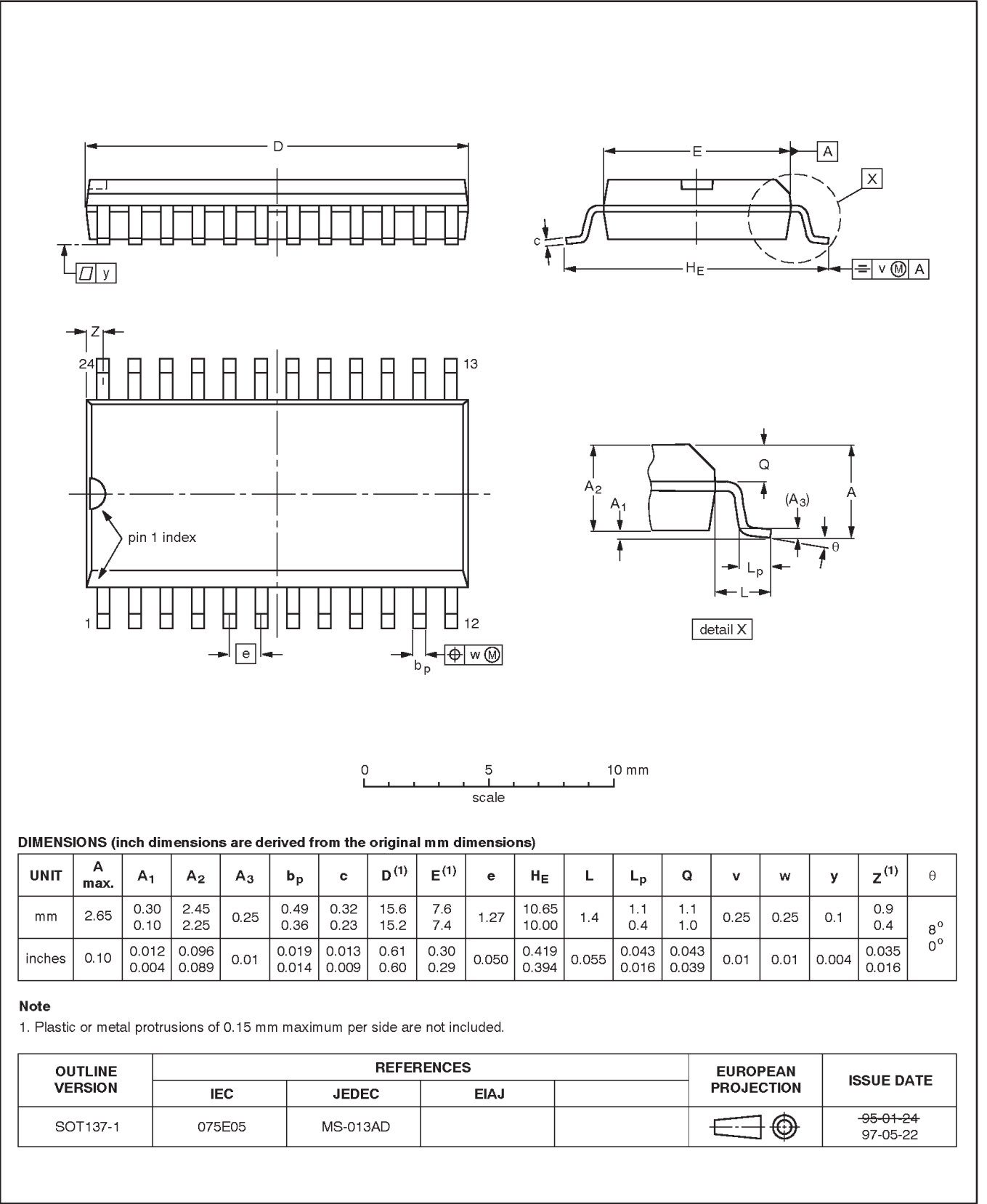
Figure 5. Load circuitry for switching times.

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

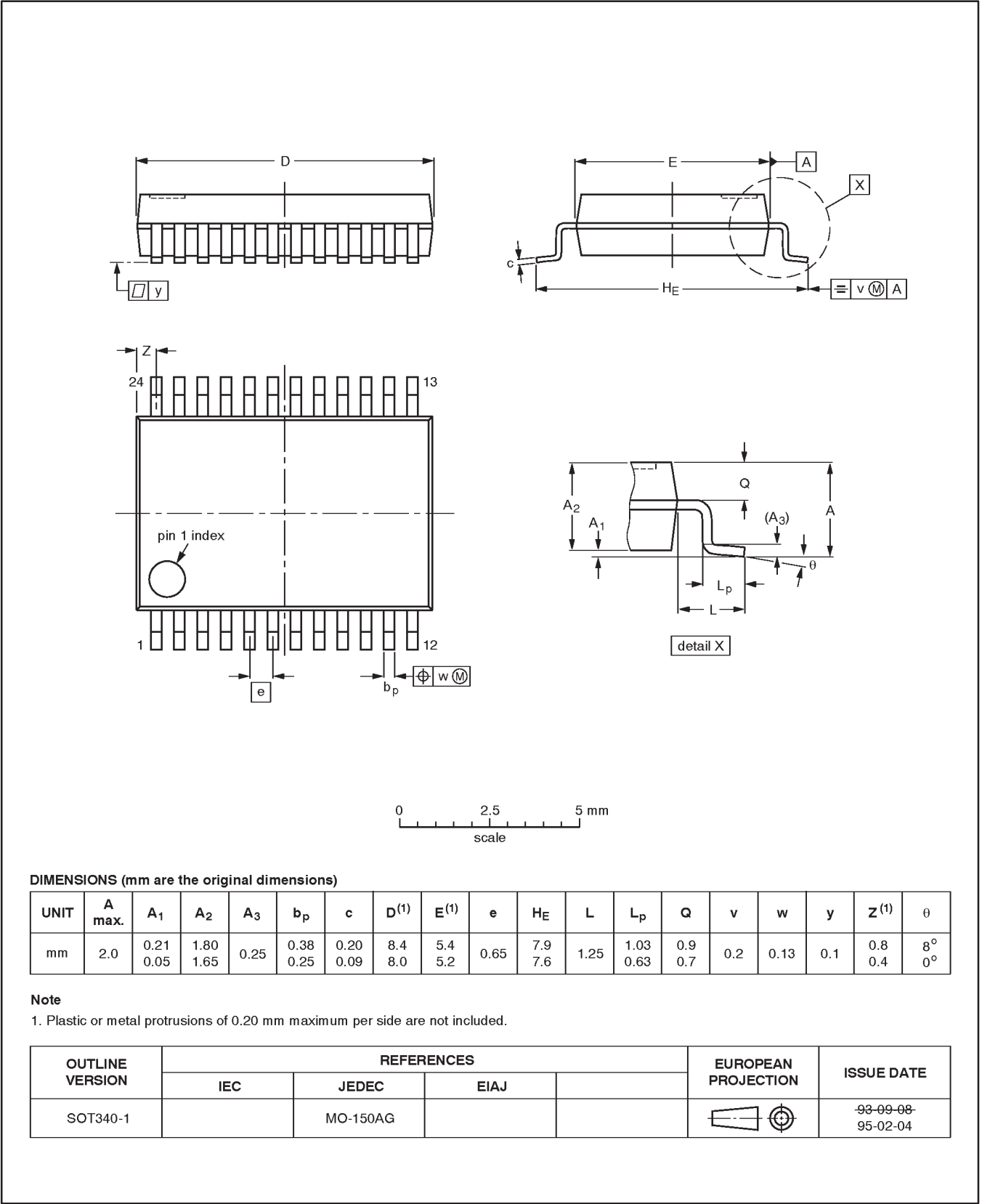


10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

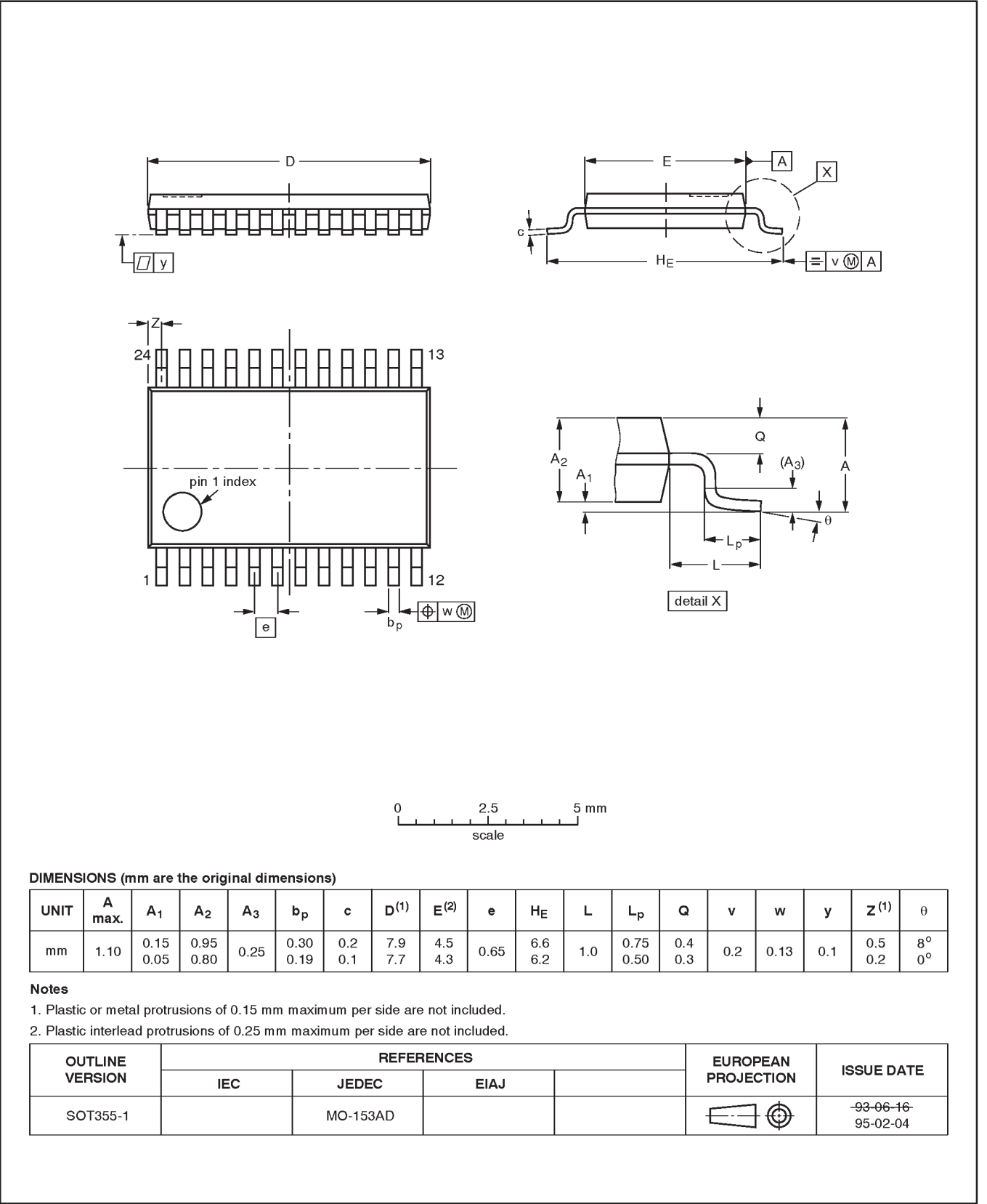


10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998
All rights reserved. Printed in U.S.A.

print code

Date of release: 06-98

Document order number:

9397-750-04522

Let's make things better.