

BTA208X-1000C

Three quadrant triacs high commutation

Rev. 01 — 4 October 2005

Product data sheet

1. Product profile

1.1 General description

Passivated high voltage, high commutation triac in a full pack, plastic package. This triac is intended for use in motor control circuits where high blocking voltage, high static and dynamic dV/dt as well as high dI/dt can occur. This device will commute the full rated RMS current at the maximum rated junction temperature, without the aid of a snubber.

1.2 Features

- False trigger immunity
- 1000 V V_{DRM} guaranteed
- Isolated package

1.3 Applications

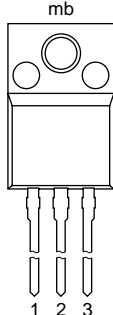

- Motor control
- Reversible induction motors

1.4 Quick reference data

- $I_{TSM} \leq 65$ A
- $V_{DRM} \leq 1000$ V
- $I_{T(RMS)} \leq 8$ A
- $I_{GT} \leq 35$ mA

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	main terminal 1 (T1)		 sym051
2	main terminal 2 (T2)		
3	gate (G)		
mb	mounting base; isolated		

SOT186A (3-lead TO-220F)

PHILIPS

3. Ordering information

Table 2: Ordering information

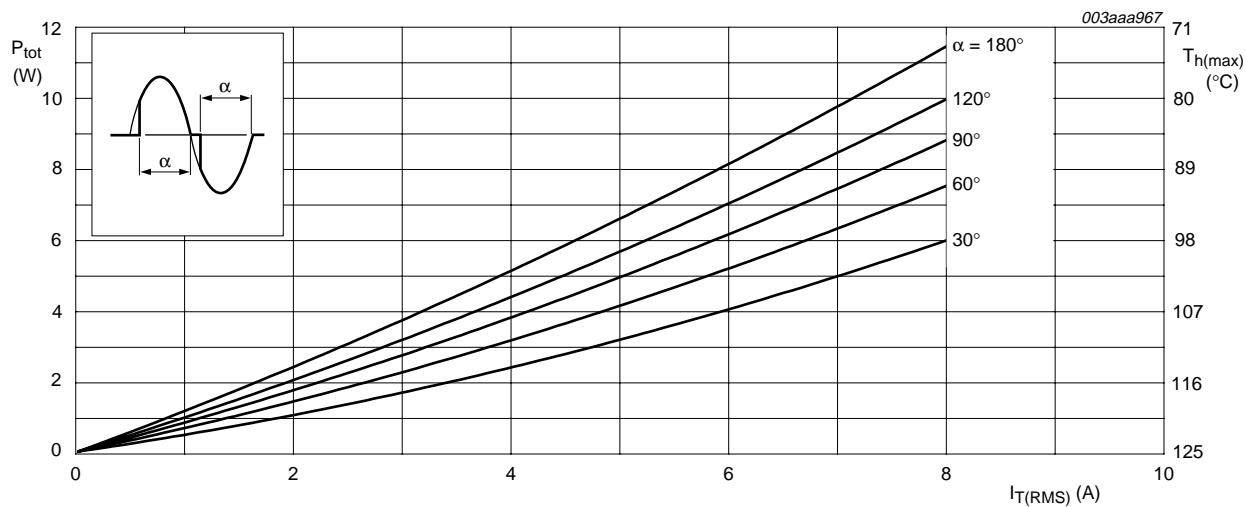
Type number	Package		
	Name	Description	Version
BTA208X-1000C	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 'full pack'	SOT186A

4. Limiting values

Table 3: Limiting values

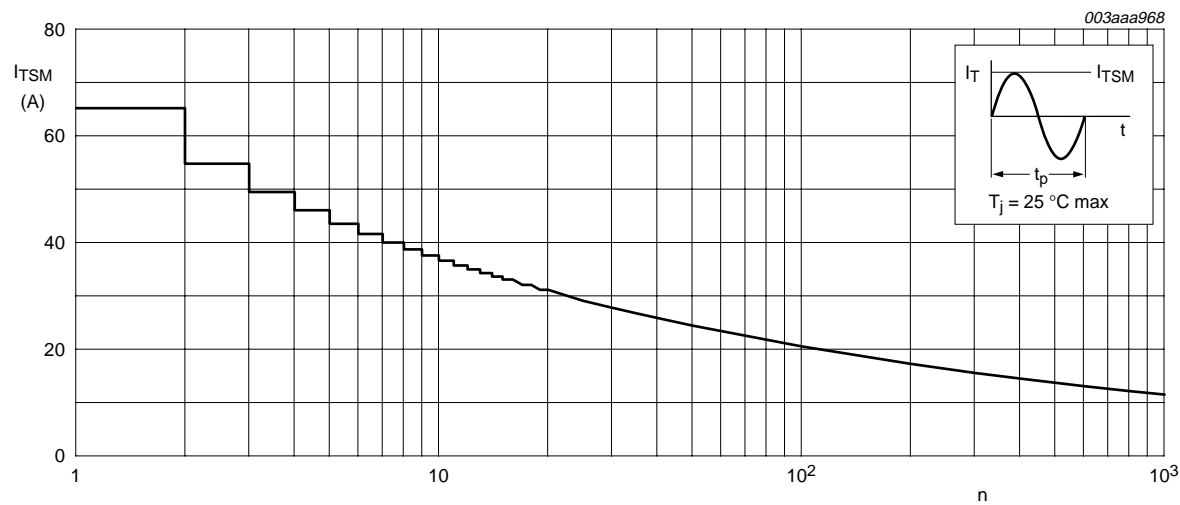
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	1000	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_h \leq 73^\circ\text{C}$; see Figure 4 and 5	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge; see Figure 2 and 3			
		$t = 20\text{ ms}$	-	65	A
		$t = 16.7\text{ ms}$	-	71	A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	21	A^2s
di_T/dt	rate of rise of on-state current	$I_{\text{TM}} = 12\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	+150	$^\circ\text{C}$
T_j	junction temperature		-	125	$^\circ\text{C}$



α = conduction angle

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



$f = 50\text{ Hz}$

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

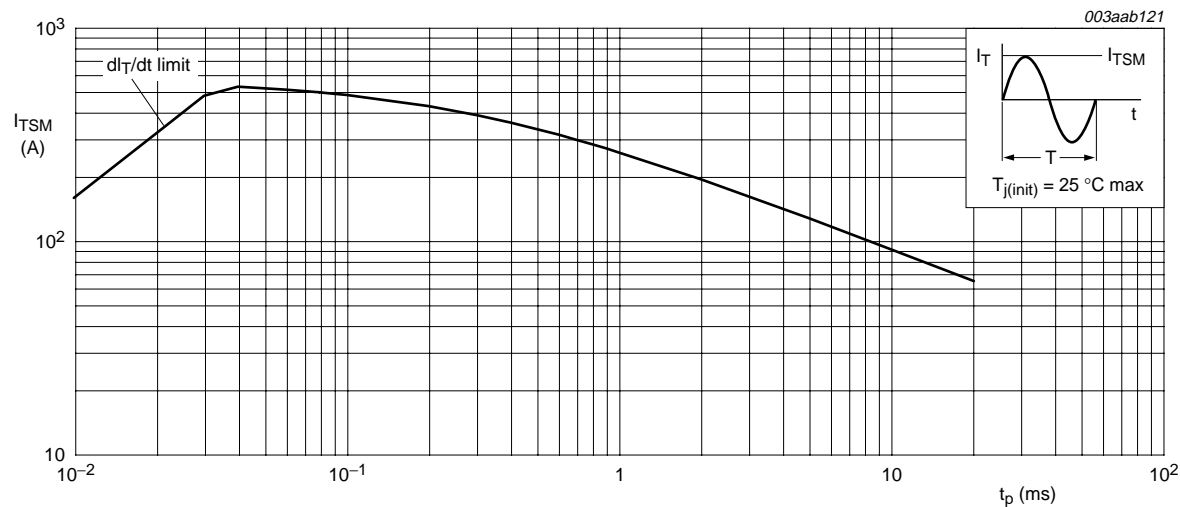


Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

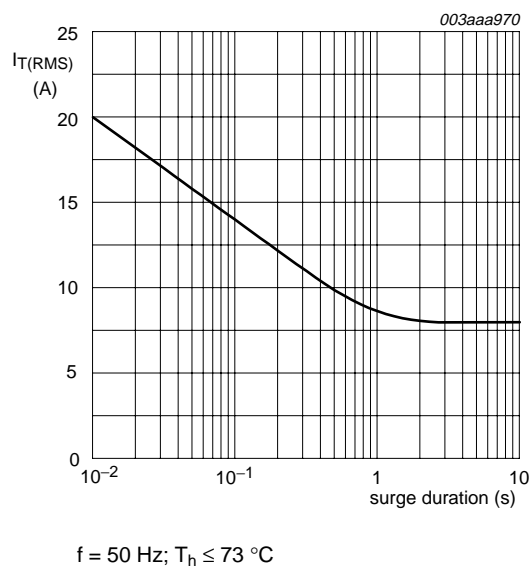


Fig 4. RMS on-state current as a function of surge duration; maximum values

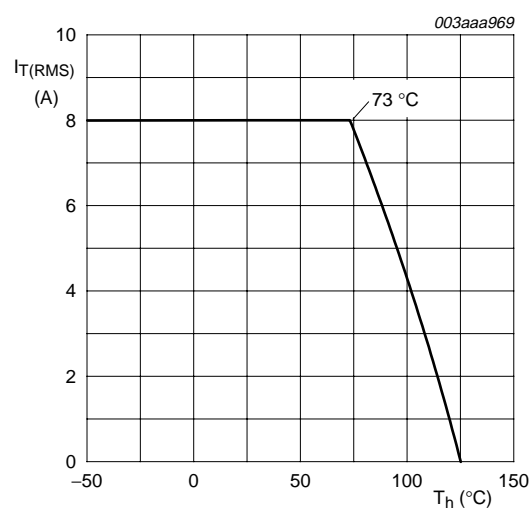


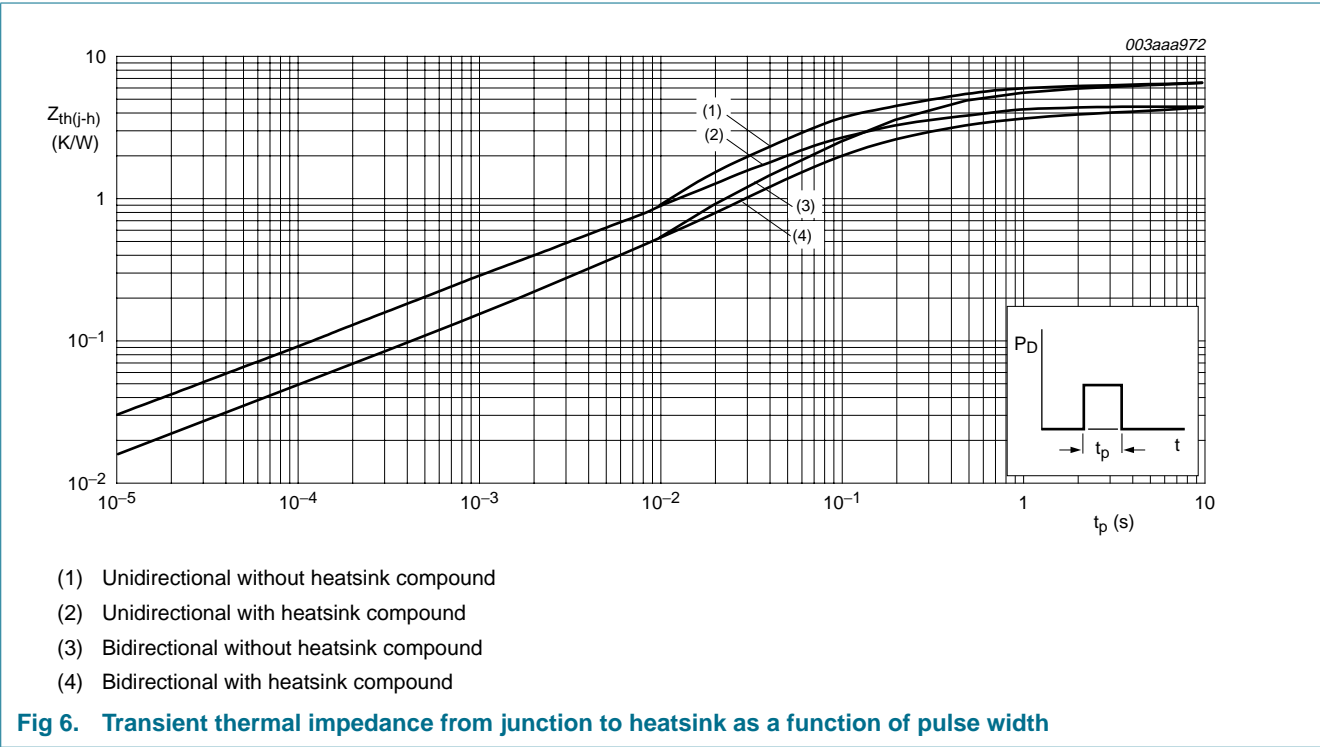
Fig 5. RMS on-state current as a function of heatsink temperature; maximum values

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	see Figure 6	[1] -	-	4.5	K/W
		see Figure 6	[2] -	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W

- [1] Full or half cycle; with heatsink compound.
[2] Full or half cycle; without heatsink compound.



6. Isolation characteristics

Table 5: Isolation limiting values and characteristics

$T_h = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(rms)}$	RMS isolation voltage	$f = 50\text{ Hz to }60\text{ Hz}$; sinusoidal waveform; $RH \leq 65\text{ \%}$; clean and dust free; from all three terminals to external heatsink	-	-	2500	V
C_{isol}	isolation capacitance	$f = 1\text{ MHz}$; from pin 2 to external heatsink	-	10	-	pF

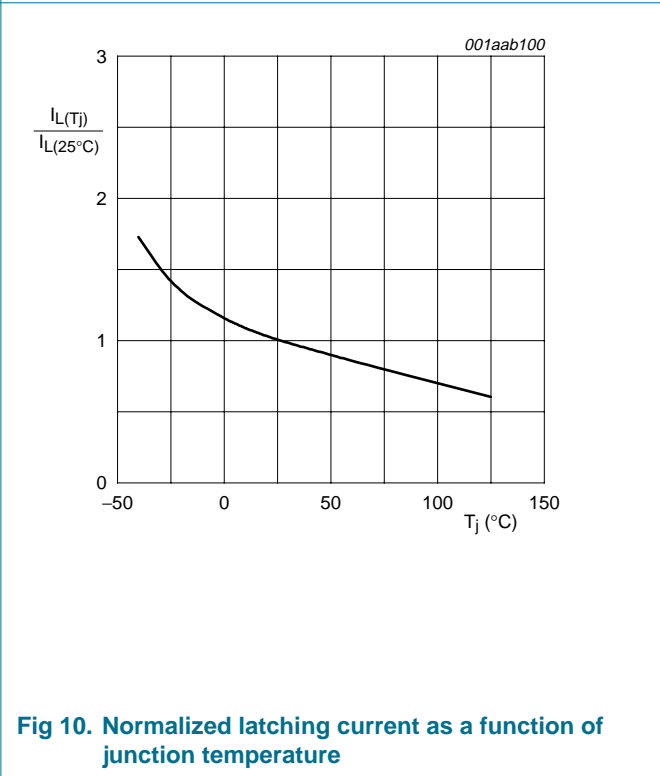
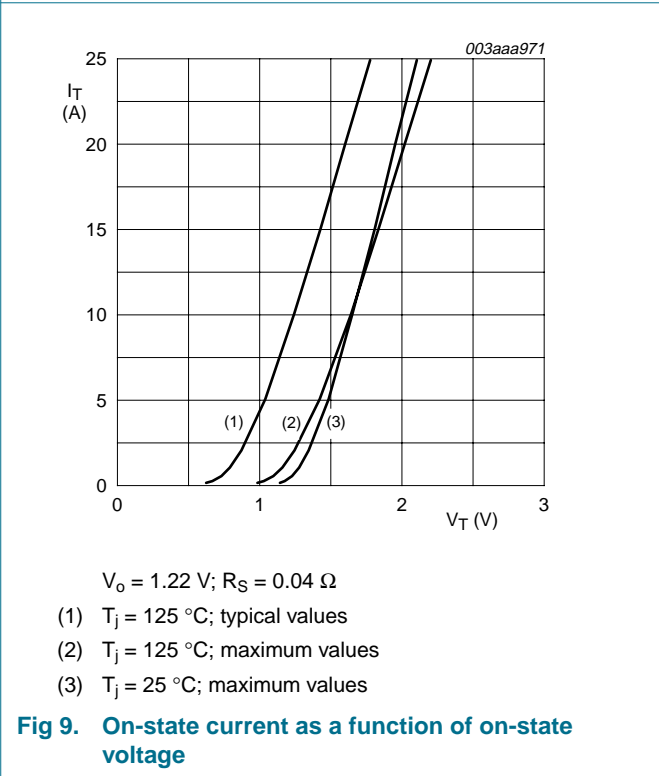
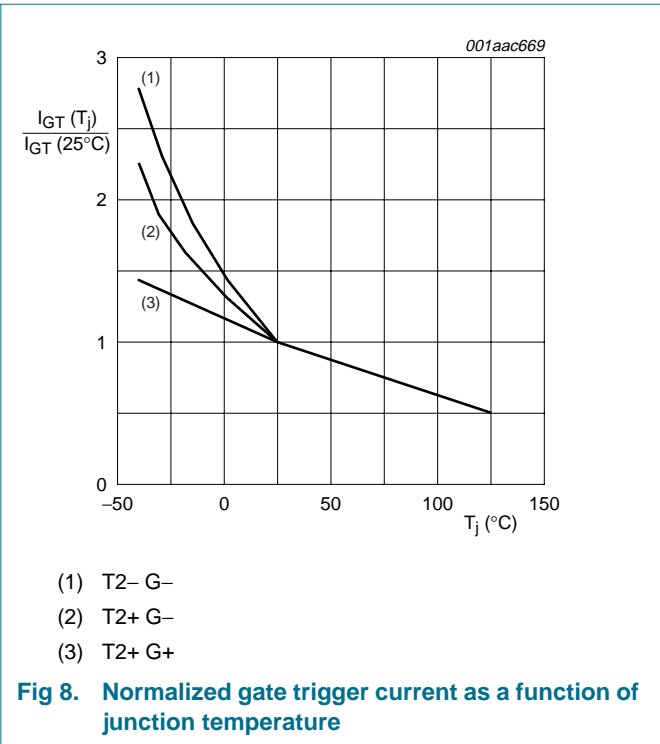
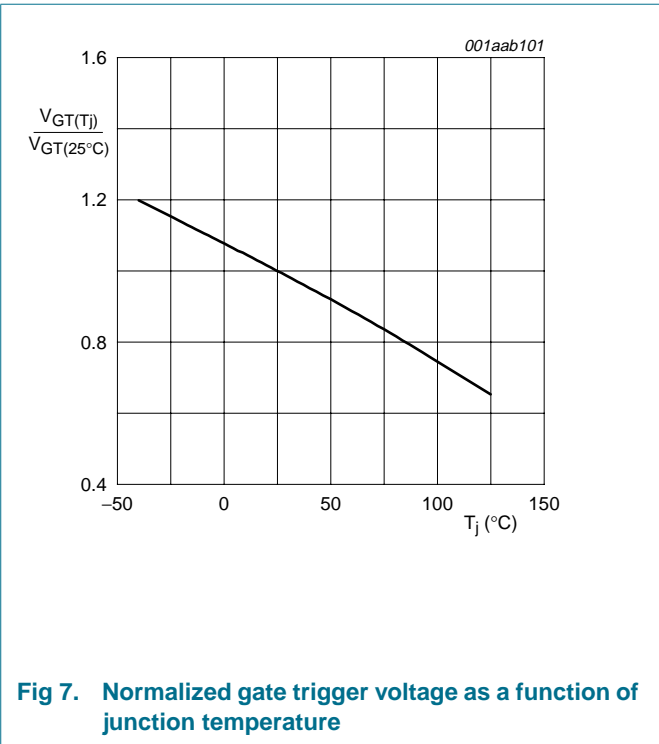
7. Characteristics

Table 6: Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 8 ^[1]				
		T2+ G+	2	6	35	mA
		T2+ G–	2	13	35	mA
		T2– G–	2	23	35	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$; see Figure 10				
		T2+ G+	-	25	50	mA
		T2+ G–	-	48	75	mA
		T2– G–	-	30	50	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$; see Figure 11	-	20	50	mA
V_T	on-state voltage	$I_T = 10\text{ A}$; see Figure 9	-	1.3	1.65	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 7	-	0.7	1.5	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^{\circ}\text{C}$	0.25	0.4	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 67\text{ }\%$ $V_{DRM(max)}$; $T_j = 125\text{ }^{\circ}\text{C}$; exponential waveform; gate open circuit	1000	4000	-	V/ μs
di_{com}/dt	rate of change of commutating current	$V_{DM} = 400\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 8\text{ A}$; without snubber; gate open circuit; see Figure 12	12	32	-	A/ms
t_{gt}	gate-controlled turn-on time	$I_{TM} = 12\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 0.1\text{ A}$; $di_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs

[1] Device will not trigger in the T2– G+ quadrant.



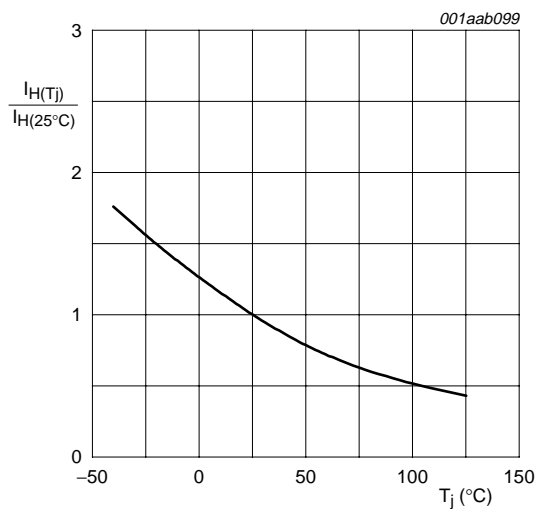


Fig 11. Normalized holding current as a function of junction temperature

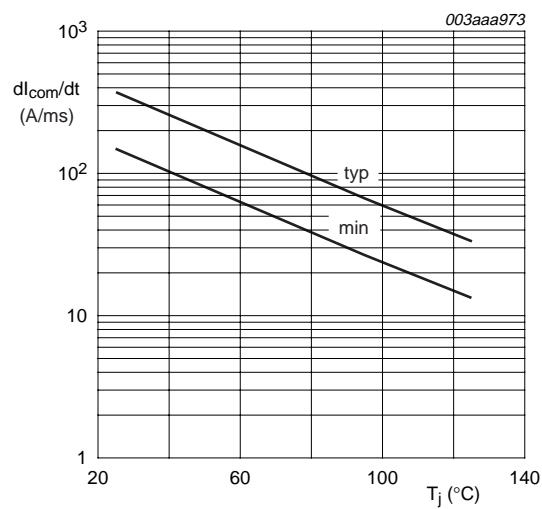
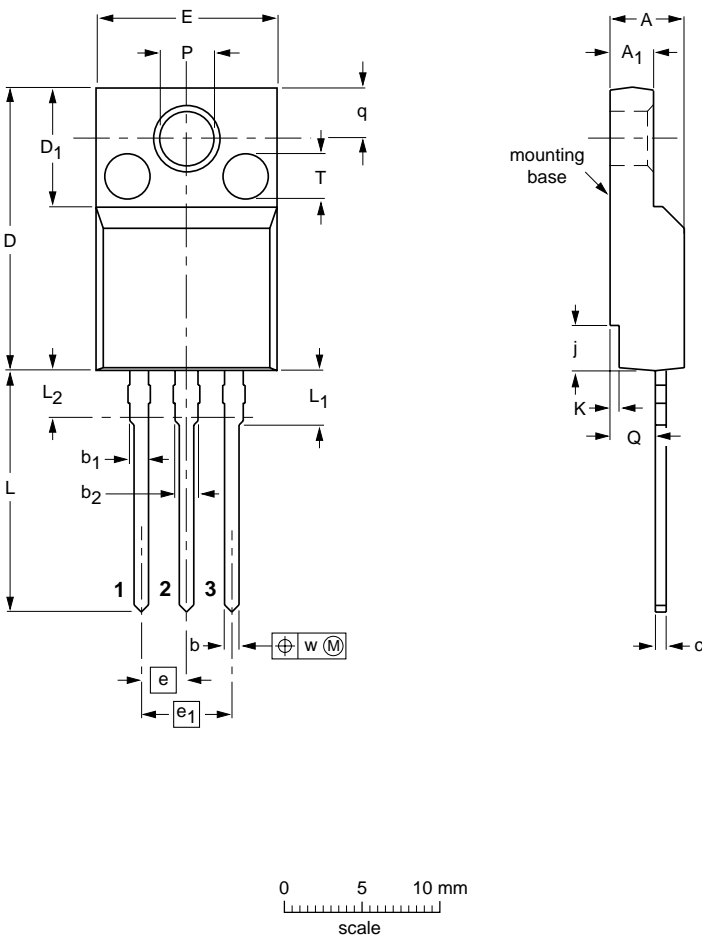


Fig 12. Rate of change of commutating current as a function of junction temperature; typical and minimum values

8. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	T ⁽²⁾	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

- Notes
- Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
 - Both recesses are $\varnothing 2.5 \times 0.8$ max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				02-03-12 02-04-09

Fig 13. Package outline SOT186A (3-lead TO-220F)



9. Revision history

Table 7: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BTA208X-1000C_1	20051004	Product data sheet	-	-	-

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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