

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40161B **MSI**

4-bit synchronous binary counter
with asynchronous reset

Product specification
File under Integrated Circuits, IC04

January 1995

4-bit synchronous binary counter with asynchronous reset

HEF40161B
MSI

DESCRIPTION

The HEF40161B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), an overriding asynchronous master reset (\overline{MR}), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable (\overline{PE}), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the \overline{MR} input) and occurs on the LOW to HIGH transition of CP. When \overline{PE} is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 regardless of the levels of CEP and CET inputs.

When \overline{PE} is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_1 to O_3 = HIGH) and when CET is HIGH. A LOW on \overline{MR} sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET and \overline{PE} must be stable only during the set-up time before the LOW to HIGH transition of CP.

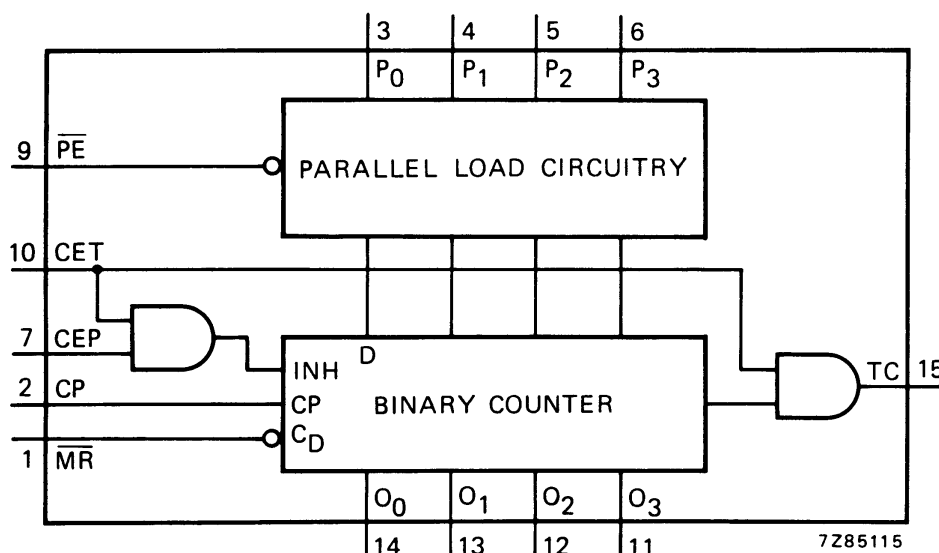


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

4-bit synchronous binary counter with
asynchronous reset

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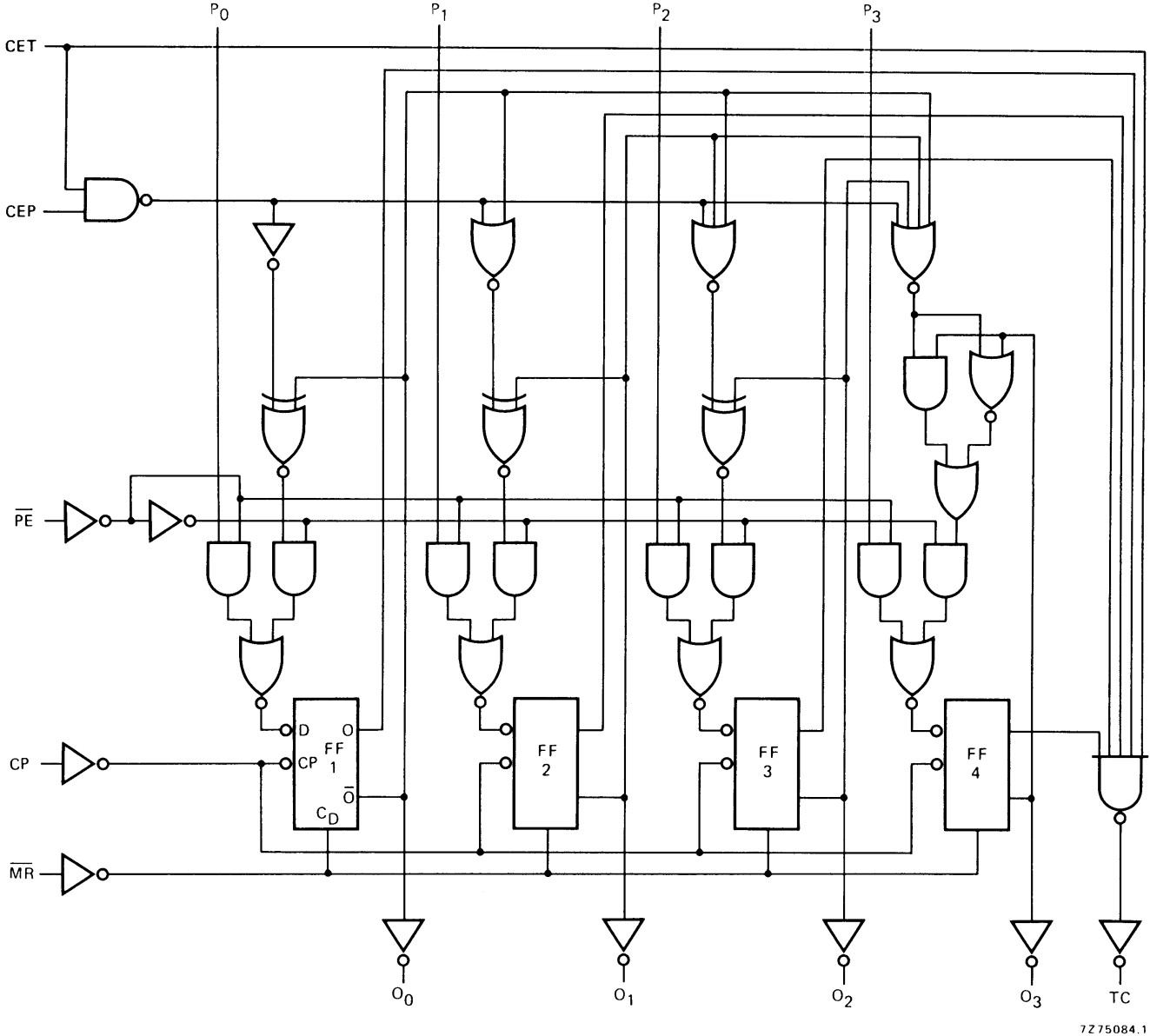
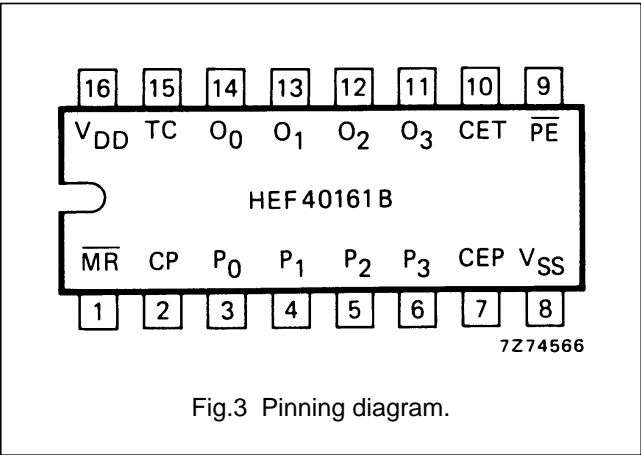


Fig.2 Logic diagram.

4-bit synchronous binary counter with asynchronous reset

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PINNING

- PE parallel enable input
- P₀ to P₃ parallel data inputs
- CEP count enable parallel input
- CET count enable trickle input
- CP clock input (LOW to HIGH, edge-triggered)
- MR master reset input (active LOW)
- O₀ to O₃ parallel outputs
- TC terminal count output

HEF40161BP(N): 16-lead DIL; plastic (SOT38-1)
HEF40161BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF40161BT(D): 16-lead SO; plastic (SOT109-1)
(): Package Designator North America

SYNCHRONOUS MODE SELECTION

| PE | CEP | CET | MODE |
|----|-----|-----|-----------|
| L | X | X | preset |
| H | L | X | no change |
| H | X | L | no change |
| H | H | H | count |

Notes

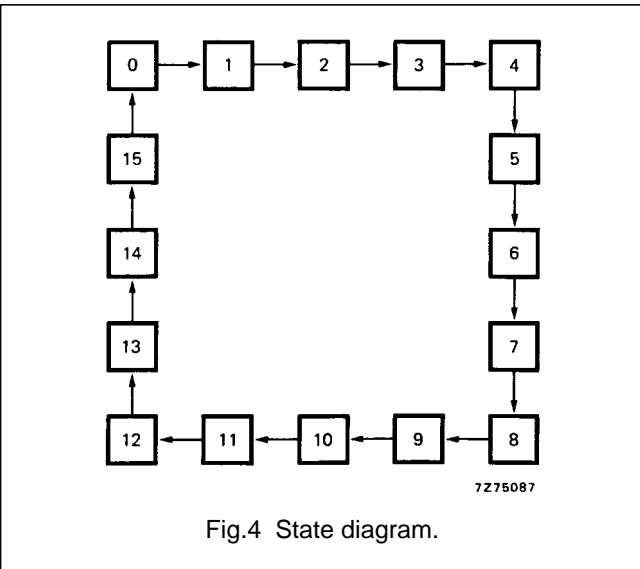
- MR = HIGH
- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

TERMINAL COUNT GENERATION

| CET | (O ₀ · O ₁ · O ₂ · O ₃) | TC |
|-----|--|----|
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

Note

- TC = CET · O₀ · O₁ · O₂ · O₃



4-bit synchronous binary counter with asynchronous reset

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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

| | V_{DD} V | TYPICAL FORMULA FOR P (μ W) | |
|---|---------------|--|---|
| Dynamic power dissipation per package (P) | 5 10 15 | $1\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$ $5\,600 f_i + \sum (f_o C_L) \times V_{DD}^2$ $16\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$ | where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V) |

AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

| | V_{DD} V | SYMBOL | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION FORMULA |
|--|---------------|-----------|------|-----------------|---------------------|---|
| Propagation delays CP \rightarrow O _n HIGH to LOW | 5 10 15 | t_{PHL} | | 110 45 30 | 220 90 60 ns | $83\text{ ns} + (0,55\text{ ns/pF}) C_L$ $34\text{ ns} + (0,23\text{ ns/pF}) C_L$ $22\text{ ns} + (0,16\text{ ns/pF}) C_L$ |
| LOW to HIGH | 5 10 15 | t_{PLH} | | 115 45 35 | 230 95 65 ns | $88\text{ ns} + (0,55\text{ ns/pF}) C_L$ $34\text{ ns} + (0,23\text{ ns/pF}) C_L$ $27\text{ ns} + (0,16\text{ ns/pF}) C_L$ |
| CP \rightarrow TC HIGH to LOW | 5 10 15 | t_{PHL} | | 130 55 35 | 260 105 75 ns | $103\text{ ns} + (0,55\text{ ns/pF}) C_L$ $44\text{ ns} + (0,23\text{ ns/pF}) C_L$ $27\text{ ns} + (0,16\text{ ns/pF}) C_L$ |
| LOW to HIGH | 5 10 15 | t_{PLH} | | 140 55 40 | 280 115 80 ns | $113\text{ ns} + (0,55\text{ ns/pF}) C_L$ $44\text{ ns} + (0,23\text{ ns/pF}) C_L$ $32\text{ ns} + (0,16\text{ ns/pF}) C_L$ |
| CET \rightarrow TC HIGH to LOW | 5 10 15 | t_{PHL} | | 105 50 35 | 210 100 75 ns | $78\text{ ns} + (0,55\text{ ns/pF}) C_L$ $39\text{ ns} + (0,23\text{ ns/pF}) C_L$ $27\text{ ns} + (0,16\text{ ns/pF}) C_L$ |
| LOW to HIGH | 5 10 15 | t_{PLH} | | 90 35 25 | 185 70 50 ns | $63\text{ ns} + (0,55\text{ ns/pF}) C_L$ $24\text{ ns} + (0,23\text{ ns/pF}) C_L$ $17\text{ ns} + (0,16\text{ ns/pF}) C_L$ |
| $\overline{\text{MR}} \rightarrow$ O _n HIGH to LOW | 5 10 15 | t_{PHL} | | 120 50 35 | 245 100 70 ns | $93\text{ ns} + (0,55\text{ ns/pF}) C_L$ $39\text{ ns} + (0,23\text{ ns/pF}) C_L$ $27\text{ ns} + (0,16\text{ ns/pF}) C_L$ |
| $\overline{\text{MR}} \rightarrow$ TC HIGH to LOW | 5 10 15 | t_{PHL} | | 145 60 45 | 295 120 85 ns | $118\text{ ns} + (0,55\text{ ns/pF}) C_L$ $49\text{ ns} + (0,23\text{ ns/pF}) C_L$ $37\text{ ns} + (0,16\text{ ns/pF}) C_L$ |

4-bit synchronous binary counter with asynchronous reset

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| | V _{DD} V | SYMBOL | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION FORMULA | |
|--|----------------------|------------------|------|------|------|----------------------------------|------------------------------------|
| Output transition times HIGH to LOW | 5 | t _{THL} | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) C _L |
| | 10 | | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) C _L |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C _L |
| LOW to HIGH | 5 | t _{TLH} | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) C _L |
| | 10 | | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) C _L |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C _L |

AC CHARACTERISTICS

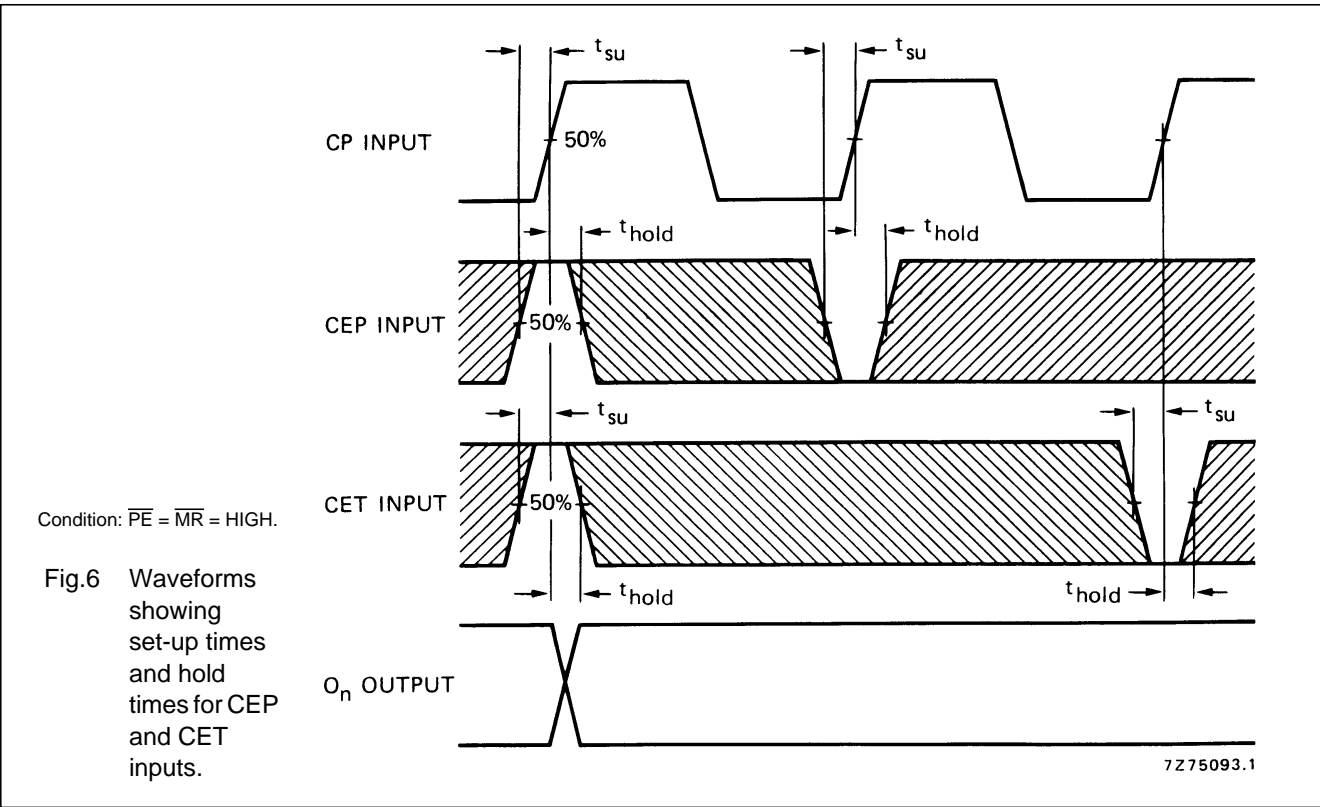
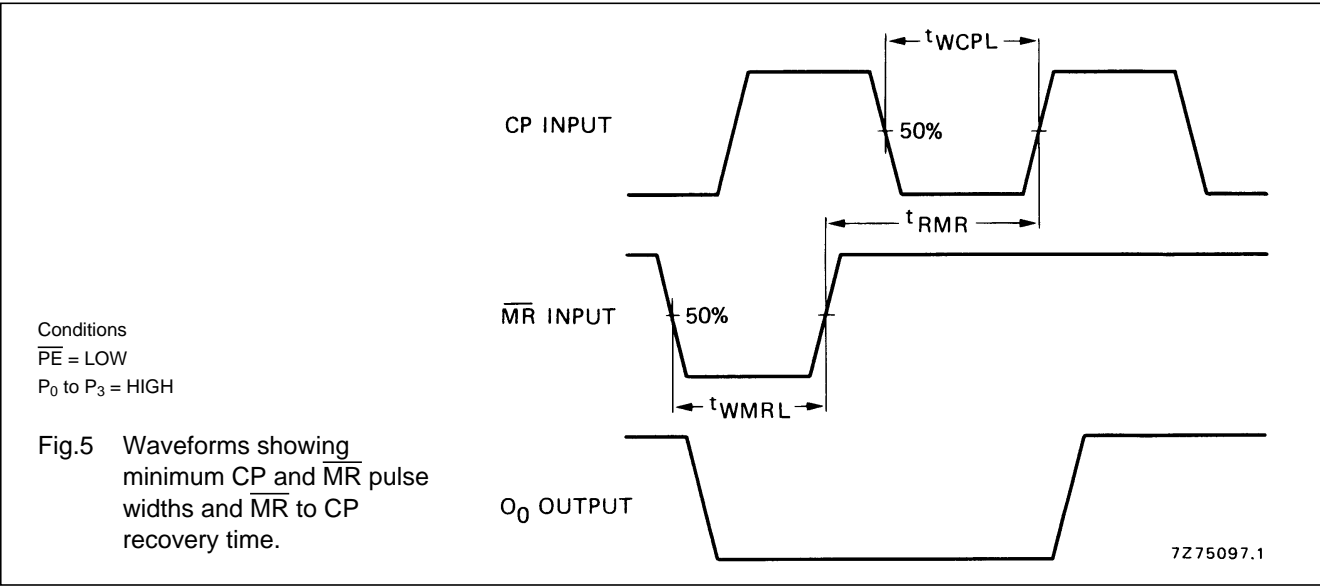
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

| | V _{DD} V | SYMBOL | MIN. | TYP. | MAX. | |
|--|----------------------|-------------------|------|------|------|--|
| Minimum clock pulse width; LOW | 5 | t _{WCPL} | 100 | 50 | ns | see also waveforms Figs 5, 6, 7 and 8 |
| | 10 | | 40 | 20 | ns | |
| | 15 | | 30 | 15 | ns | |
| Minimum $\overline{\text{MR}}$ pulse width; LOW | 5 | t _{WMRL} | 100 | 50 | ns | |
| | 10 | | 40 | 20 | ns | |
| | 15 | | 30 | 15 | ns | |
| Recovery time for $\overline{\text{MR}}$ | 5 | t _{RMR} | 25 | 0 | ns | |
| | 10 | | 15 | 0 | ns | |
| | 15 | | 10 | 0 | ns | |
| Set-up times P _n → CP | 5 | t _{su} | 110 | 55 | ns | |
| | 10 | | 40 | 20 | ns | |
| | 15 | | 30 | 15 | ns | |
| $\overline{\text{PE}}$ → CP | 5 | t _{su} | 120 | 60 | ns | |
| | 10 | | 40 | 20 | ns | |
| | 15 | | 25 | 10 | ns | |
| CEP, CET → CP | 5 | t _{su} | 260 | 130 | ns | |
| | 10 | | 100 | 50 | ns | |
| | 15 | | 70 | 35 | ns | |
| Hold times P _n → CP | 5 | t _{hold} | 20 | −35 | ns | |
| | 10 | | 10 | −10 | ns | |
| | 15 | | 5 | −10 | ns | |
| $\overline{\text{PE}}$ → CP | 5 | t _{hold} | 15 | −45 | ns | |
| | 10 | | 5 | −15 | ns | |
| | 15 | | 5 | −10 | ns | |
| CEP, CET → CP | 5 | t _{hold} | 25 | −105 | ns | |
| | 10 | | 15 | −35 | ns | |
| | 15 | | 10 | −25 | ns | |

4-bit synchronous binary counter with asynchronous reset

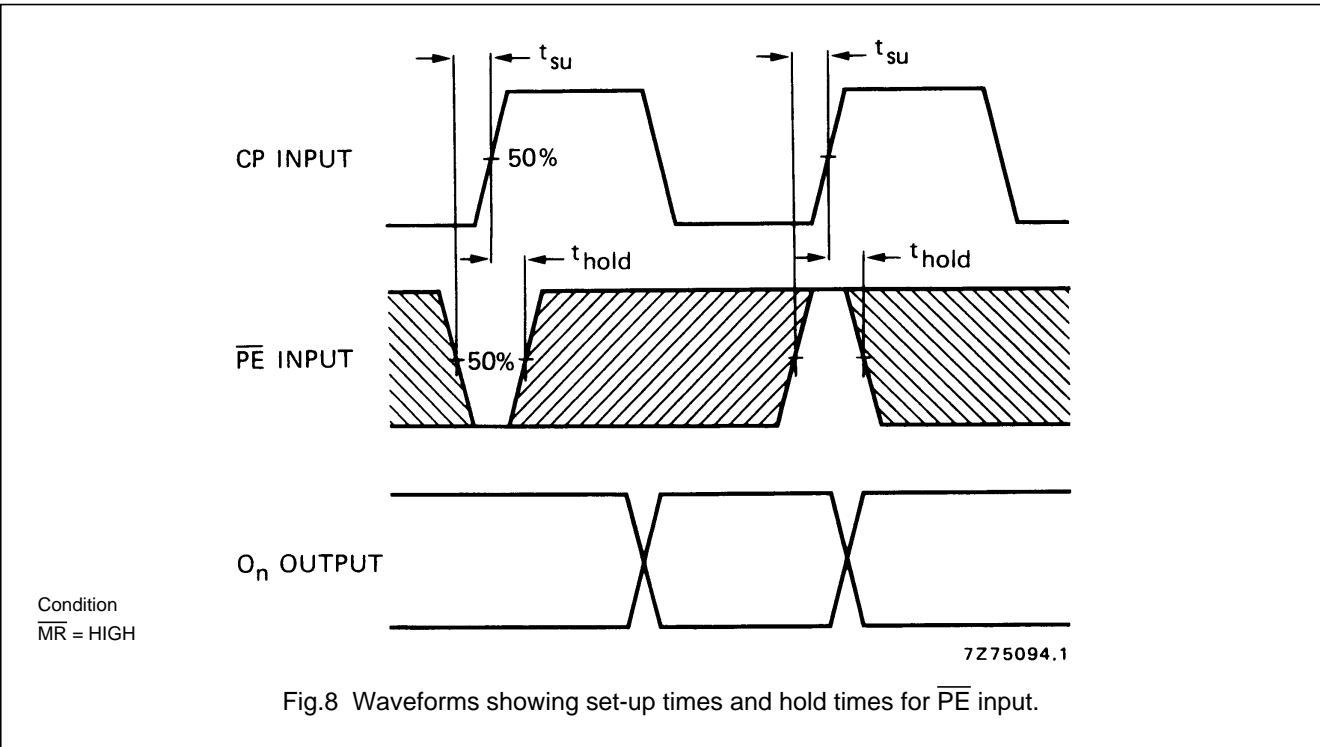
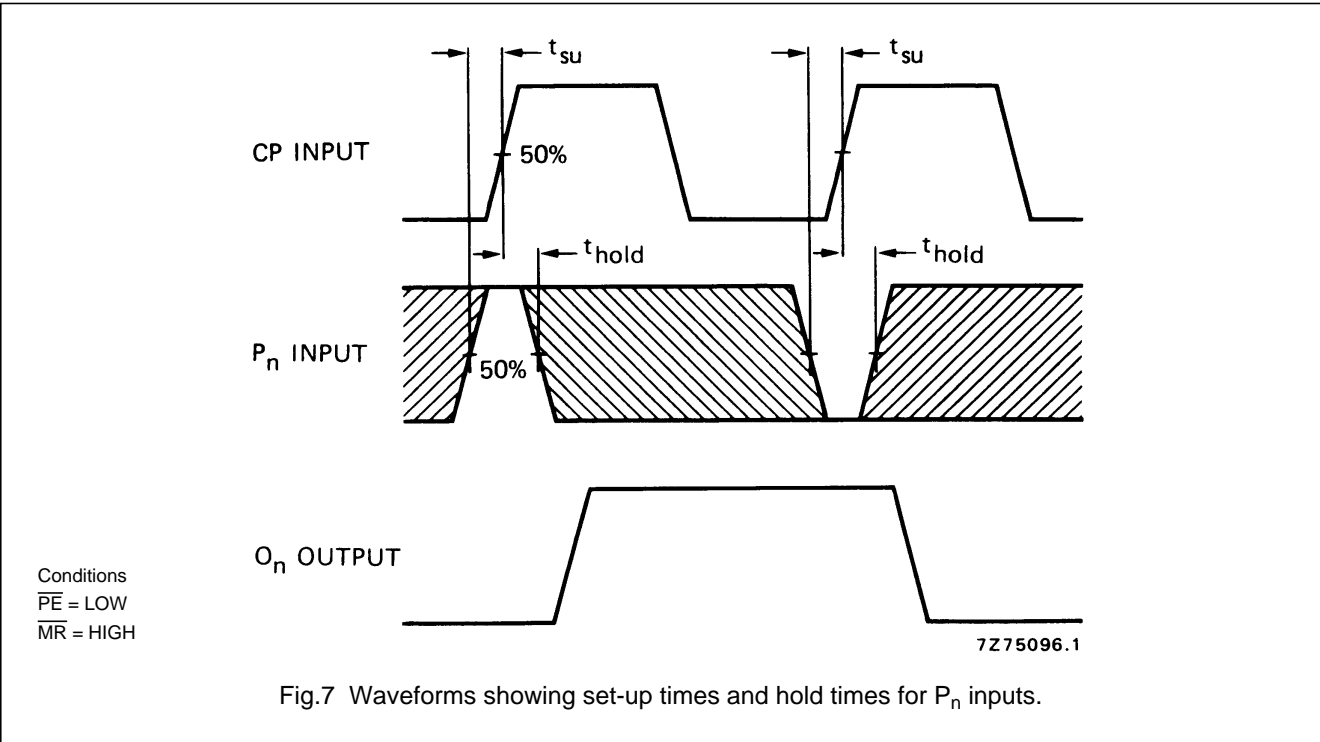
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| | V _{DD} V | SYMBOL | MIN. | TYP. | MAX. | |
|-------------------------------|----------------------|------------------|------|------|------|--|
| Maximum clock pulse frequency | 5 | f _{max} | 2,5 | 5 | MHz | |
| | 10 | | 7 | 14 | MHz | |
| | 15 | | 9 | 18 | MHz | |



4-bit synchronous binary counter with asynchronous reset

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Note
Set-up and hold times are shown as positive values but may be specified as negative values.

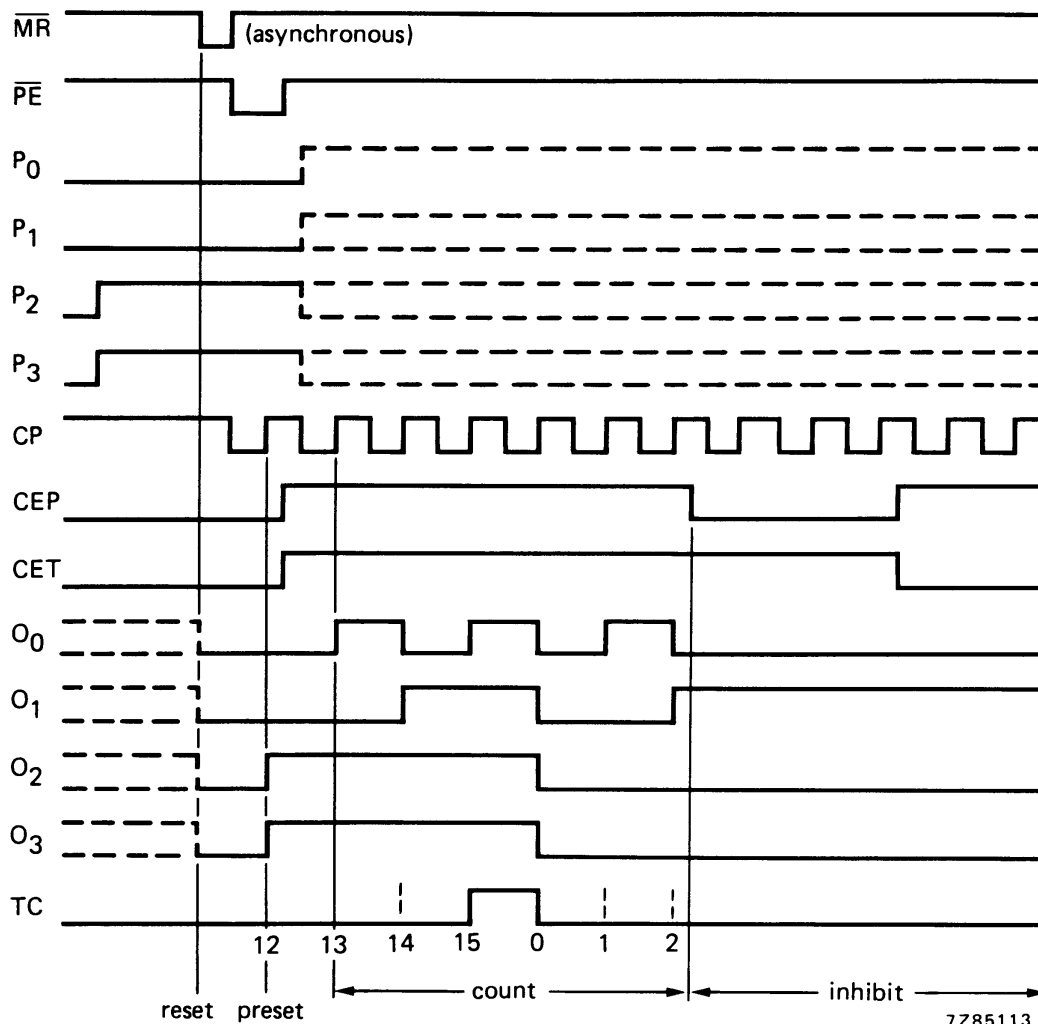
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Fig.9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40161B is:

- Programmable binary counter.

4-bit synchronous binary counter with asynchronous reset

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