

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4527B **MSI** BCD rate multiplier

Product specification
File under Integrated Circuits, IC04

January 1995

BCD rate multiplier

HEF4527B
MSI

DESCRIPTION

The HEF4527B is a BCD rate multiplier with two buffered rate outputs (O_1 and \overline{O}_1), two buffered terminal count outputs (TC and \overline{TC}), four BCD rate select inputs (S_A , S_B , S_C , S_D), a common clock input (CP), a preset input (PL), an overriding asynchronous clear input (CL), a strobe input (STR), a cascade input (CAS) and an active LOW count enable input (\overline{CE}).

The BCD rate multiplier provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD number, there will be six output pulses for every ten clock input pulses. The output is clocked on the negative-going transition of the clock.

When \overline{CE} , STR, CAS, CL and PL are LOW, the rate pulses are available at the outputs O_1 and \overline{O}_1 , the terminal count pulses at TC and \overline{TC} .

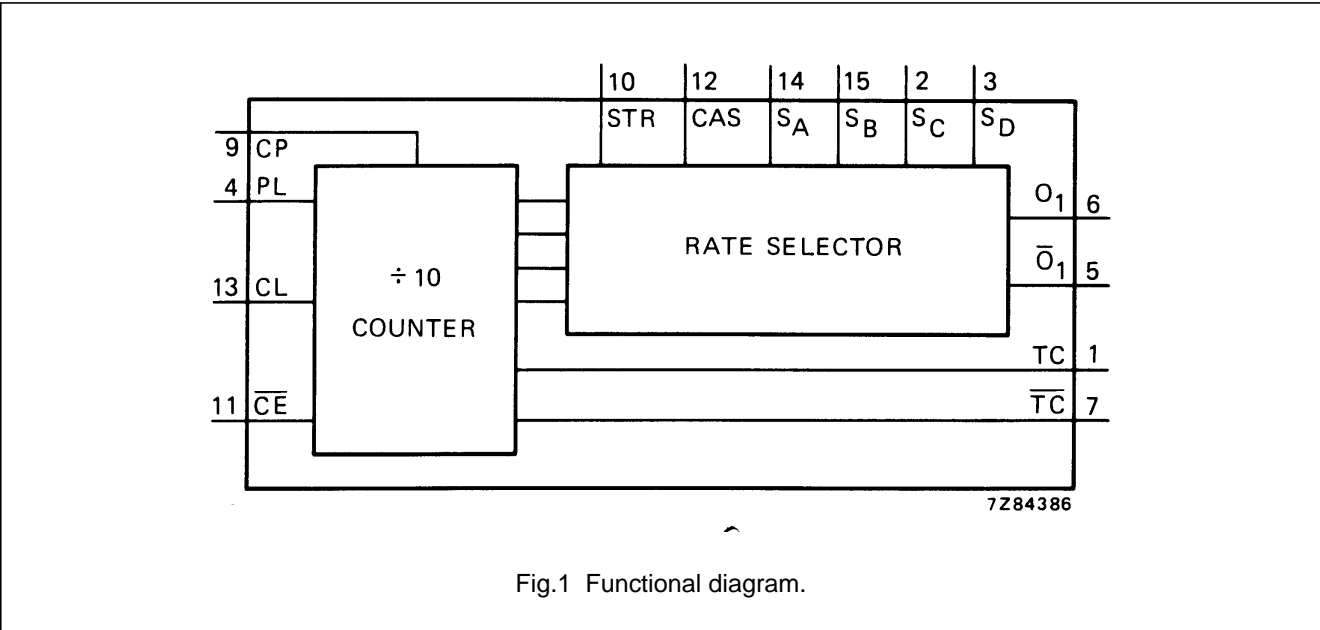
A HIGH on CL resets the counter, independent of all other input conditions and a rate of 10 pulses is available at O_1 and \overline{O}_1 when S_D is HIGH. When \overline{CE} is HIGH, the counter is disabled, the state of the outputs (O_1 , \overline{O}_1) depend on the content of the counter.

A HIGH on PL sets the counter in the '9' state and TC becomes HIGH.

A HIGH on STR inhibits the outputs O_1 and \overline{O}_1 . A HIGH on CAS forces the output O_1 to HIGH, while the state of \overline{O}_1 depends on the inputs S_A to S_D (see lines 1 to 16 of function table).

This device may be used to perform arithmetic operations. For the add mode and multiply mode see Figs 5 and 6.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.



FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

BCD rate multiplier

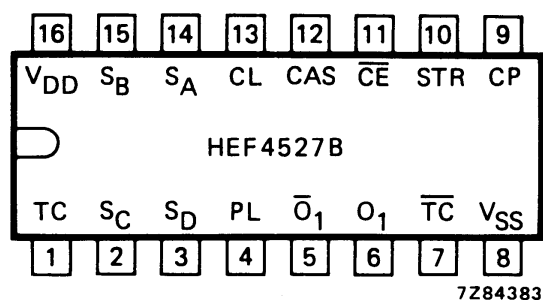
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Fig.2 Pinning diagram.

HEF4527BP(N): 16-lead DIL; plastic (SOT38-1)
 HEF4527BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
 HEF4527BT(D): 16-lead SO; plastic (SOT109-1)

(): Package Designator North America

PINNING

| | |
|------------------------------------|-------------------------------------|
| CP | clock input |
| PL | preset to '9' input |
| CL | counter clear input |
| \overline{CE} | count enable input (active LOW) |
| STR | strobe input |
| CAS | cascade input |
| S _A to S _D | rate select inputs |
| O ₁ to \overline{O}_1 | rate outputs |
| TC | terminal count output (active HIGH) |
| \overline{TC} | terminal count output (active LOW) |

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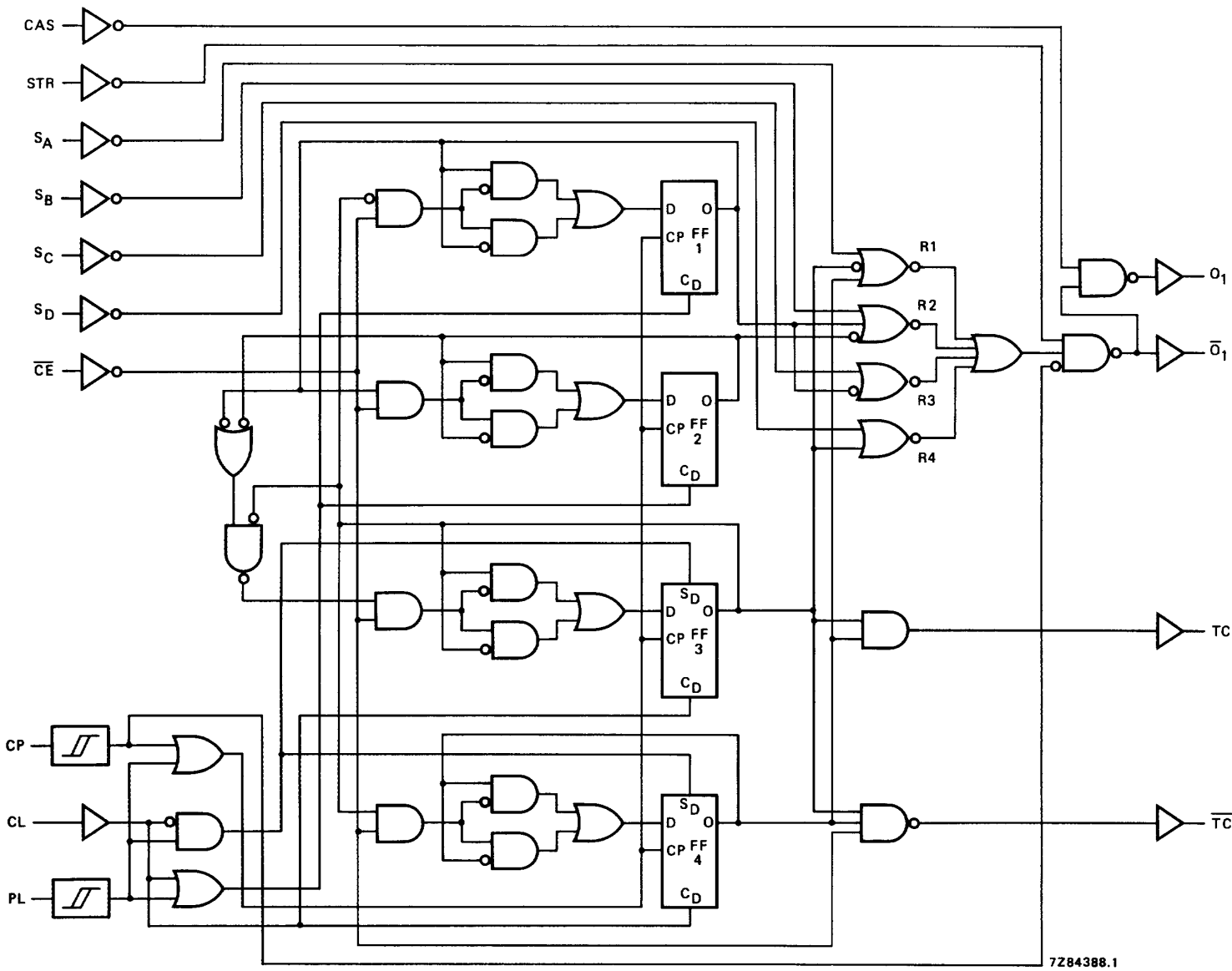


Fig.3 Logic diagram.

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FUNCTION TABLE

| INPUTS | | | | | | | | | | OUTPUTS | | | | MODE OF OPERATION |
|---------------------------------|----------------|----------------|----------------|----|------------------------|-----|-----|----|----|---------------------------------|-------------------------|------------------------|-----|---|
| NUMBER OF PULSES OR LOGIC LEVEL | | | | | | | | | | NUMBER OF PULSES OR LOGIC LEVEL | | | | |
| S _D | S _C | S _B | S _A | CP | $\overline{\text{CE}}$ | STR | CAS | CL | PL | O ₁ | $\overline{\text{O}}_1$ | $\overline{\text{TC}}$ | TC | |
| L | L | L | L | 10 | L | L | L | L | L | L | H | 1 | 1 | rate pulses at the outputs depend on the BCD input number at S _A to S _D |
| L | L | L | H | 10 | L | L | L | L | L | 1 | 1 | 1 | 1 | |
| L | L | H | L | 10 | L | L | L | L | L | 2 | 2 | 1 | 1 | |
| L | L | H | H | 10 | L | L | L | L | L | 3 | 3 | 1 | 1 | |
| L | H | L | L | 10 | L | L | L | L | L | 4 | 4 | 1 | 1 | |
| L | H | L | H | 10 | L | L | L | L | L | 5 | 5 | 1 | 1 | |
| L | H | H | L | 10 | L | L | L | L | L | 6 | 6 | 1 | 1 | |
| L | H | H | H | 10 | L | L | L | L | L | 7 | 7 | 1 | 1 | |
| H | L | L | L | 10 | L | L | L | L | L | 8 | 8 | 1 | 1 | |
| H | L | L | H | 10 | L | L | L | L | L | 9 | 9 | 1 | 1 | |
| H | L | H | L | 10 | L | L | L | L | L | 8 | 8 | 1 | 1 | |
| H | L | H | H | 10 | L | L | L | L | L | 9 | 9 | 1 | 1 | |
| H | H | L | L | 10 | L | L | L | L | L | 8 | 8 | 1 | 1 | |
| H | H | L | H | 10 | L | L | L | L | L | 9 | 9 | 1 | 1 | |
| H | H | H | L | 10 | L | L | L | L | L | 8 | 8 | 1 | 1 | |
| H | H | H | H | 10 | L | L | L | L | L | 9 | 9 | 1 | 1 | |
| X | X | X | X | X | H | L | L | L | L | (5) | (5) | H | (5) | CE = H; counter disabled |
| X | X | X | X | 10 | L | H | L | L | L | L | H | 1 | 1 | outputs O ₁ and O ₂ disabled |
| X | X | X | X | 10 | L | L | H | L | L | H | (4) | 1 | 1 | output O ₁ disabled |
| H | X | X | X | 10 | L | L | L | H | X | 10 | 10 | H | L | CL = H |
| L | X | X | X | X | L | L | L | H | X | L | H | H | L | counter reset |
| X | X | X | X | X | L | L | L | L | H | L | H | L | H | PL = H; preset to '9' |

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. Same output as the first 16 lines of this function table (depends on the values of S_A to S_D).
5. Depends on internal state of the counter.

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns.

| PARAMETER | V_{DD} V | SYMBOL | MIN. | TYP. | MAX. | UNIT | TYPICAL EXTRAPOLATION FORMULA |
|---|---------------|-----------|------|------|------|------|----------------------------------|
| Propagation delays | | | | | | | |
| CP \rightarrow O ₁ , \overline{O}_1 | 5 | | | 130 | 260 | ns | 103 ns + (0,55 ns/pF) C_L |
| HIGH to LOW | 10 | t_{PHL} | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) C_L |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 130 | 260 | ns | 103 ns + (0,55 ns/pF) C_L |
| | 10 | | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) C_L |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) C_L |
| CP \rightarrow TC | 5 | | | 175 | 350 | ns | 148 ns + (0,55 ns/pF) C_L |
| HIGH to LOW | 10 | t_{PHL} | | 65 | 130 | ns | 54 ns + (0,23 ns/pF) C_L |
| | 15 | | | 45 | 90 | ns | 37 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 160 | 320 | ns | 133 ns + (0,55 ns/pF) C_L |
| | 10 | | | 65 | 130 | ns | 54 ns + (0,23 ns/pF) C_L |
| | 15 | | | 45 | 90 | ns | 37 ns + (0,16 ns/pF) C_L |
| CP \rightarrow \overline{TC} | 5 | | | 175 | 350 | ns | 148 ns + (0,55 ns/pF) C_L |
| HIGH to LOW | 10 | t_{PHL} | | 65 | 130 | ns | 54 ns + (0,23 ns/pF) C_L |
| | 15 | | | 50 | 100 | ns | 42 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 150 | 300 | ns | 123 ns + (0,55 ns/pF) C_L |
| | 10 | | | 60 | 120 | ns | 49 ns + (0,23 ns/pF) C_L |
| | 15 | | | 45 | 90 | ns | 37 ns + (0,16 ns/pF) C_L |
| CAS \rightarrow O ₁ | 5 | | | 90 | 180 | ns | 63 ns + (0,55 ns/pF) C_L |
| HIGH to LOW | 10 | t_{PHL} | | 35 | 70 | ns | 24 ns + (0,23 ns/pF) C_L |
| | 15 | | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 70 | 140 | ns | 43 ns + (0,55 ns/pF) C_L |
| | 10 | | | 30 | 60 | ns | 19 ns + (0,23 ns/pF) C_L |
| | 15 | | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) C_L |
| STR \rightarrow O ₁ , \overline{O}_1 | 5 | | | 100 | 200 | ns | 73 ns + (0,55 ns/pF) C_L |
| HIGH to LOW | 10 | t_{PHL} | | 40 | 80 | ns | 29 ns + (0,23 ns/pF) C_L |
| | 15 | | | 30 | 60 | ns | 22 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 85 | 170 | ns | 58 ns + (0,55 ns/pF) C_L |
| | 10 | | | 35 | 70 | ns | 24 ns + (0,23 ns/pF) C_L |
| | 15 | | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) C_L |
| $\overline{CE} \rightarrow \overline{TC}$ | 5 | | | 95 | 190 | ns | 68 ns + (0,55 ns/pF) C_L |
| HIGH to LOW | 10 | t_{PHL} | | 35 | 70 | ns | 24 ns + (0,23 ns/pF) C_L |
| | 15 | | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 65 | 130 | ns | 38 ns + (0,55 ns/pF) C_L |
| | 10 | | | 30 | 60 | ns | 19 ns + (0,23 ns/pF) C_L |
| | 15 | | | 20 | 40 | ns | 12 ns + (0,16 ns/pF) C_L |

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| PARAMETER | V _{DD} V | SYMBOL | MIN. | TYP. | MAX. | UNIT | TYPICAL EXTRAPOLATION FORMULA |
|---|----------------------|-------------------|------|------|------|------|--------------------------------------|
| CL → O ₁ HIGH to LOW | 5 | t _{PHL} | | 145 | 290 | ns | 118 ns + (0,55 ns/pF) C _L |
| | 10 | | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) C _L |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) C _L |
| CL → \overline{O}_1 LOW to HIGH | 5 | t _{PLH} | | 145 | 290 | ns | 118 ns + (0,55 ns/pF) C _L |
| | 10 | | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) C _L |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) C _L |
| Propagation delays PL → O ₁ , \overline{O}_1 HIGH to LOW | 5 | t _{PHL} | | 260 | 520 | ns | 233 ns + (0,55 ns/pF) C _L |
| | 10 | | | 100 | 200 | ns | 89 ns + (0,23 ns/pF) C _L |
| | 15 | | | 70 | 140 | ns | 62 ns + (0,16 ns/pF) C _L |
| | 5 | t _{PLH} | | 235 | 470 | ns | 208 ns + (0,55 ns/pF) C _L |
| | 10 | | | 90 | 180 | ns | 79 ns + (0,23 ns/pF) C _L |
| | 15 | | | 50 | 100 | ns | 42 ns + (0,16 ns/pF) C _L |
| Minimum clock pulse width HIGH | 5 | t _{WCPH} | | 45 | 90 | ns | |
| | 10 | | | 18 | 36 | ns | |
| | 15 | | | 12 | 24 | ns | |
| Minimum CL pulse width; HIGH | 5 | t _{WCLH} | | 20 | 40 | ns | |
| | 10 | | | 12 | 24 | ns | |
| | 15 | | | 10 | 20 | ns | |
| Minimum PL pulse width; HIGH | 5 | t _{WPLH} | | 50 | 100 | ns | |
| | 10 | | | 20 | 40 | ns | |
| | 15 | | | 15 | 30 | ns | |
| Set-up times $\overline{CE} \rightarrow CP$ | 5 | t _{su} | 30 | 15 | | ns | |
| | 10 | | 20 | 10 | | ns | |
| | 15 | | 12 | 5 | | ns | |
| Recovery times CL → CP | 5 | t _{RCL} | 20 | 10 | | ns | |
| | 10 | | 16 | 8 | | ns | |
| | 15 | | 10 | 5 | | ns | |
| PL → CP | 5 | t _{RPL} | 80 | 40 | | ns | |
| | 10 | | 36 | 18 | | ns | |
| | 15 | | 25 | 10 | | ns | |
| Maximum clock pulse frequency | 5 | f _{max} | 4,5 | 9 | | MHz | |
| | 10 | | 11 | 22 | | MHz | |
| | 15 | | 16 | 32 | | MHz | |

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AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

| | V _{DD} V | TYPICAL FORMULA FOR P (μW) | |
|---|----------------------|---|---|
| Dynamic power dissipation per package (P) | 5 10 15 | $1\,050\,f_i + \sum (f_o C_L) \times V_{DD}^2$ $4\,500\,f_i + \sum (f_o C_L) \times V_{DD}^2$ $10\,500\,f_i + \sum (f_o C_L) \times V_{DD}^2$ | where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V) |

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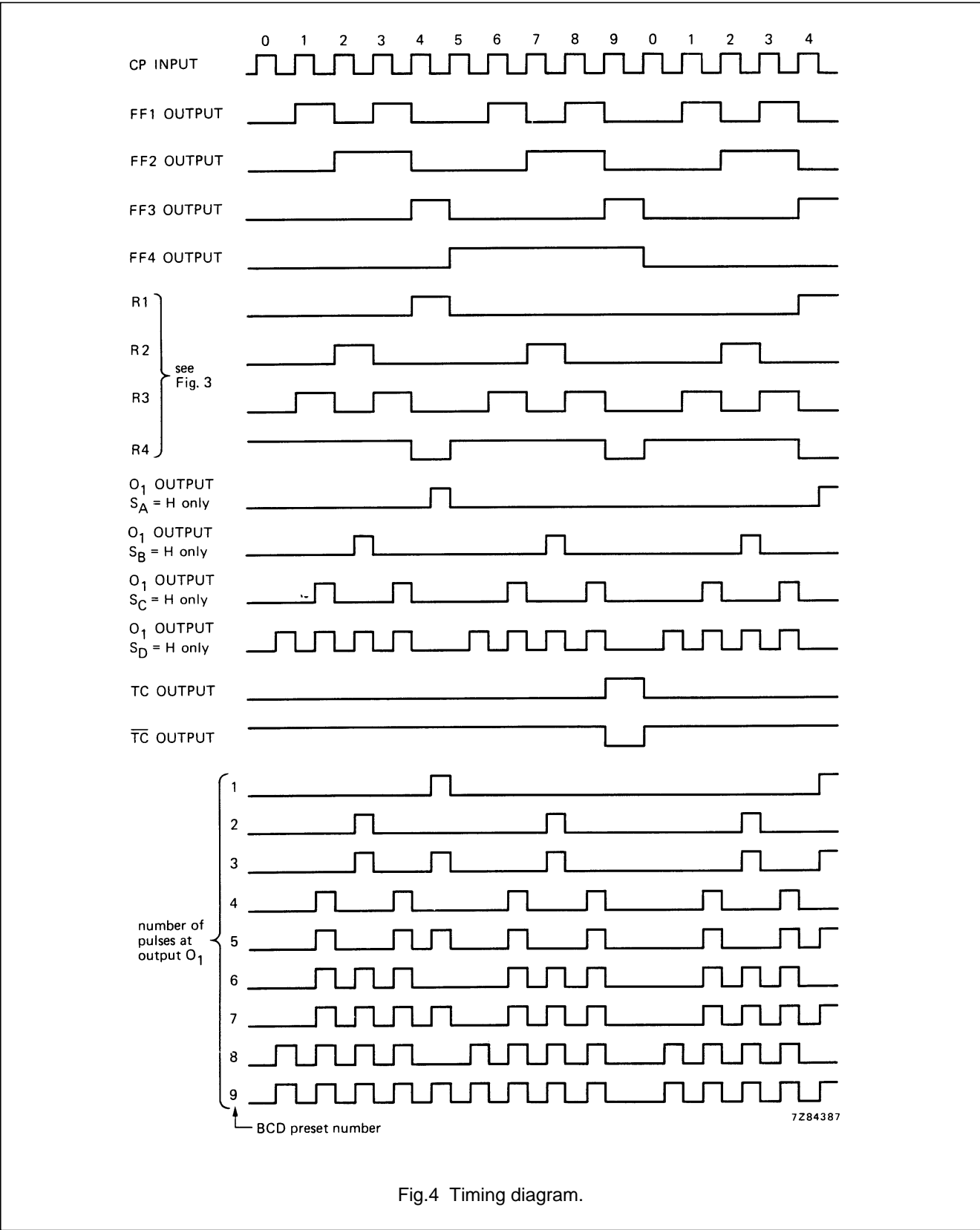


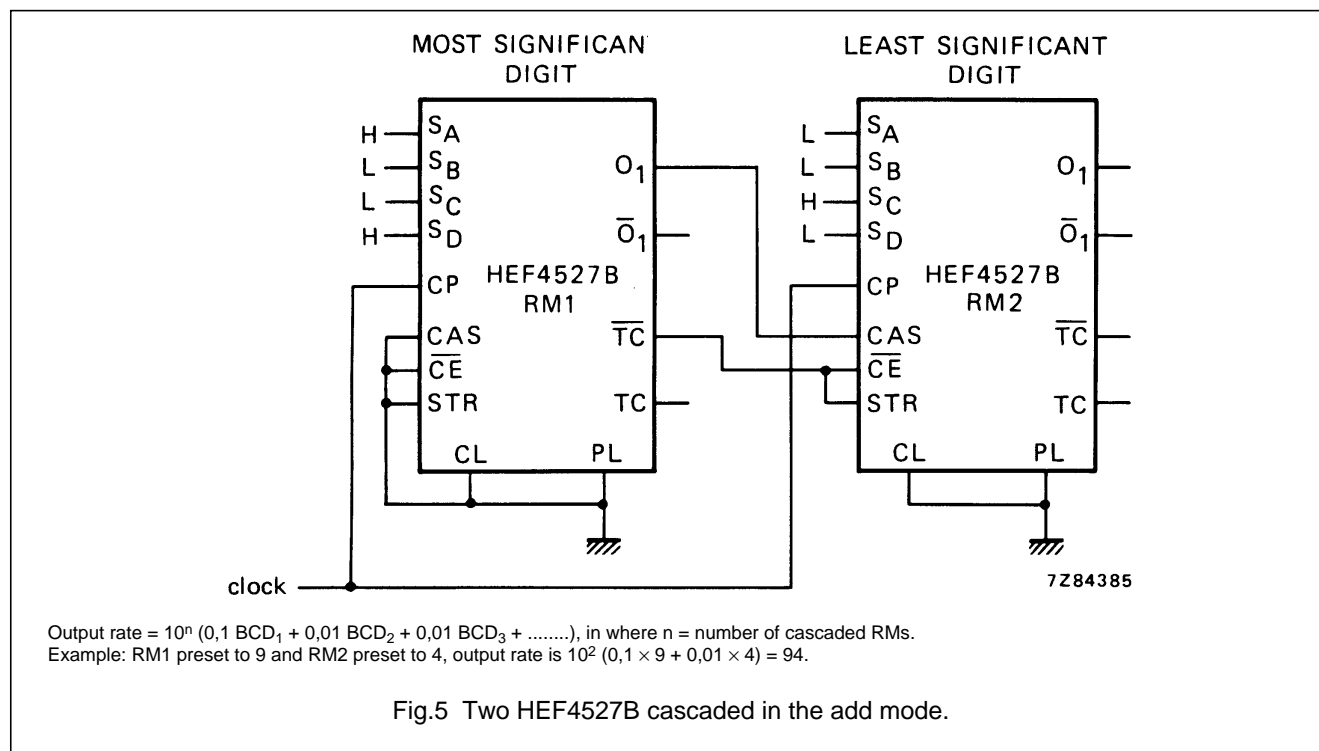
Fig.4 Timing diagram.

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APPLICATION INFORMATION

Add mode



Multiply mode

