

DATA SHEET

74F620

Octal bus transceiver, inverting (3state)

74F623

Octal bus transceiver, non-inverting
(3state)

Product specification

1989 Apr 06

IC15 Data Handbook

Transceivers

74F620/74F623

74F620 Octal Bus Transceiver, Inverting (3-State)
74F623 Octal Bus Transceiver, Non-Inverting (3-State)

FEATURES

- High-impedance NPN base inputs for reduced loading (70µA in High and Low states)
- Ideal for applications which require high output drive and minimal bus loading
- Octal bidirectional bus interface
- 3-State buffer outputs sink 64mA and source 15mA
- 74F620, inverting
- 74F623, non-inverting

DESCRIPTION

The 74F620 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 74F623 is a non-inverting version of the 74F620.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the

Enable inputs ($\overline{\text{OEBA}}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 74F620 and 74F623 the capability to store data by the simultaneous enabling of $\overline{\text{OEBA}}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain in their last states.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F620	3.5ns	80mA
74F623	4.5ns	105mA

ORDERING INFORMATION

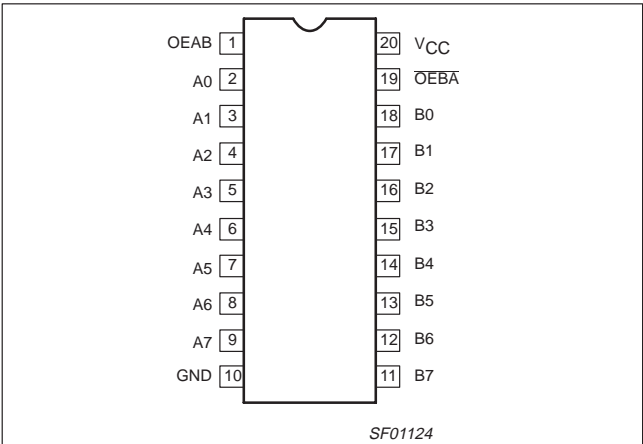
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	PKG DWG #
20-pin plastic DIP	N74F620N, N74623N	SOT146-1
20-pin plastic SOL	N74F620D, N74623D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

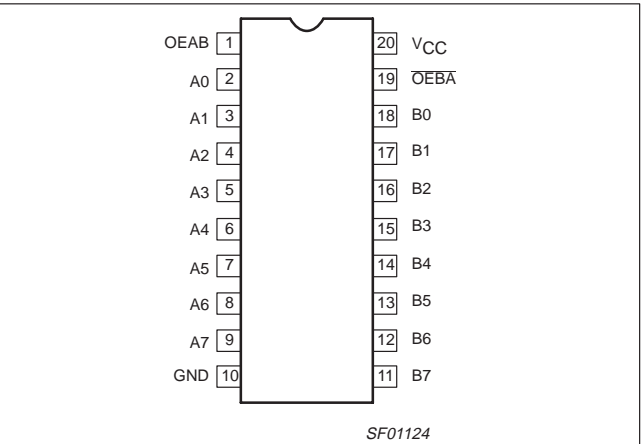
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	3.5/1.16	70µA/70µA
$\overline{\text{OEBA}}$, OEAB	Output Enable inputs	1.0/0.033	20µA/20µA
A0 - A7	Data outputs	150/40	3mA/24mA
B0 - B7	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION – 74F620



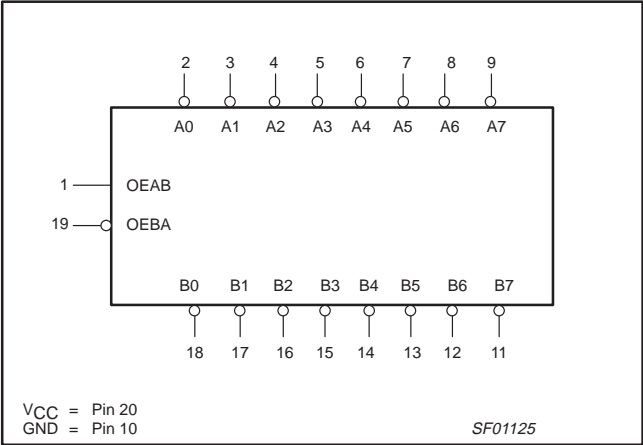
PIN CONFIGURATION – 74F623



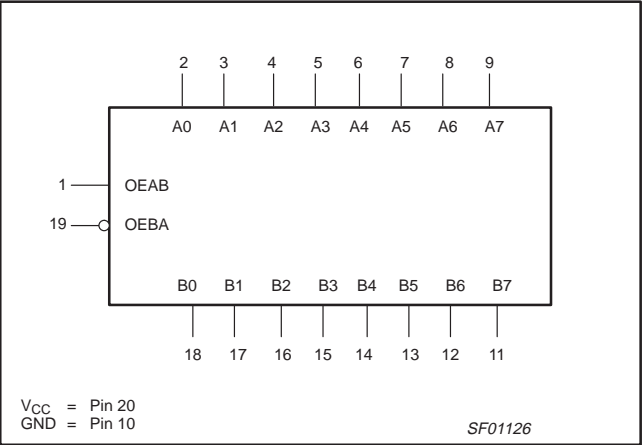
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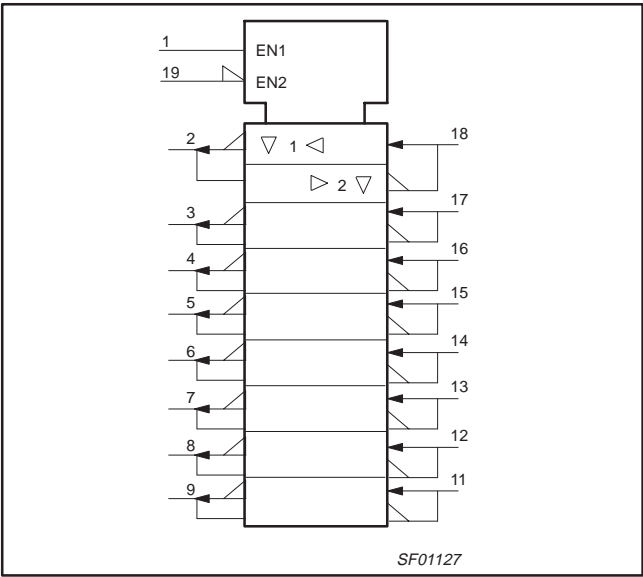
LOGIC SYMBOL – 74F620



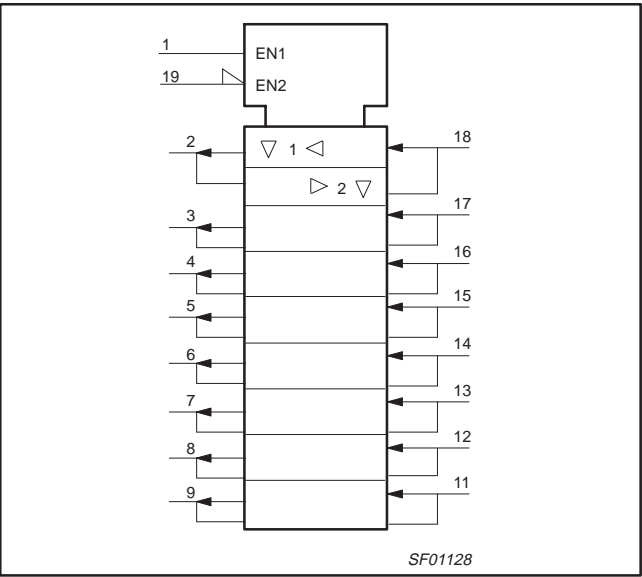
LOGIC SYMBOL – 74F623



IEC/IEEE SYMBOL (IEEE/IEC) – 74F620



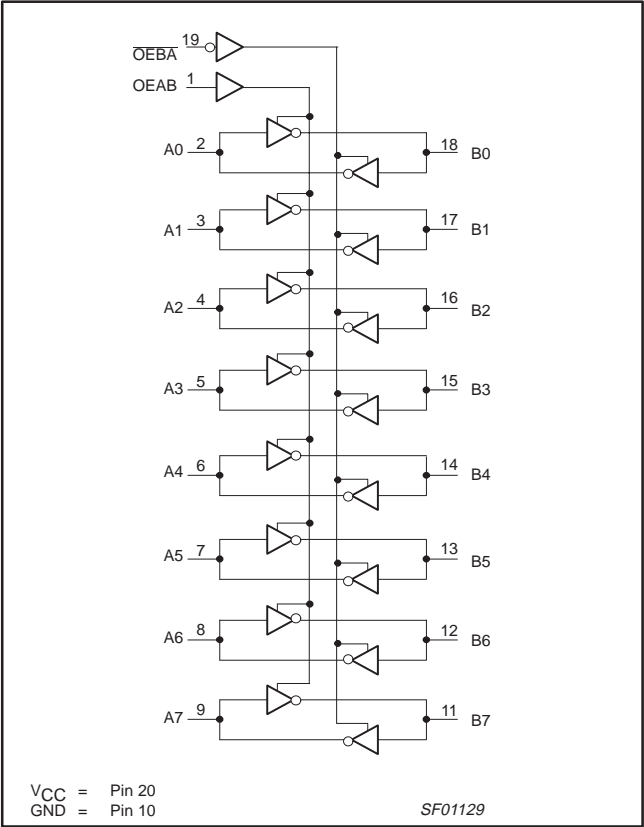
IEC/IEEE SYMBOL (IEEE/IEC) – 74F623



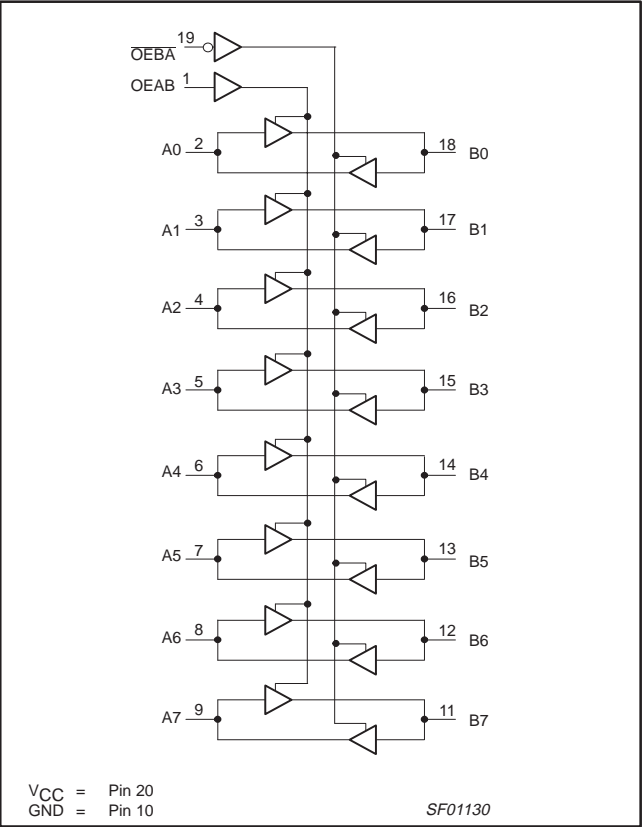
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LOGIC DIAGRAM – 74F620



LOGIC DIAGRAM – 74F623



FUNCTION TABLE

INPUTS		OPERATING MODES	
OEBA	OEAB	74F620	74F623
L	L	\overline{B} data to A bus	B data to A bus
H	H	\overline{A} data to B bus	A data to B bus
H	L	Z	Z
L	H	\overline{B} data to A bus	B data to A bus
		\overline{A} data to B bus	A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A0–A7			−3	mA
		B0–B7			−15	mA
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ^{NO TAG}			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V _{OH}	High-level output voltage	A0–A7 B0–B7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = –3mA	±10%V _{CC}	2.4			V
		±5%V _{CC}			2.7	3.3		V	
		B0–B7		I _{OH} = –15mA	±10%V _{CC}	2.0			V
					±5%V _{CC}	2.0			V
V _{OL}	Low-level output voltage	A0–A7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN,	I _{OL} = 24mA	±10%V _{CC}		0.35	0.50	V
		±5%V _{CC}				0.35	0.50	V	
		B0–B7		I _{OL} = 48mA	±10%V _{CC}		0.38	0.55	V
					I _{OL} = 64mA	±5%V _{CC}		0.42	0.55
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				–0.73	–1.2	V
I _I	Input current at maximum input voltage	OEBA̅, OEAB	V _{CC} = 0.0V, V _I = 7.0V					100	μA
		others	V _{CC} = 5.5V, V _I = 5.5V					1	mA
I _{IH}	High-level input current	OEBA̅, OEAB	V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current	only	V _{CC} = MAX, V _I = 0.5V					–20	μA
I _{OZH} +I _{IH}	Off-state output current, High-level of voltage applied	A0–A7 B0–B7	V _{CC} = MAX, V _I = 2.7V					70	μA
I _{OZL} +I _{IL}	Off-state output current, Low-level of voltage applied		V _{CC} = MAX, V _I = 0.5V					–70	μA
I _{OS}	Short-circuit output current ^{NO TAG}	A0–A7	V _{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	mA
I _{CC}	Supply current (total)	74F620	I _{CCH}	V _{CC} = MAX	OEBA̅=OEAB=4.5V; A0–A7=GND		70	92	mA
			I _{CCL}		OEBA̅=OEAB=4.5V; A0–A7=4.5V		84	110	mA
			I _{CCZ}		OEAB=GND; OEBA̅=A0–A7=4.5V		84	110	mA
		74F623	I _{CCH}	V _{CC} = MAX	OEBA̅=OEAB=4.5V; A0–A7=4.5V		110	140	mA
			I _{CCL}		OEBA̅=OEAB=4.5V; A0–A7=GND		110	140	mA
			I _{CCZ}		OEAB=GND; OEBA̅=A0–A7=4.5V		99	130	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS – 74F620

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, \overline{OEBA} to An	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, \overline{OEBA} to An	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	10.5 10.5	ns

AC ELECTRICAL CHARACTERISTICS – 74F623

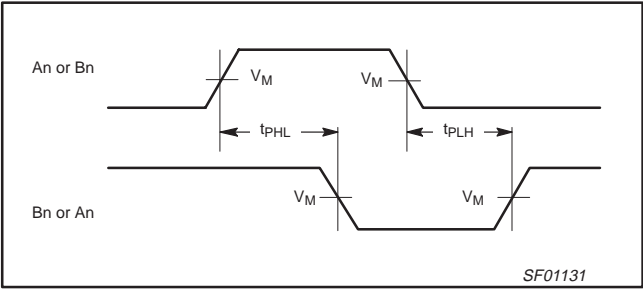
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay An to Bn	Waveform 1	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	6.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay Bn to An	Waveform 1	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	6.5 7.5	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level, \overline{OEBA} to An	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	12.0 10.0	ns
t _{PHZ} t _{PLZ}	Output Disable time to High or Low level, \overline{OEBA} to An	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	7.5 7.0	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	11.5 9.5	ns
t _{PHZ} t _{PLZ}	Output Disable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	10.0 10.0	ns

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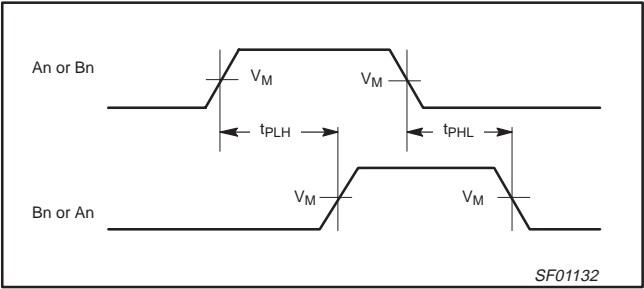
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AC WAVEFORMS

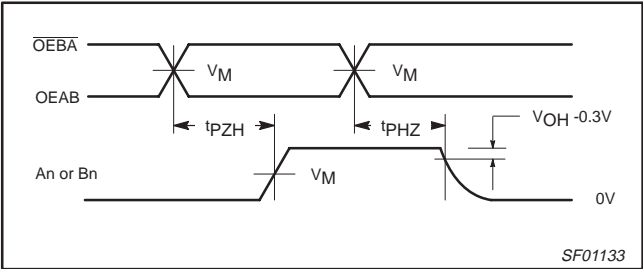
For all waveforms, $V_M = 1.5V$.



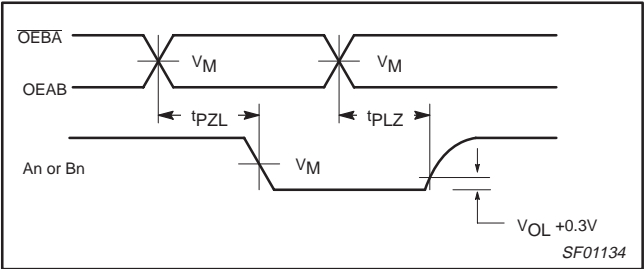
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

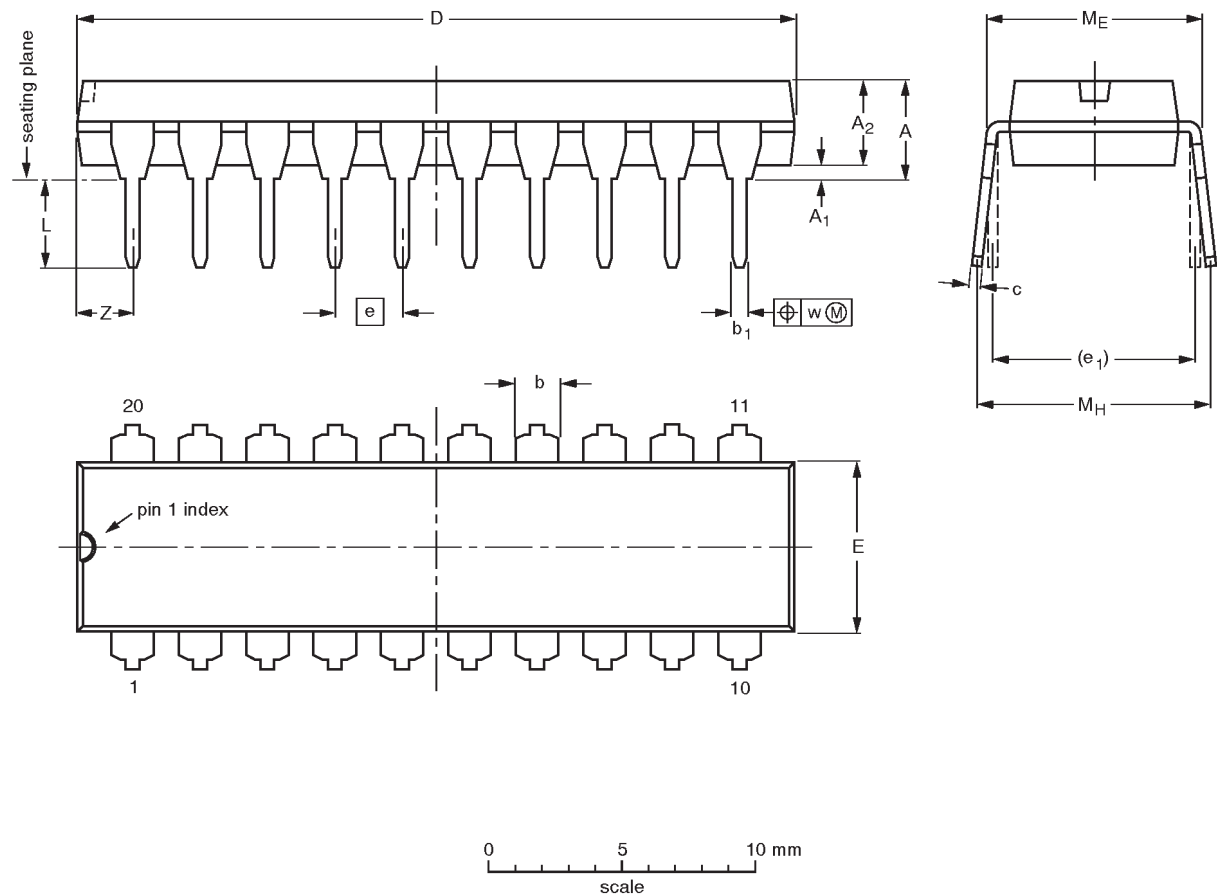
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

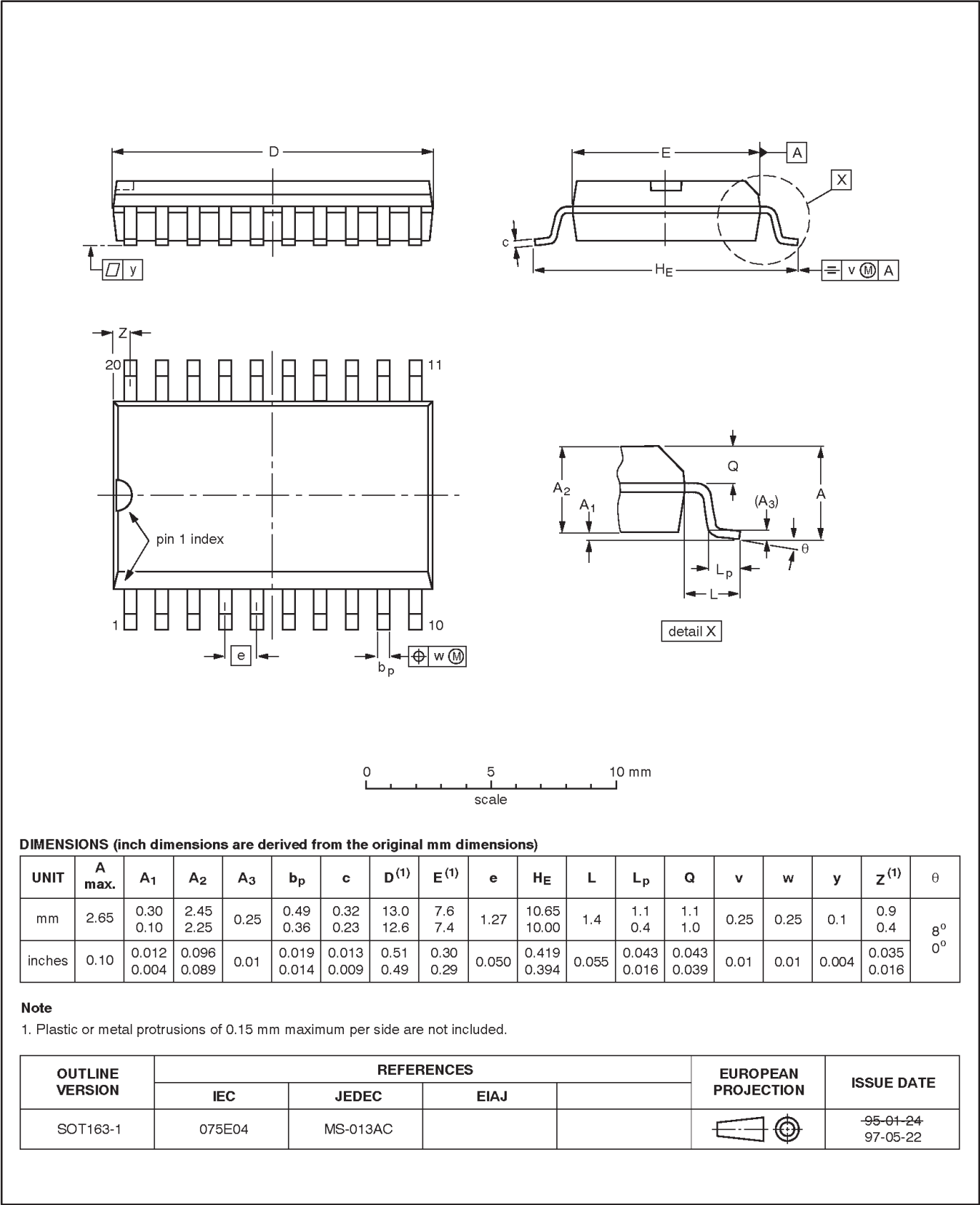
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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