

# DATA SHEET

**74F1240**

Octal inverter buffer (3-State)

~~74F1241~~

~~Octal buffer (3-State)\*~~

\* Discontinued part. Please see the Discontinued Product List.

Product specification  
Supersedes data of 1989 Apr 04  
IC15 Data Handbook

1999 Jan 08

## Buffers

## 74F1240, 74F1241\*

74F1240 Octal inverter buffer (3-State)

### FEATURES

- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Low power, light loading
- Functional pin-for-pin equivalent of 74F240 and 74F241
- 1/30th the bus loading of 74F240 and 74F241
- Provides ideal interface and increase fan-out of MOS microprocessors
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA
74F1241	4.5ns	46mA

### ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	DRAWING NUMBER
20-pin plastic DIP	N74F1240N	SOT146-1
20-pin plastic SOL	N74F1240D	SOT163-1

### DESCRIPTION

The 74F1240 and 74F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables,  $\overline{OE}a$  and  $\overline{OE}b$ , each controlling four of the 3-State outputs.

### INPUT AND OUTPUT LOADING AND FAN OUT TABLE

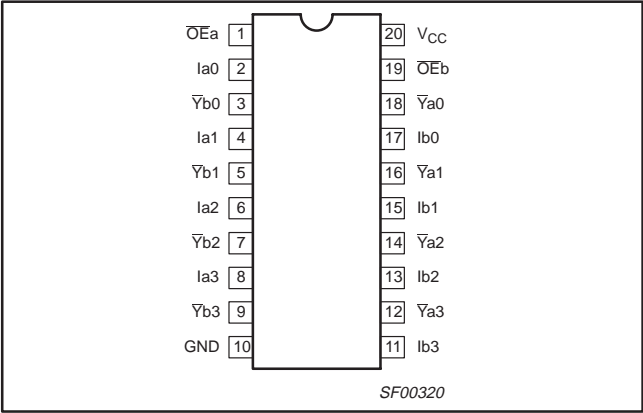
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}a$ , $\overline{OE}b$	Output enable inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{OE}b$	Output enable input (active High, 74F1241)	1.0/0.033	20µA/20µA
Yan, Ybn	Data outputs (74F1241)	750/106.7	15mA/64mA
$\overline{Y}an$ , $\overline{Y}bn$	Data outputs (74F1240)	750/106.7	15mA/64mA

**NOTE:** One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

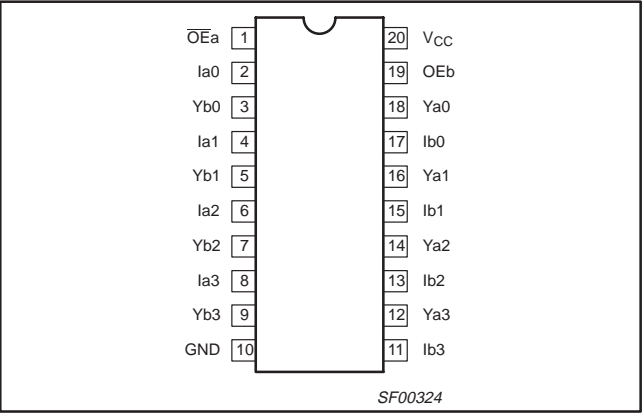
Buffers

74F1240, 74F1241\*

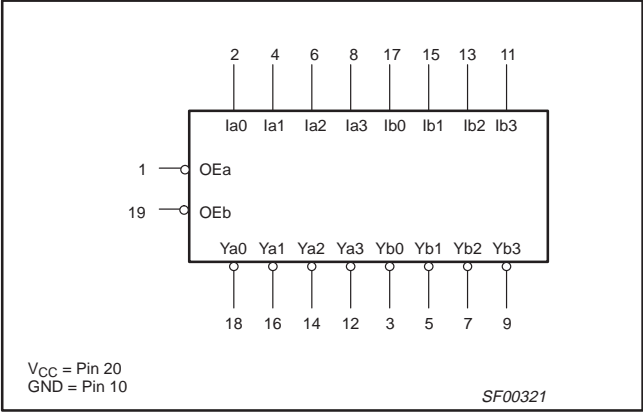
PIN CONFIGURATION – 74F1240



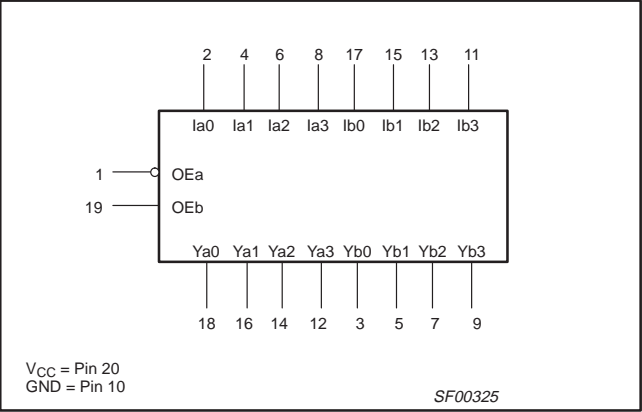
PIN CONFIGURATION – 74F1241



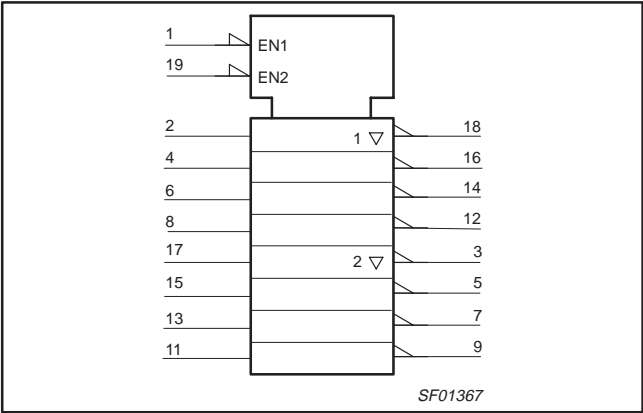
LOGIC SYMBOL – 74F1240



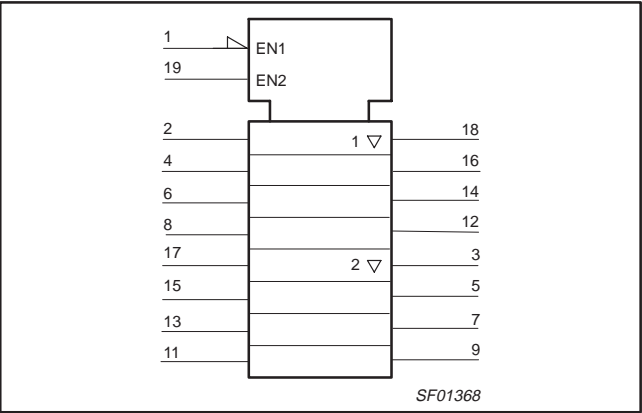
LOGIC SYMBOL – 74F1241



IEC/IEEE SYMBOL – 74F1240



IEC/IEEE SYMBOL – 74F1241

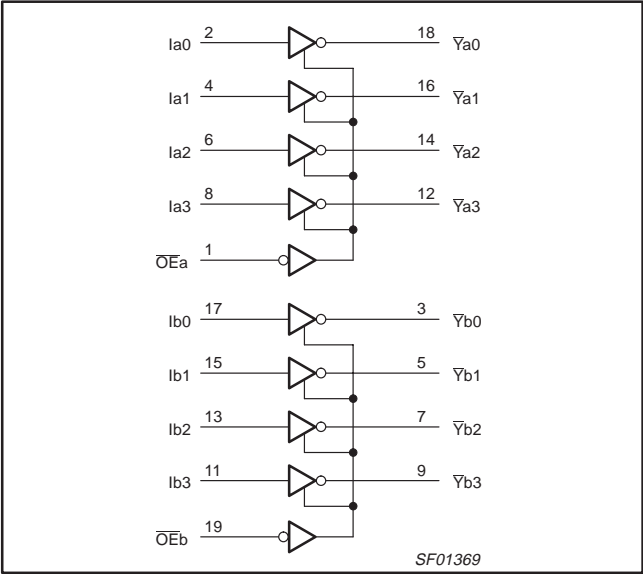


\* Discontinued part. Please see the Discontinued Products List.

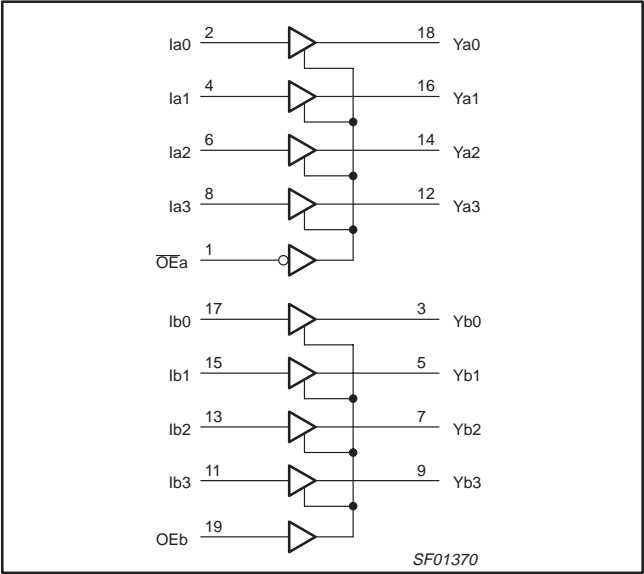
Buffers

74F1240, 74F1241\*

LOGIC DIAGRAM – 74F1240



LOGIC DIAGRAM – 74F1241



FUNCTION TABLE – 74F1240

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	$\overline{OEb}$	Ib	$\overline{Ya}$	$\overline{Yb}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level  
L = Low voltage level  
X = Don't care  
Z = High impedance "off" state

FUNCTION TABLE – 74F1241

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level  
L = Low voltage level  
X = Don't care  
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	−0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	−0.5 to +7.0	V
I <sub>IN</sub>	Input current	−30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	−0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	128	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	−65 to +150	°C

\* Discontinued part. Please see the Discontinued Products List.

## Buffers

## 74F1240, 74F1241\*

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current			64	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>		LIMITS			UNIT
					MIN	TYP	MAX	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	$I_{OH} = -3\text{mA}$	$\pm 10\% V_{CC}$	2.4			V
				$\pm 5\% V_{CC}$	2.7	3.3		V
			$I_{OH} = -15\text{mA}$	$\pm 10\% V_{CC}$	2.0			V
				$\pm 5\% V_{CC}$	2.0			V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	$I_{OL} = 48\text{mA}$	$\pm 10\% V_{CC}$		0.38	0.55	V
			$I_{OL} = 64\text{mA}$	$\pm 5\% V_{CC}$		0.42	0.55	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-0.73	-1.2	V
$I_I$	Input current at maximum input voltage	$V_{CC} = 0.0\text{V}, V_I = 7.0\text{V}$					100	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$					20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$					-20	$\mu\text{A}$
$I_{OZH}$	Off-state output current, High-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$					50	$\mu\text{A}$
$I_{OZL}$	Off-state output current, Low-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$					-50	$\mu\text{A}$
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$			-100		-225	mA
$I_{CC}$	Supply current (total)	74F1240	$I_{CCH}$	$V_{CC} = \text{MAX}$		22	30	mA
			$I_{CCL}$			58	75	mA
			$I_{CCZ}$			44	58	mA
		74F1241	$I_{CCH}$	$V_{CC} = \text{MAX}$		33	44	mA
			$I_{CCL}$			62	80	mA
			$I_{CCZ}$			45	60	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

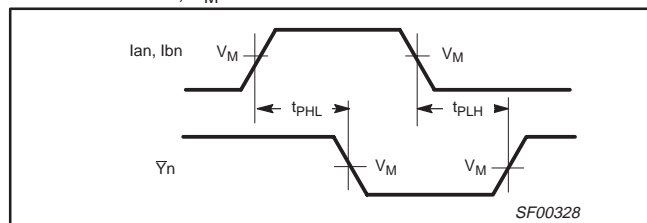
## Buffers

## 74F1240, 74F1241\*

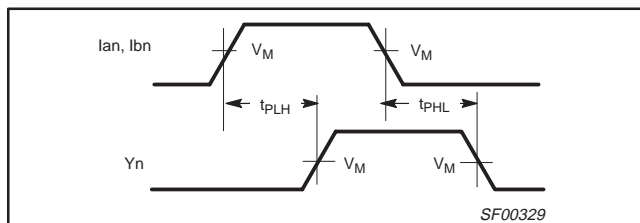
## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> , to Y <sub>n</sub>	74F1240	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	7.5 9.0	3.0 4.0	8.0 9.5	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> , to Y <sub>n</sub>	74F1241	Waveform 2	2.5 2.5	4.0 5.0	5.5 6.5	2.5 2.5	6.0 7.0	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.0	3.0 3.0	7.5 8.5	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 6.0	7.5 8.0	3.0 3.0	8.5 8.5	ns ns

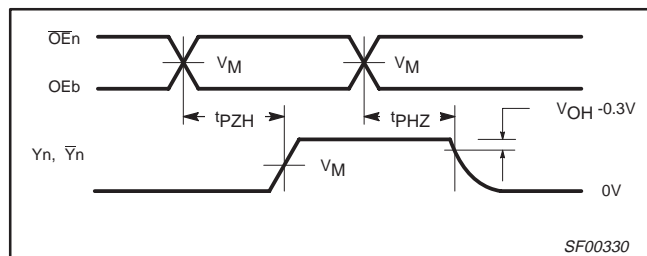
## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.

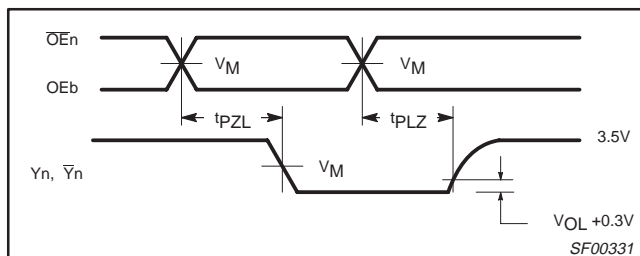
Waveform 1. For Inverting Outputs



Waveform 2. For Non-inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



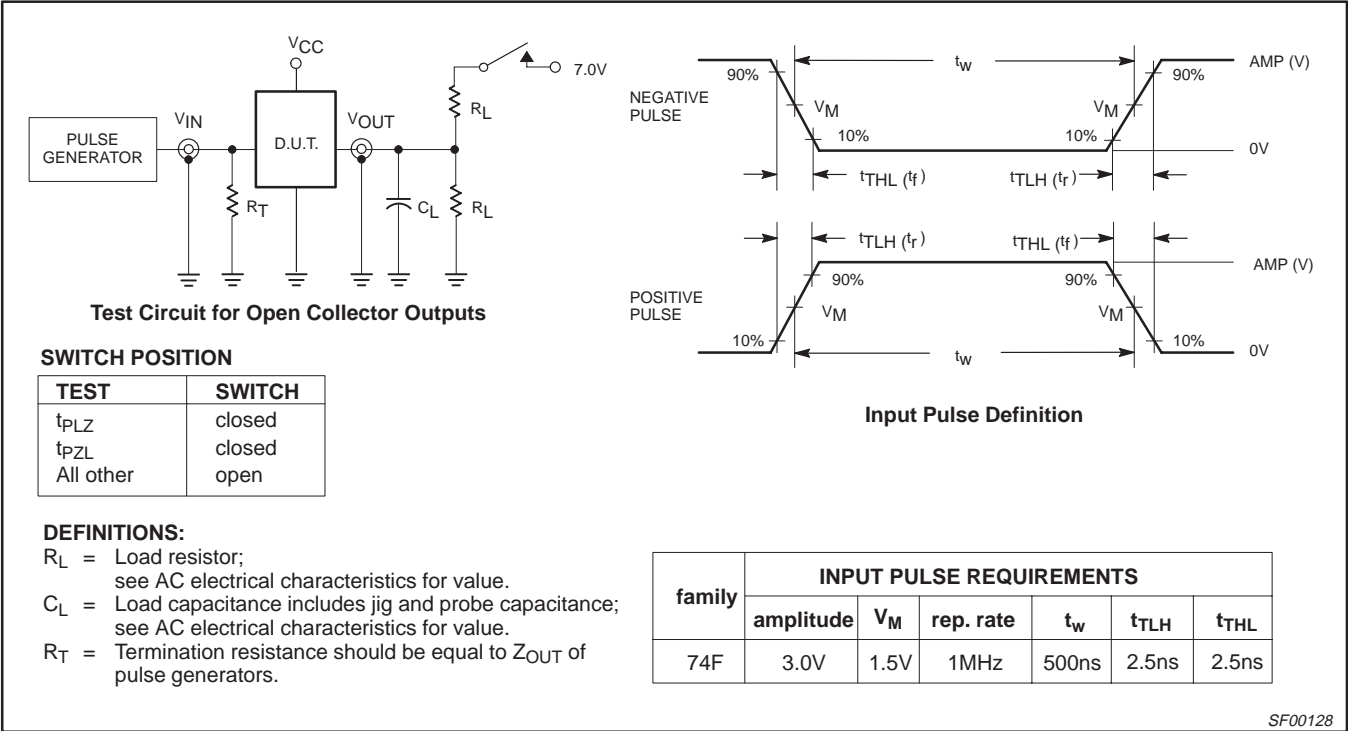
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

\* Discontinued part. Please see the Discontinued Products List.

Buffers

74F1240, 74F1241\*

TEST CIRCUIT AND WAVEFORMS



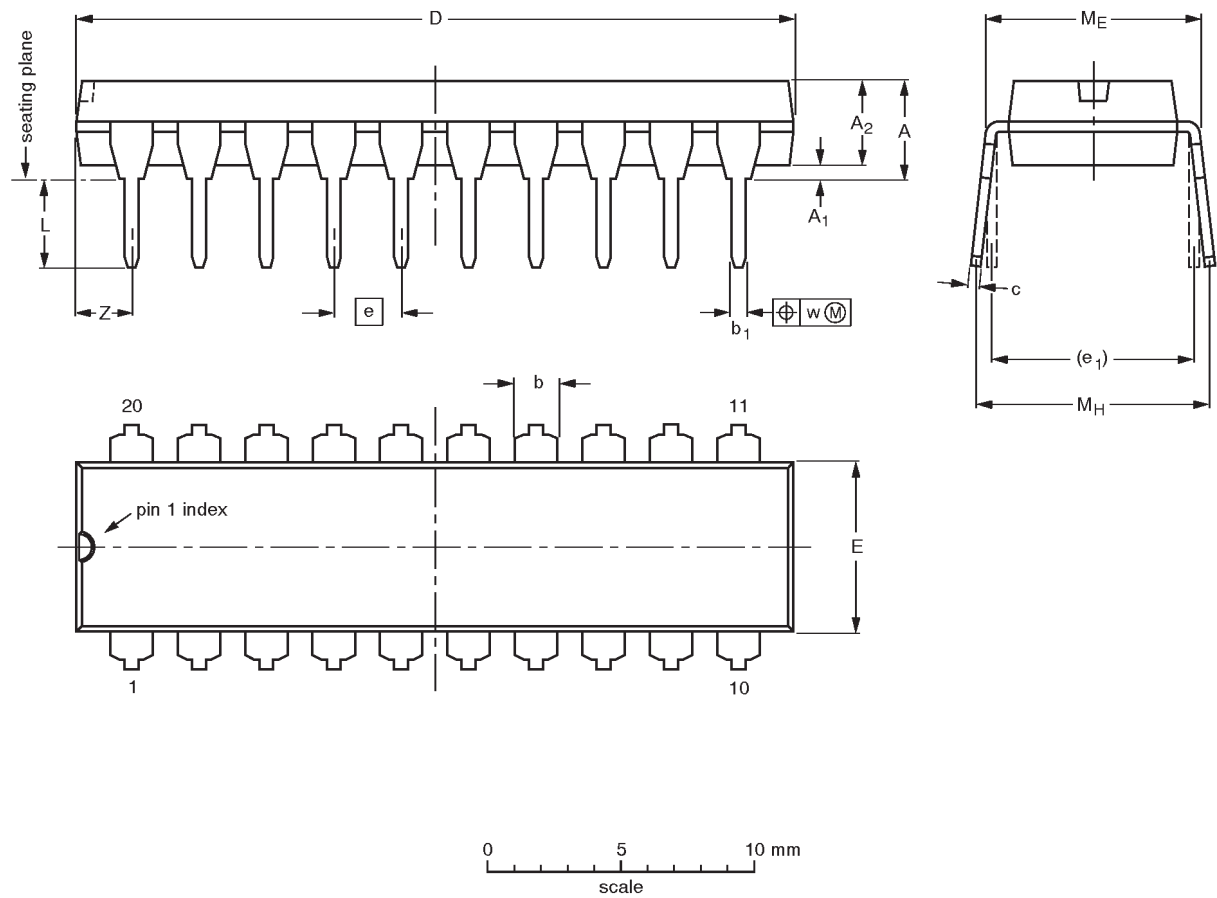
SF00128

Buffers

74F1240, 74F1241\*

DIP20: plastic dual in-line package; 20 leads (300 mil)


SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

\* Discontinued part. Please see the Discontinued Product List.

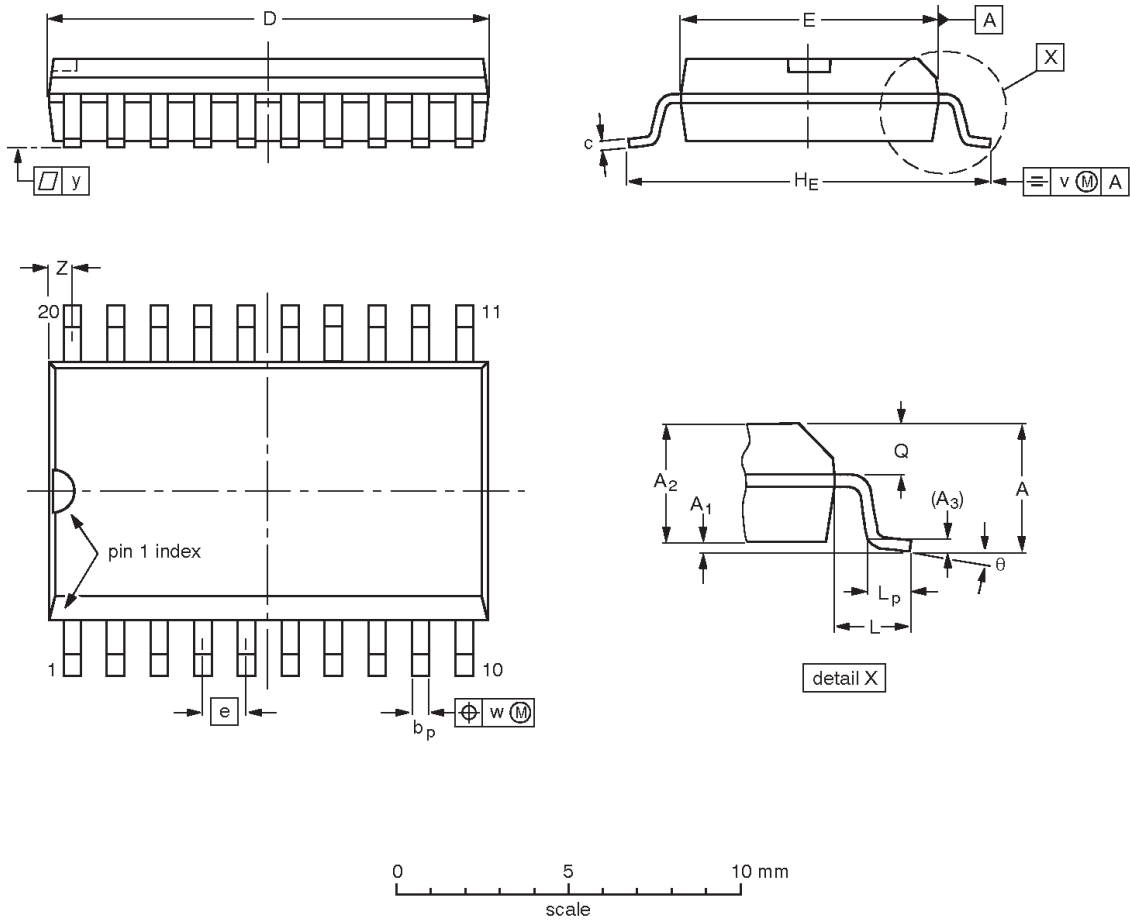


Buffers

74F1240, 74F1241\*

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				-95-01-24 97-05-22

\* Discontinued part. Please see the Discontinued Product List.

## Buffers

74F1240, 74F1241\*

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998  
All rights reserved. Printed in U.S.A.

Date of release: 03-98

Document order number:

9397-750-05191

\* Discontinued part. Please see the Discontinued Product List in Section 1, page 21.

*Let's make things better.*