

DATA SHEET

74F269

8-bit bidirectional binary counter

Product specification

1996 Jan 05

IC15 Data Handbook

8-bit bidirectional binary counter

74F269

FEATURES

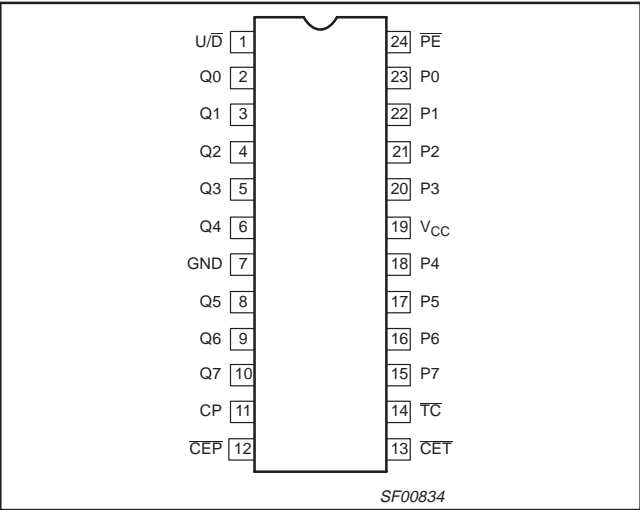
- Synchronous counting and loading
- Built-in look-ahead carry capability
- Count frequency 115MHz typ
- Supply current 95mA typ

DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

TYPE	TYPICAL f _{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V _{CC} = 5V ±10%, T _{amb} = 0°C to +70°C	PKG DWG #
24-Pin Plastic Slim DIP (300mil)	N74F269N	SOT222-1
24-Pin Plastic SOL	N74F269D	SOT137-1
24-Pin Plastic SSOP type II	N74F269DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

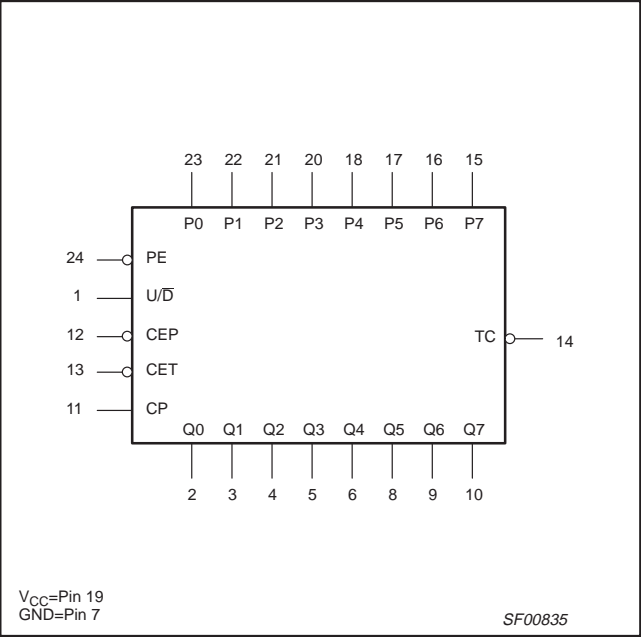
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P0 - P7	Parallel Data inputs	1.0/1.0	20μA/0.6mA
PE	Parallel Enable input (active Low)	1.0/1.0	20μA/0.6mA
U/D	Up/Down count control input	1.0/1.0	20μA/0.6mA
CEP	Count Enable Parallel input (active Low)	1.0/1.0	20μA/0.6mA
CET	Count Enable Trickle input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
TC	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q0 - Q7	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

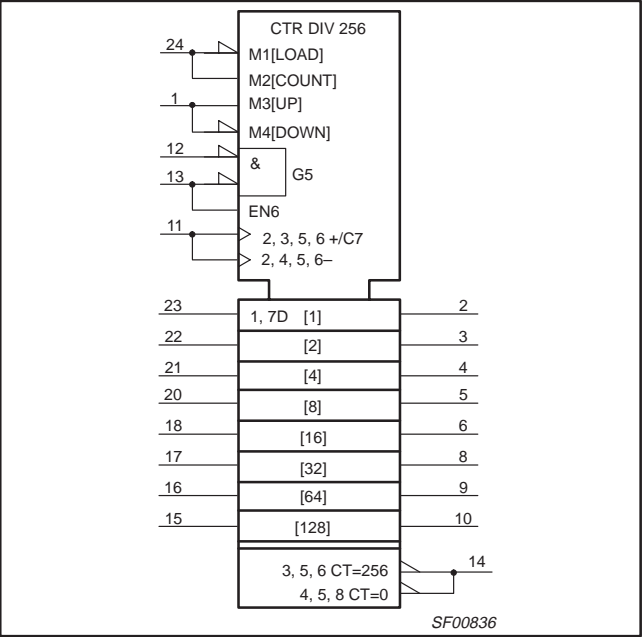
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



APPLICATION

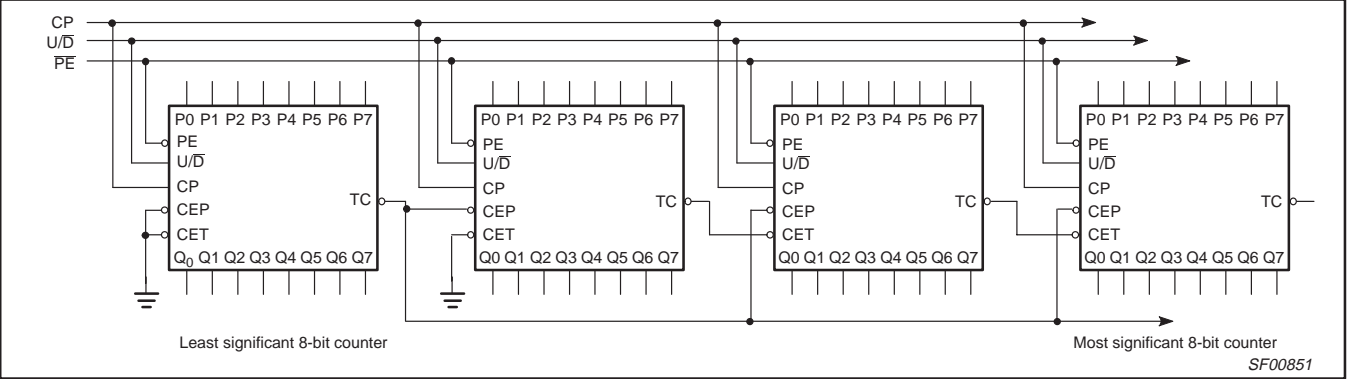


Figure 1. Synchronous Multistage Counting Scheme

MODE SELECT FUNCTION TABLE

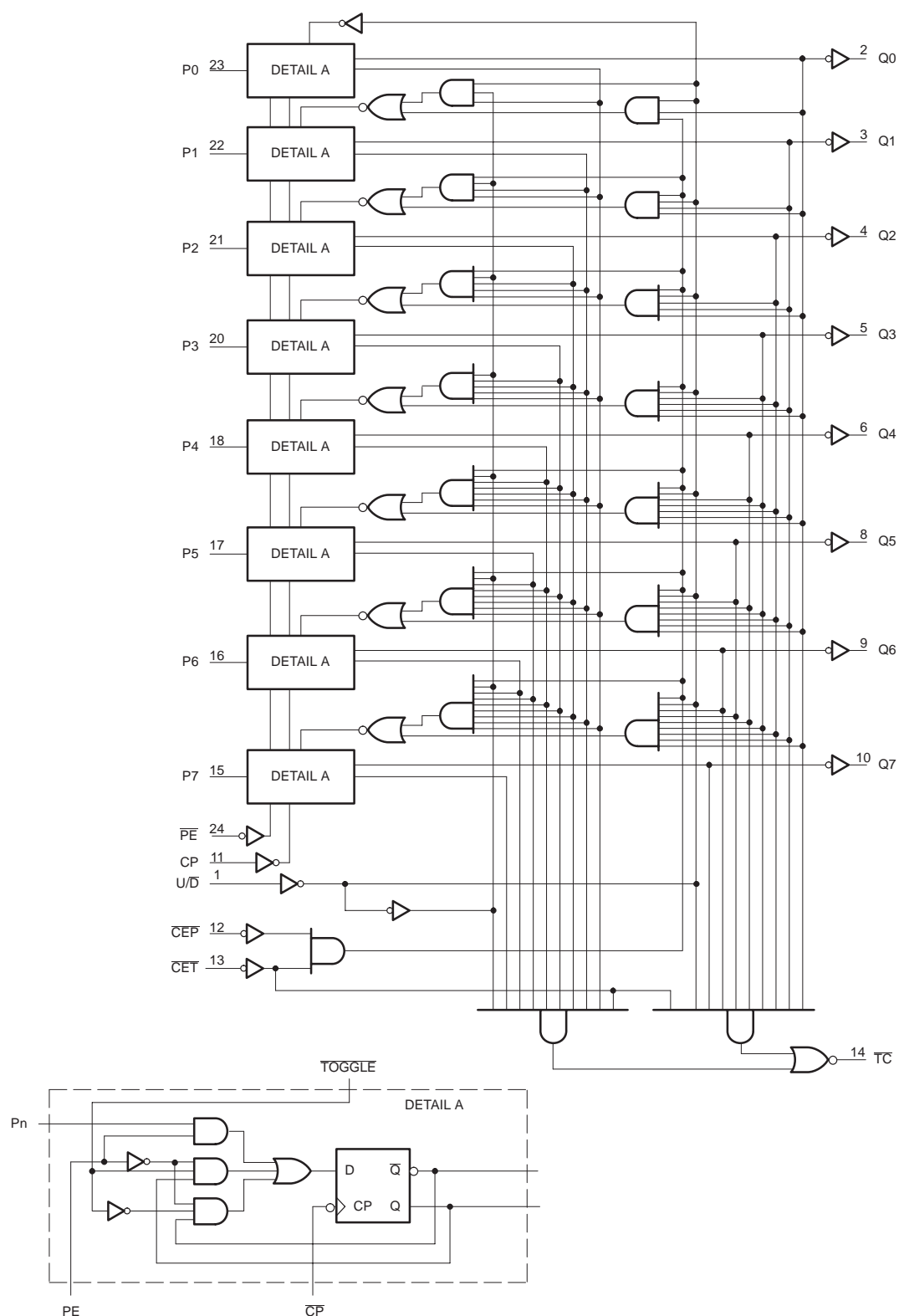
INPUTS						OUTPUTS		OPERATING MODE
CP	U/D	CEP	CET	PE	P _n	Q _n	TC	
↑	X	X	X	l	l	L	(a)	Parallel load
↑	X	X	X	l	h	H	(a)	
↑	h	l	l	h	X	Count Up	(a)	Count Up
↑	l	l	l	h	X	Count Down	(a)	Count Down
↑	X	h	l	h	X	q _n	(a)	Hold (do nothing)
↑	X	X	h	h	X	q _n	H	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(a)= TC is Low when CET is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Q_n outputs Low.

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LOGIC DIAGRAM



V_{CC}=Pin 19
GND=Pin 7

SF00837

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ^{NO TAG}		LIMITS			UNIT
				MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5			V
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.30	0.50	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.30	0.50	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				100	μA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				−0.6	mA
I_{OS}	Short-circuit output current ^{NO TAG}	$V_{CC} = \text{MAX}$		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		93	120	mA
		I_{CCL}	$V_{CC} = \text{MAX}$		98	125	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t _{PLH} t _{pPHL}	Propagation delay CP to Q _n (Load, \overline{PE} = Low)	Waveform 1	3.0 4.0	6.0 6.5	8.5 8.5	3.0 4.0	9.0 9.0	ns ns
t _{PLH} t _{PHL}	Propagation delay CP to Q _n (Count, \overline{PE} = High)	Waveform 1	3.0 4.5	6.0 7.0	9.0 10.0	3.0 4.0	10.0 10.5	ns ns
t _{PLH} t _{PHL}	Propagation delay CP to \overline{TC}	Waveform 1	4.5 5.0	6.5 6.5	9.5 9.5	4.0 5.0	10.5 10.0	ns ns
t _{PLH} t _{PHL}	Propagation delay \overline{CET} to \overline{TC}	Waveform 2	3.5 3.0	6.0 6.5	9.0 9.0	3.0 3.0	10.0 10.0	ns ns
t _{PLH} t _{PHI}	Propagation delay U/D to \overline{TC}	Waveform 3	4.5 4.5	7.0 7.0	9.0 9.5	4.0 4.0	10.0 10.0	ns ns

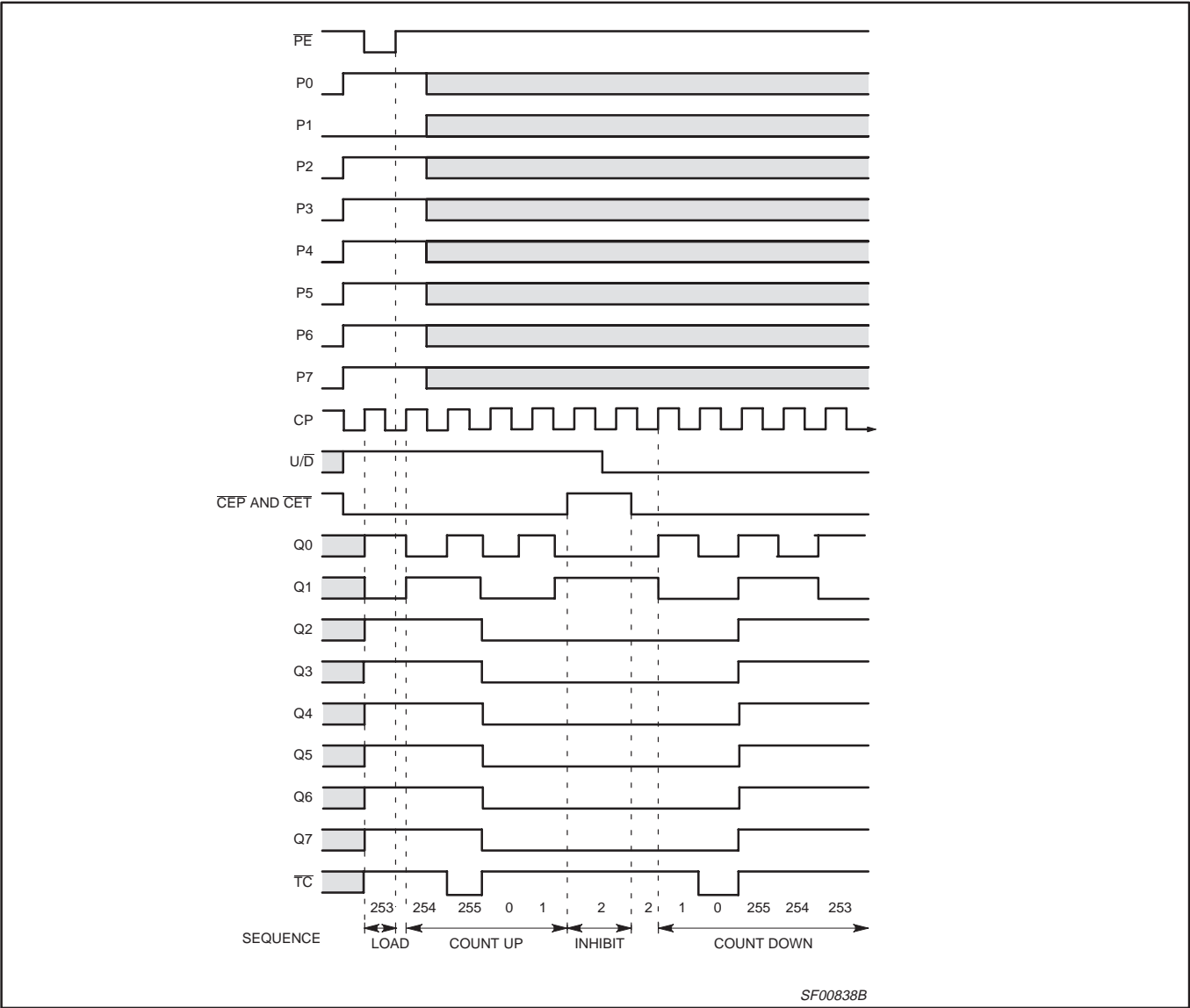
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω		T _{amb} = 0°C to +70°C V _{CC} = +5V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low P _n to CP	Waveform 4	3.5 3.5		2.5 2.5		ns ns
t _h (H) t _h (L)	Hold time, High or Low P _n to CP	Waveform 4	1.0 1.0		0 1.0		ns ns
t _s (H) t _s (L)	Setup time, High or Low PE to CP	Waveform 4	5.5 6.5		5.5 6.5		ns ns
t _h (H) t _h (L)	Hold time, High or Low PE to CP	Waveform 4	0 0		0 0		ns ns
t _s (H) t _s (L)	Setup time, High or Low CEP or CET to CP	Waveform 5	6.0 8.0		5.0 6.5		ns ns
t _h (H) t _h (L)	Hold time, High or Low CEP or CET to CP	Waveform 5	0 0		0 0		ns ns
t _s (H) t _s (L)	Setup time, High or Low U/D to CP	Waveform 6	8.0 6.5		6.5 6.5		ns ns
t _h (H) t _h (L)	Hold time, High or Low U/D to CP	Waveform 6	0 0		0 0		ns ns
t _w (H) t _w (L)	CP Pulse width High or Low	Waveform 1	4.0 4.5		4.0 5.0		ns ns

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TIMING DIAGRAM

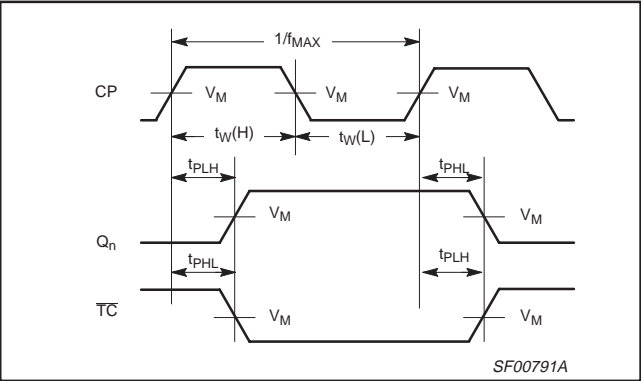


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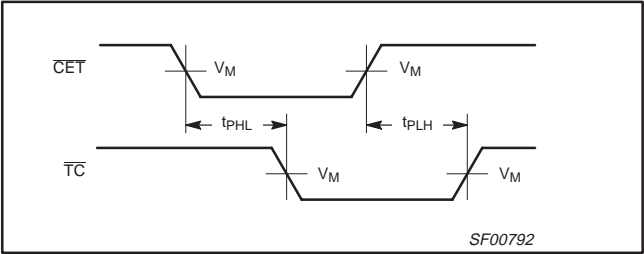
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AC WAVEFORMS

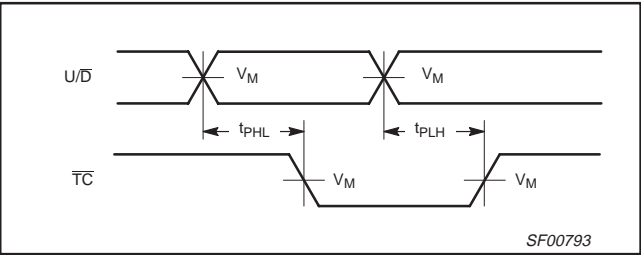
For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.



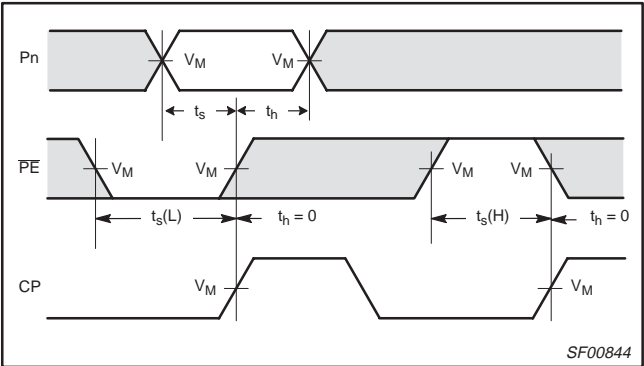
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



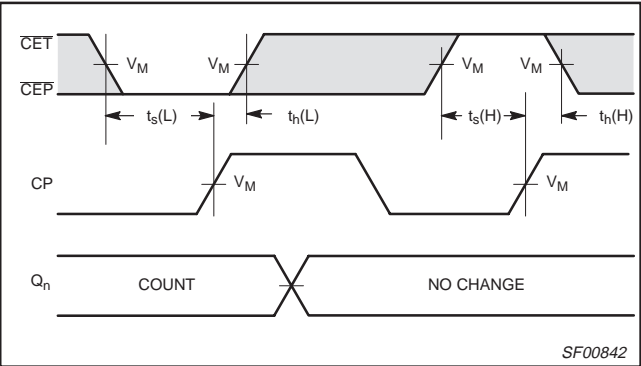
Waveform 2. Propagation Delay, CET Input to Terminal Count Output



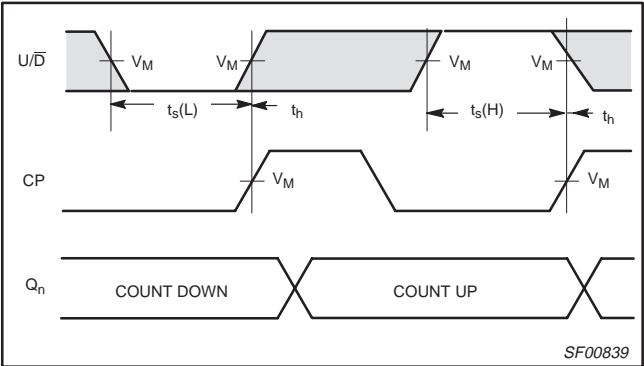
Waveform 3. Propagation Delay, Up/Down Count Control Input to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times



Waveform 5. Count Enables Setup and Hold Times

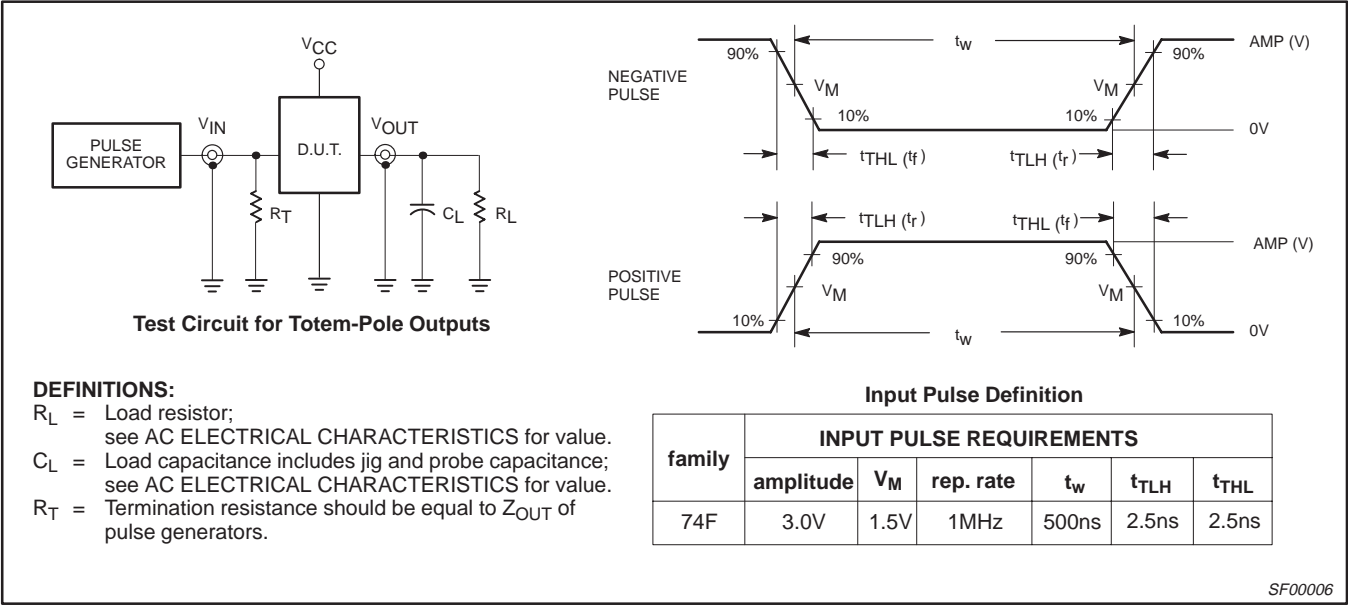


Waveform 6. Up/Down Count Control Setup and Hold Times

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TEST CIRCUIT AND WAVEFORMS

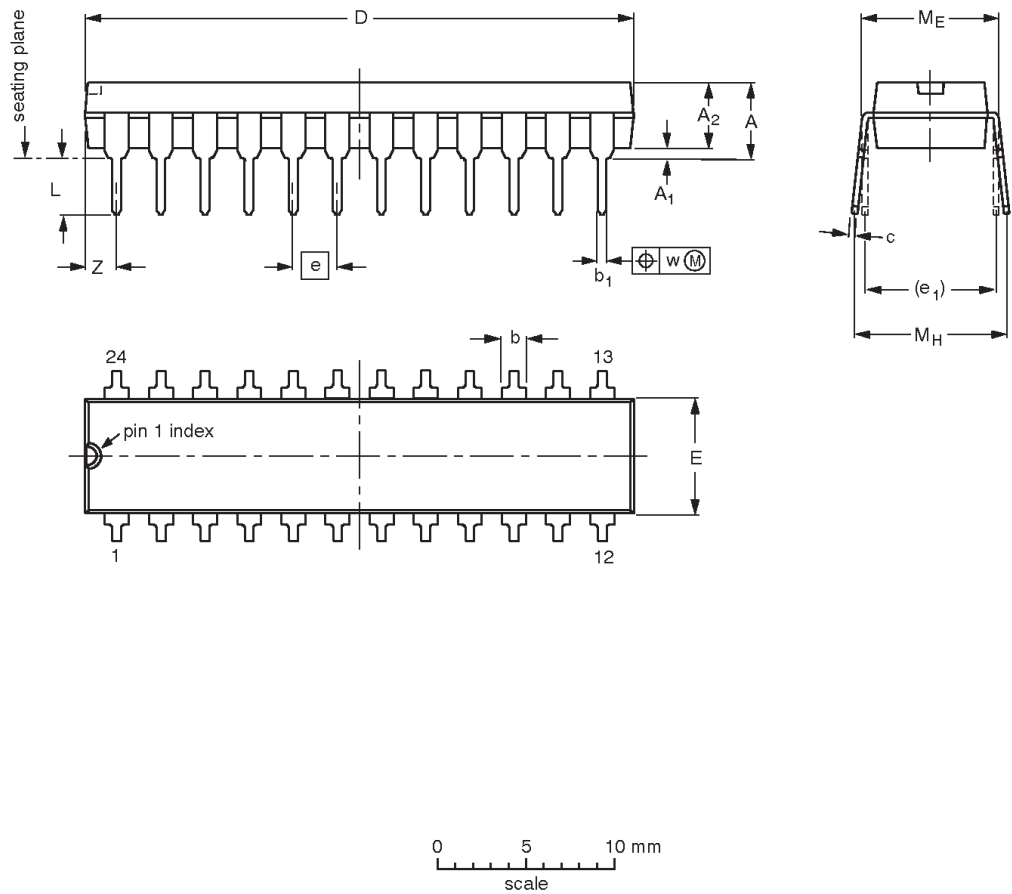


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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

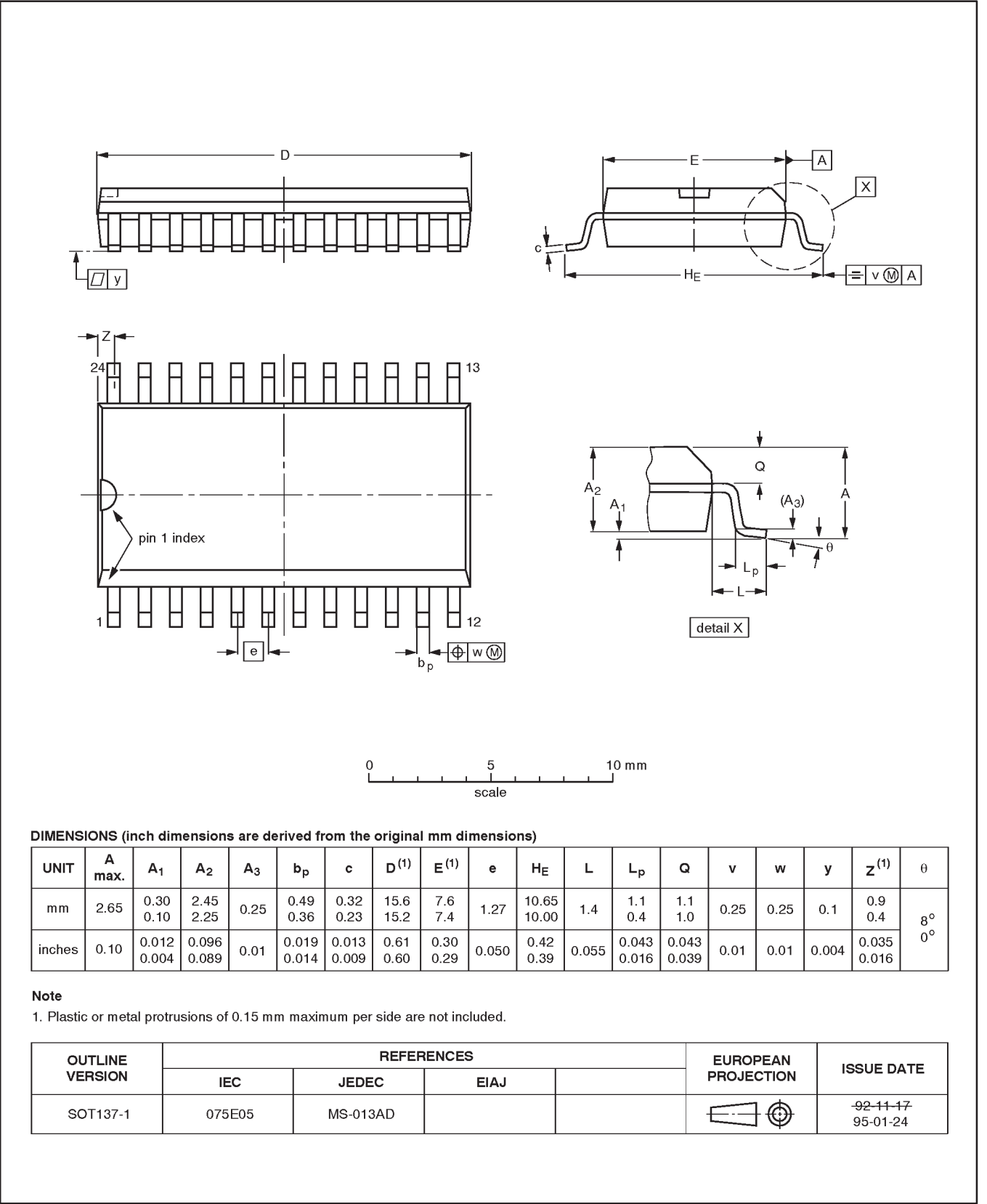
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

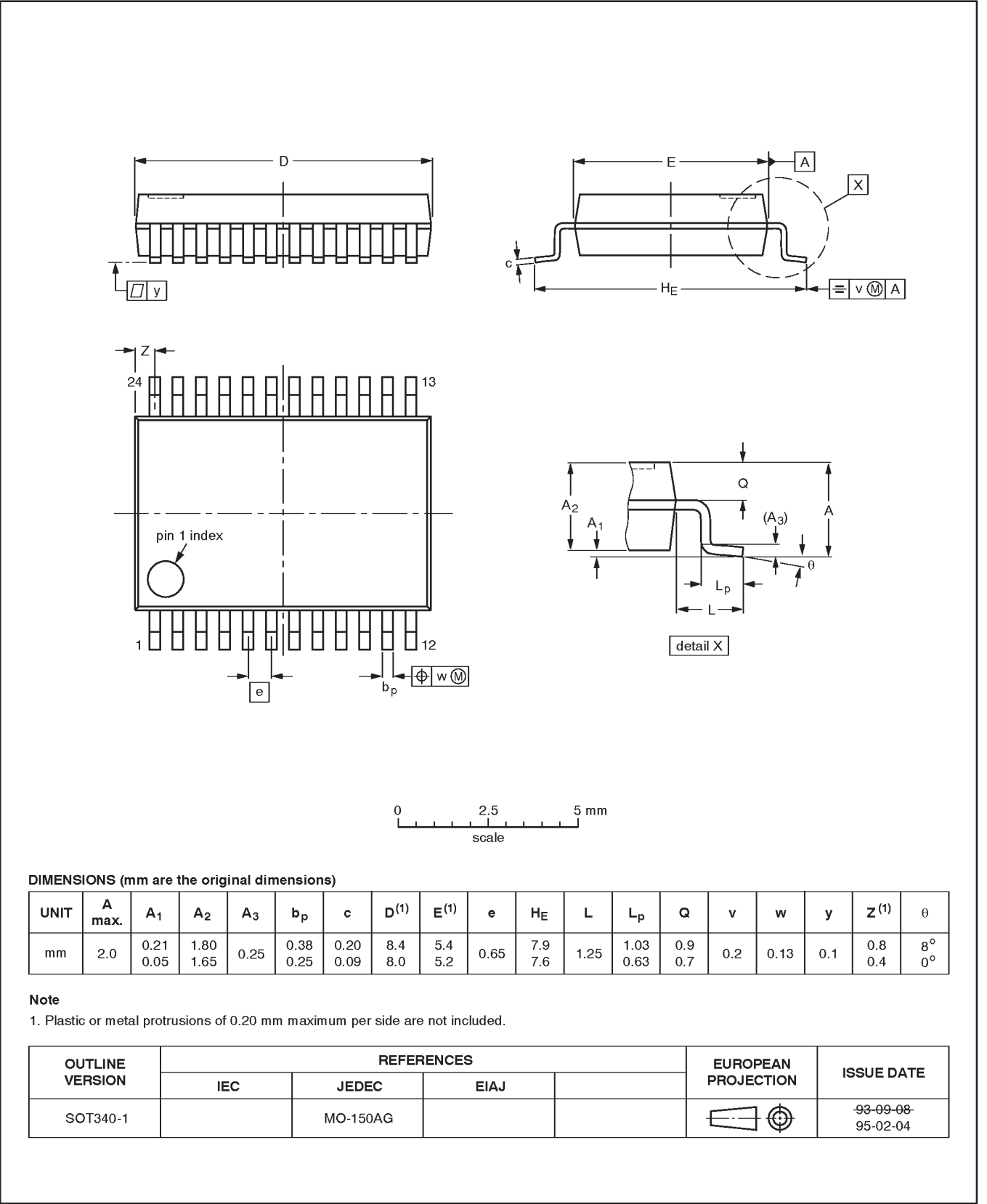


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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



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NOTES

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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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