

# DATA SHEET

**NE56610/11/12-XX**

**System reset**

Product data  
Supersedes data of 2001 Apr 24  
File under Integrated Circuits, Standard Analog

2001 Jun 19

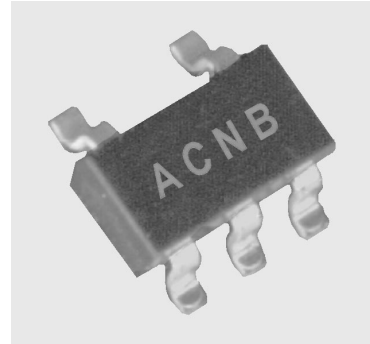
# System reset

## NE56610/11/12-XX

### GENERAL DESCRIPTION

The NE56610/11/12-XX series is a family of devices designed to generate a reset signal for a variety of microprocessor and logic systems. Accurate reset signals are generated during momentary power interruptions or when ever power supply voltages sag to intolerable levels. The NE56610/11/12 incorporates an internal timer to provide reset delay and ensure proper operating voltage has been attained. In addition, a manual reset pin (M/R) is available. An Open Collector output topology provides adaptability for a wide variety of logic and microprocessor systems.

NE56610/11/12 is available in the SOT23-5 surface mount package.



### FEATURES

- 12 V<sub>DC</sub> maximum operating voltage
- Low operating voltage (0.65 V)
- Manual Reset input
- SOT23-5 surface mount package
- Offered in reset thresholds of 2.5, 2.7, 2.9, 3.9, 4.2, 4.5 V<sub>DC</sub>
- Internal reset delay timer
  - NE56610 (50 ms typical)
  - NE56611 (100 ms typical)
  - NE56612 (200 ms typical)

### APPLICATIONS

- Microcomputer systems
- Logic systems
- Battery monitoring systems
- Back-up power supply circuits
- Voltage detection circuits
- Mechanical reset circuits

### SIMPLIFIED DEVICE DIAGRAM

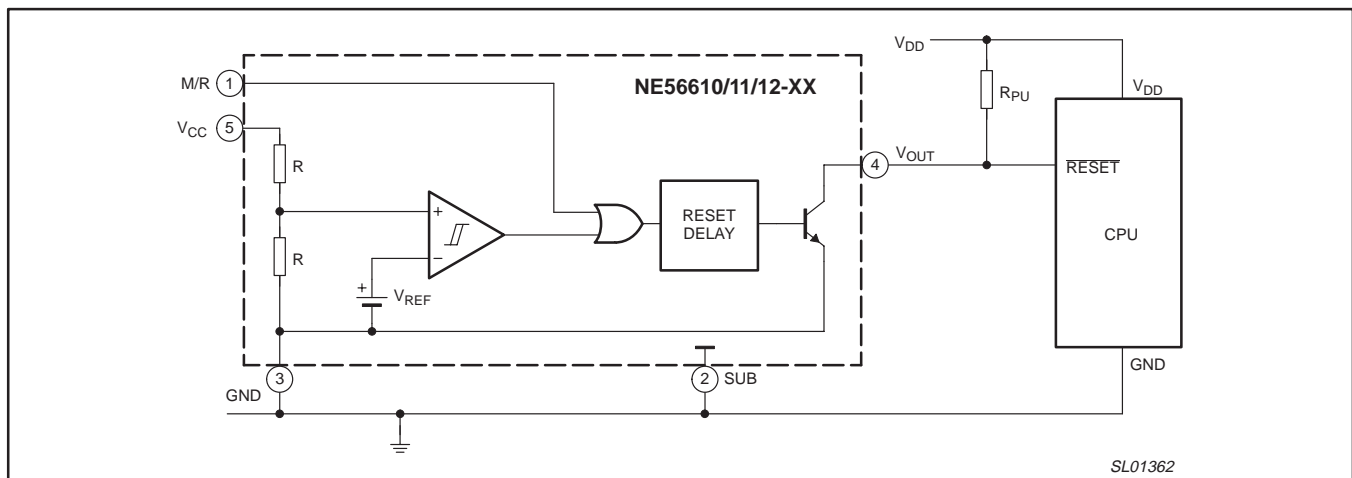


Figure 1. Simplified device diagram.

## System reset

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## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE	TYPICAL RESET DELAY
	NAME	DESCRIPTION		
NE56610-XXGW	SOT23-5, SOT25, SO5	plastic small outline package; 5 leads (see dimensional drawing)	–20 to +75 °C	50 ms
NE56611-XXGW	SOT23-5, SOT25, SO5	plastic small outline package; 5 leads (see dimensional drawing)	–20 to +75 °C	100 ms
NE56612-XXGW	SOT23-5, SOT25, SO5	plastic small outline package; 5 leads (see dimensional drawing)	–20 to +75 °C	200 ms

**NOTE:**

Each device has six detection voltage options, indicated by the XX on the 'Type number'.

XX	DETECT VOLTAGE (Typical)
25	2.5 V
27	2.7 V
29	2.9 V
39	3.9 V
42	4.2 V
45	4.5 V

## Part number marking

Each device is marked with a four letter code. The first three letters designate the product. The fourth letter, represented by 'x', is a date tracking code. For example, ACNB is device ACN (the NE56610-25 reset) produced in time period 'B'.

Part number	Marking	Part number	Marking	Part number	Marking
NE56610-25	A C N x	NE56611-25	A C V x	NE56612-25	A C B x
NE56610-27	A C M x	NE56611-27	A C U x	NE56612-27	A C A x
NE56610-29	A C L x	NE56611-29	A C T x	NE56612-29	A C Z x
NE56610-39	A C K x	NE56611-39	A C S x	NE56612-39	A C Y x
NE56610-42	A C J x	NE56611-42	A C R x	NE56612-42	A C X x
NE56610-45	A C H x	NE56611-45	A C P x	NE56612-45	A C W x

## PIN CONFIGURATION

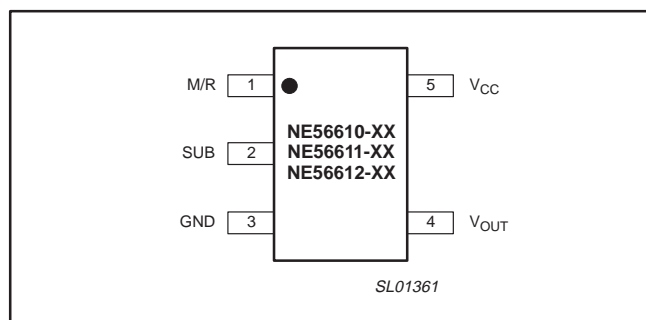


Figure 2. Pin configuration.

## PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	M/R	Manual Reset input. Connect to ground when not using.
2	SUB	Substrate pin. Connect to ground.
3	GND	Ground
4	V <sub>OUT</sub>	Reset HIGH output pin
5	V <sub>CC</sub>	Positive power supply input

## MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>CC</sub>	Power supply voltage	–0.3	12	V
V <sub>M/R</sub>	Manual Reset input voltage	–0.3	12	V
T <sub>amb</sub>	Operating ambient temperature	–20	75	°C
T <sub>stg</sub>	Storage temperature	–40	125	°C
P	Power dissipation	–	150	mW

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**ELECTRICAL CHARACTERISTICS**

Characteristics noted with M/R pin connected to ground. Typical values reflect appropriate average value at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	TEST CIRCUIT	PART #	MIN.	TYP.	MAX.	UNIT
$V_S$	Threshold detection	$V_{CC}$ falling; $R_L = 470\ \Omega$ ; $V_{OL} \leq 0.4\text{ V}$	1 Fig. 20	–45	4.3	4.5	4.7	V
				–42	4.0	4.2	4.4	V
				–39	3.7	3.9	4.1	V
				–29	2.75	2.90	3.05	V
				–27	2.55	2.70	2.85	V
				–25	2.35	2.50	2.65	V
$\Delta V_S$	Hysteresis	$\Delta V_S = V_{SH} \text{ (rising } V_{CC}) - V_{SL} \text{ (falling } V_{CC})$ ; $R_L = 470\ \Omega$		All	30	50	100	mV
$\Delta T_C / \Delta V_S$	Threshold temperature coefficient	$R_L = 470\ \Omega$ ; $-20\text{ }^{\circ}\text{C} \leq T_{amb} \leq +75\text{ }^{\circ}\text{C}$		All	–	$\pm 0.01$	–	%/ $^{\circ}\text{C}$
$V_{OL}$	LOW-level output voltage	$V_{CC} = V_{S(min)} - 0.05\text{ V}$ ; $R_L = 470\ \Omega$		All	–	0.01	0.4	V
$I_{LO}$	Output leakage current	$V_{CC} = 10\text{ V}$		All	–	–	$\pm 0.1$	$\mu\text{A}$
$I_{CCL}$	Circuit current (output LOW)	$V_{CC} = V_{S(min)} - 0.05\text{ V}$ ; $R_L = \infty$		All	–	300	500	$\mu\text{A}$
$I_{CCH}$	Circuit current (output HIGH)	$V_{CC} = V_{S(typ)} / 0.85\text{ V}$ ; $R_L = \infty$		All	–	15	25	$\mu\text{A}$
$t_{DLH}$	Reset delay time HIGH (Note 1)	$R_L = 4.7\text{ k}\Omega$ ; $C_L = 100\text{ pF}$	2 Fig. 21	NE56610	30	50	75	ms
				NE56611	60	100	150	ms
				NE56612	120	200	300	ms
$t_{DHL}$	Reset delay time LOW (Note 2)	$R_L = 4.7\text{ k}\Omega$ ; $C_L = 100\text{ pF}$		All	–	20	–	$\mu\text{s}$
$V_{OPL}$	Operating supply voltage	$R_L = 4.7\text{ k}\Omega$ ; $V_{OL} \leq 0.4\text{ V}$	1 Fig. 20	All	–	0.65	0.85	V
$I_{OL1}$	Output sink current 1	$V_{CC} = V_{S(min)} - 0.05\text{ V}$ ; $R_L = 0$		All	–8.0	–	–	mA
$I_{OL2}$	Output sink current 2	$V_{CC} = V_{S(min)} - 0.05\text{ V}$ ; $R_L = 0$ ; $-20\text{ }^{\circ}\text{C} \leq T_{amb} \leq +75\text{ }^{\circ}\text{C}$		All	–6.0	–	–	mA
$V_{M/RH}$	HIGH-level M/R threshold voltage (Note 3)			All	2.0	–	–	V
$I_{M/RH}$	HIGH-level M/R threshold current	$V_{M/RH} = 2.0\text{ V}$		All	–	10	60	$\mu\text{A}$
$V_{M/RL}$	LOW-level M/R threshold voltage			All	–0.3	–	0.8	V
$t_{M/R}$	M/R pulse width (Note 4)			All	15	–	–	$\mu\text{s}$

**NOTES:**

- $t_{DLH}$  measured with  $V_{CC} = (V_{S(typ)} - 0.4\text{ V})$  and abruptly transitioning to  $(V_{S(typ)} + 0.4\text{ V})$ .  $t_{DLH}$  is the duration from  $V_{CC}$  transition HIGH to output transition HIGH.
- $t_{DHL}$  measured with  $V_{CC} = (V_{S(typ)} + 0.4\text{ V})$  and abruptly transitioning to  $(V_{S(typ)} - 0.4\text{ V})$ .  $t_{DHL}$  is the duration from  $V_{CC}$  transition LOW to output transition LOW.
- Ramp M/R voltage until output RESET goes LOW.
- Minimum M/R pulse width for detection.

System reset

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TYPICAL PERFORMANCE CURVES

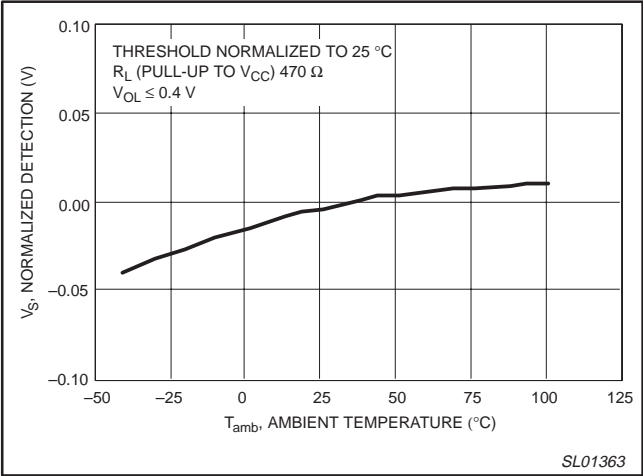


Figure 3. Normalized detection versus temperature.

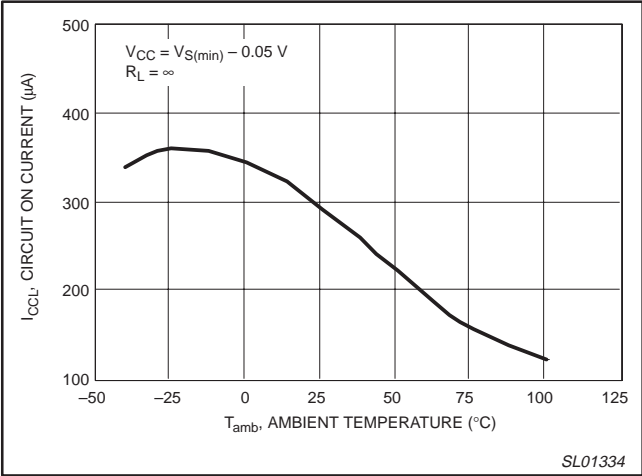


Figure 4. Circuit ON current versus temperature.

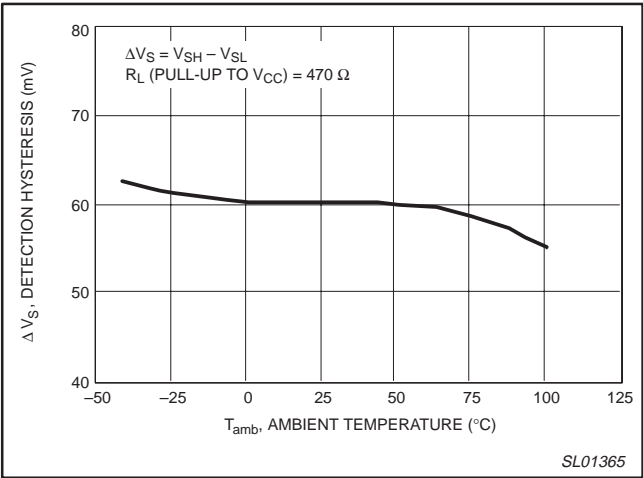


Figure 5. Detection hysteresis versus temperature.

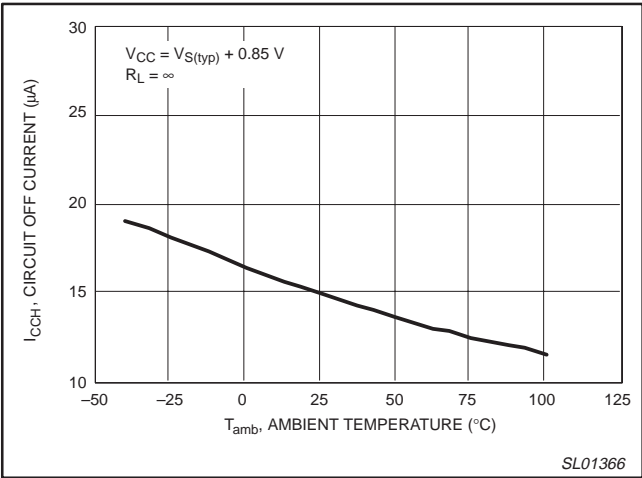


Figure 6. Circuit OFF current versus temperature.

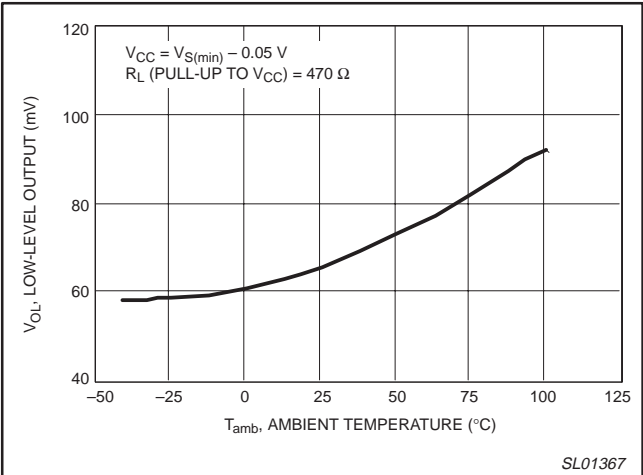


Figure 7. LOW-level output voltage versus temperature.

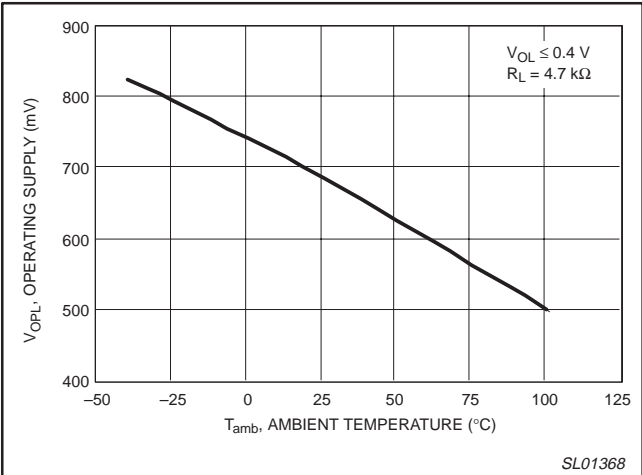


Figure 8. Operating supply voltage versus temperature.

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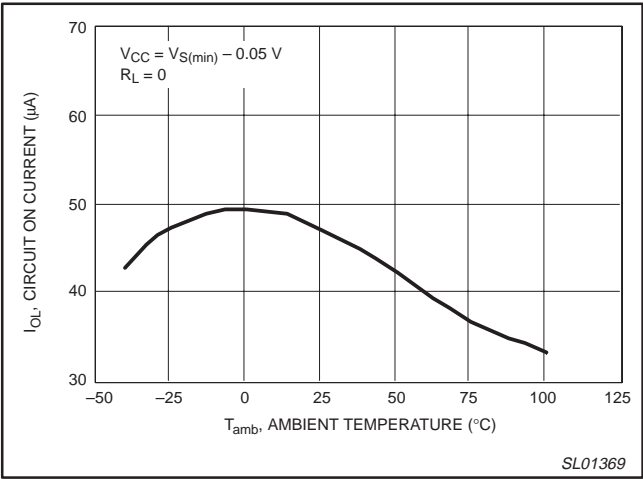


Figure 9. Output ON current versus temperature.

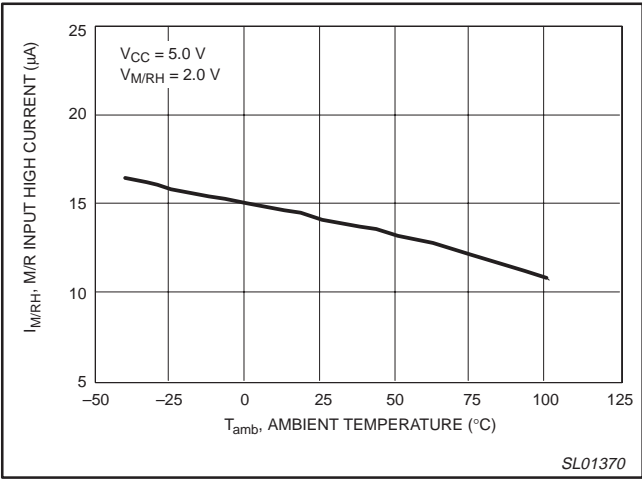


Figure 10. M/R input HIGH current versus temperature.

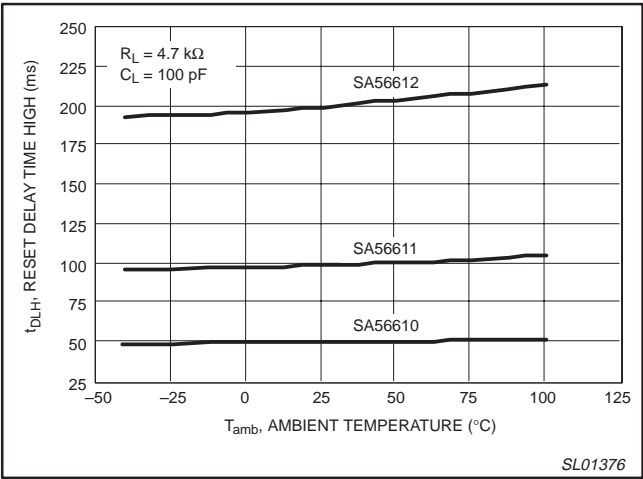


Figure 11. Reset delay time HIGH versus temperature.

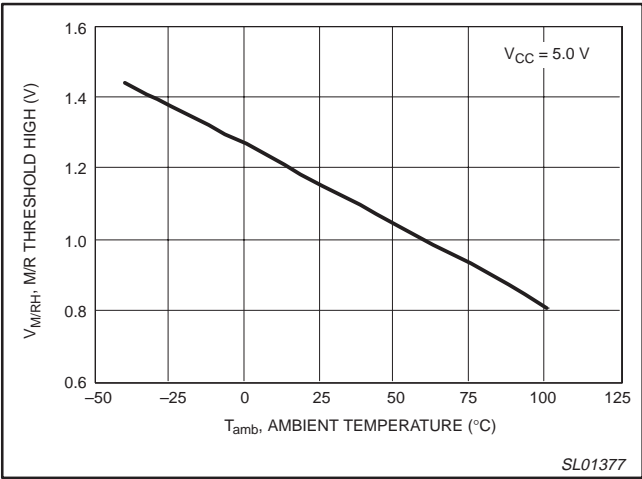


Figure 12. M/R threshold HIGH versus temperature.

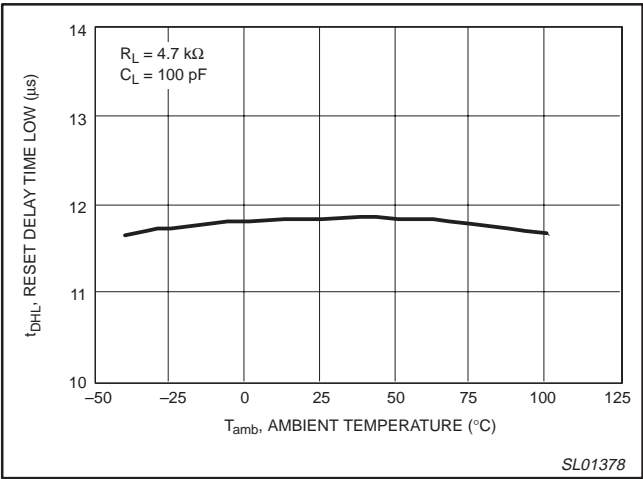


Figure 13. Reset delay time LOW versus temperature.

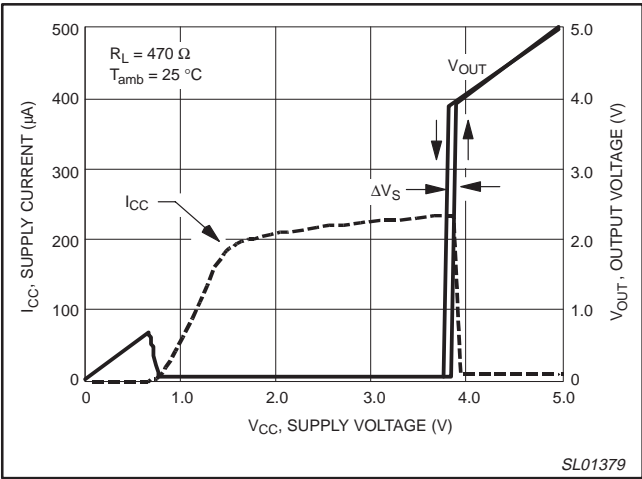


Figure 14.  $I_{CC}$  and  $V_{OUT}$  versus supply voltage.

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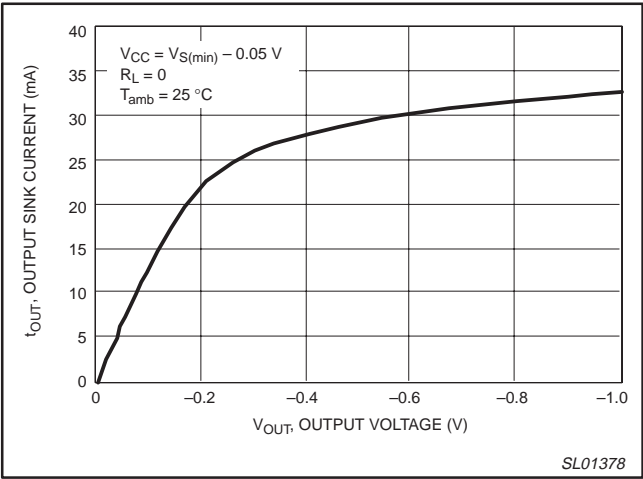


Figure 15. Output sink current versus output voltage.

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## TECHNICAL DESCRIPTION

The NE56610/11/12-XX devices comprise a family of devices designed to monitor the supply voltage and output a  $\overline{\text{RESET}}$  signal whenever the supply voltage sags below an acceptable system level or when supply voltage interruptions occur. Each of the three devices of the family are available with a fixed detection threshold voltage (2.5, 2.7, 2.9, 3.9, 4.2, 4.5 V). The device family is very versatile and adaptable for a wide variety of applications.

The devices are designed to have a detection threshold hysteresis of 50 mV typical. When the supply voltage delivered to the device falls to the detection sense level ( $V_S$ ), a  $\overline{\text{RESET}}$  is output and not released until the supply voltage rises to the level of  $V_S$  or greater. These levels are termed  $V_L$  (synonymous with  $V_S$ ) and  $V_H$ , and the difference of  $V_H - V_L = V_{HYS}$  (the hysteresis voltage value).

Internally, the devices incorporate a fixed internal digital timer which, when activated, produces a fixed internal delay before a  $\overline{\text{RESET}}$  signal is output. This delay can not be influenced externally. The NE56510 has an internal delay of 50 ms, while the NE56611 and NE56612 have internal delays of 100 ms and 200 ms respectively.

Incorporating a delay in the output  $\overline{\text{RESET}}$  prevents output oscillations from occurring and helps ensure system supply voltages are adequate and stabilized before the microprocessor is placed into full operation. Where there is little or no delay in output  $\overline{\text{RESET}}$ , there is a possibility of output oscillations occurring, particularly where high impedance supply sources are used.

In addition, the devices have a manual reset (M/R) pin, which when pulled to a HIGH voltage state, forces a  $\overline{\text{RESET}}$  signal at the output. The M/R pin should always be connected to ground when manual reset is not used.

The output of the NE56610/11/12 utilizes a low side open collector topology, requiring the user to use an external pull-up resistor ( $R_{PU}$ ) to the  $V_{CC}$  power source. Although this may be regarded as a disadvantage, it is an advantage in many sensitive applications. The open drain output topology does not have the capability of sourcing reset current to a microprocessor when both are operated from a common supply. It is for this reason the device family offers a safe inter-connect to a wide variety of microprocessors.

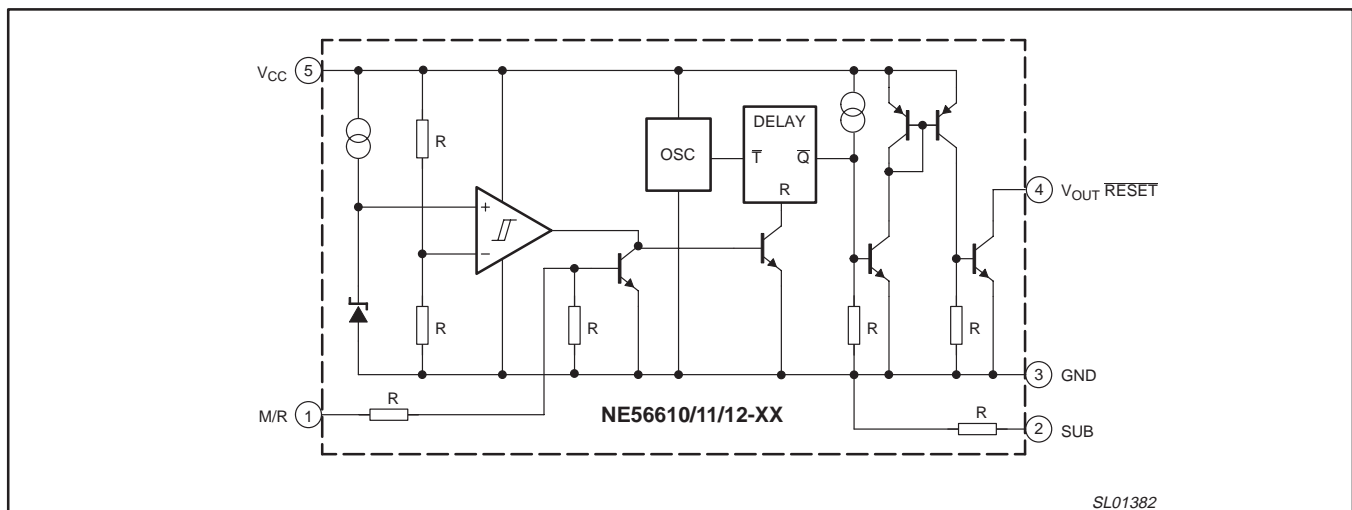


Figure 16. Functional diagram



## System reset

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## TIMING DIAGRAM

The Timing Diagram shown in Figure 17 depicts the operation of the device. Letters indicate events on the TIME axis.

**A:** At start-up, event 'A', the  $V_{CC}$  and  $V_{OUT}$  ( $\overline{RESET}$ ) voltages begin to rise. The reset voltage initially starts to rise but then abruptly returns to a LOW voltage state. This is due to  $V_{CC}$  reaching a level (approximately 0.8 V) which activates the internal bias circuitry asserting a RESET state at  $V_{OUT}$ .

**B:** At event 'B', the fixed internal delay time ( $t_{DLH}$ ) is initiated. This is caused and coincident to  $V_{CC}$  rising to the threshold level of  $V_{SH}$ . At this level the device is in full operation. The output remains in a low voltage state as  $V_{CC}$  rises above  $V_{SH}$ . This is normal.

**C:** At event 'C',  $V_{CC}$  is above the undervoltage detection threshold ( $V_{SL}$ ) and the fixed internal delay time ( $t_{DLH}$ ) has elapsed. At this instant the device releases the hold on  $V_{OUT}$  and  $V_{OUT}$  ( $\overline{RESET}$ ) goes to a high state.

In a microprocessor-based system these events remove the reset from the microprocessor, allowing the microprocessor to be fully functional.

**D-E:** At event 'D',  $V_{CC}$  begins to ramp down and  $V_{OUT}$  follows.  $V_{CC}$  continues to fall until the undervoltage threshold ( $V_{SL}$ ) is reached at 'E'. This causes the device to generate a reset signal.

**E-F:** Between 'E' and 'F',  $V_{CC}$  recovers and starts to rise.

**F:** At event 'F',  $V_{CC}$  reaches the upper threshold ( $V_{SH}$ ). Once again, the  $t_{DLH}$  fixed internal delay time is initiated.

**G:** At event 'G',  $V_{CC}$  is above the  $V_{SL}$  undervoltage detection voltage and the  $t_{DLH}$  fixed internal delay time has elapsed. At this point the device releases the hold on  $V_{OUT}$  and  $V_{OUT}$  goes to a HIGH state.

**H-K:** At event 'H',  $V_{CC}$  is normal, but a manual reset voltage (HIGH voltage state) has been applied to the M/R pin. This forces the output into a reset (LOW voltage state). Removal of the manual reset voltage, at 'J', from the M/R pin initiates the fixed internal delay time, and at 'K', the internal delay time has elapsed and  $V_{OUT}$  goes to a HIGH voltage state.

**L:** At event 'L',  $V_{CC}$  sags to the  $V_{SL}$  undervoltage threshold level and the output goes into low voltage reset condition.

**M:** At event 'M', the  $V_{CC}$  voltage has deteriorated to a level where normal internal circuit bias is no longer able to maintain the device and  $V_{OUT}$  reset assertion is no longer be guaranteed. As a result,  $V_{OUT}$  may exhibit a slight rise to something less than 0.8 V. As  $V_{CC}$  decays even further,  $V_{OUT}$  reset also decays to zero.

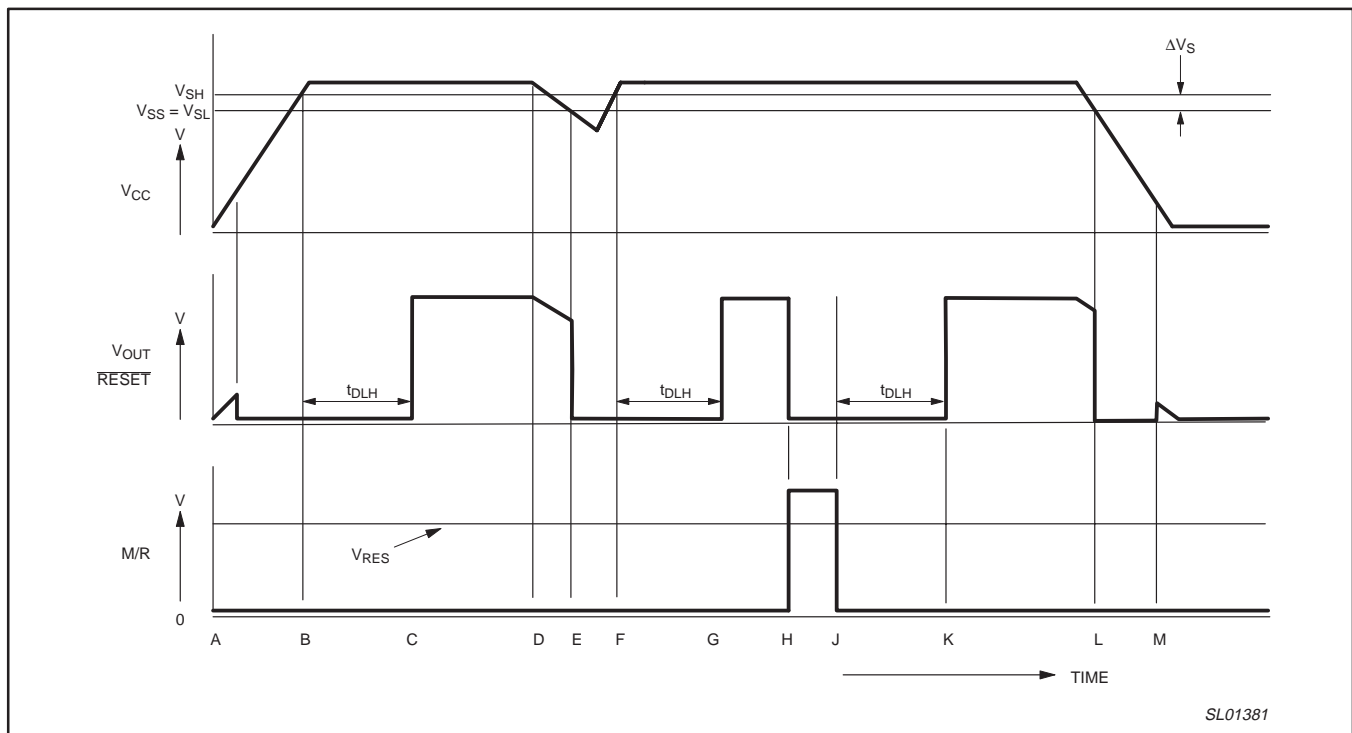


Figure 17. Timing diagram.

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## APPLICATION INFORMATION

When the manual reset is not needed, the M/R, manual reset pin is connected to ground as shown in Figure 18. A capacitor connected from  $V_{CC}$  to ground is recommended when the  $V_{CC}$  supply impedance is appreciably high. This may be the situation with a poor quality or aged battery.

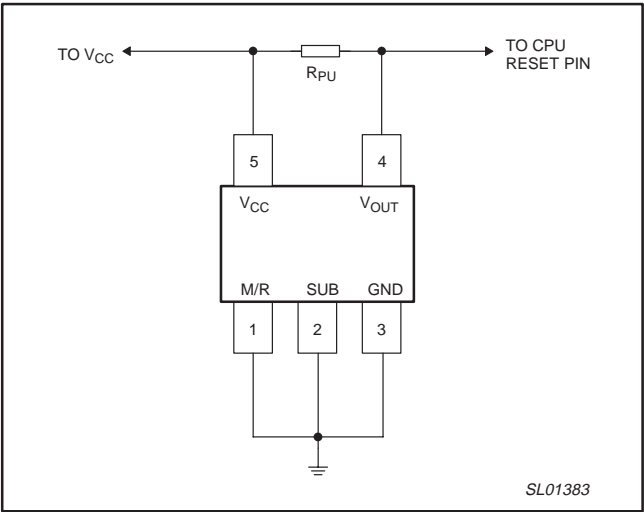


Figure 18. Typical hard reset circuit

Figure 19 shows a circuit with a manual reset switch. When the manual switch is closed,  $V_{OUT}$  reset is a low voltage state. Conversely, when it is opened,  $V_{OUT}$  reset is a HIGH voltage state. As a precaution, a clamp diode is placed from the M/R pin to ground to ensure that the pin does not go below  $-0.3$  V.

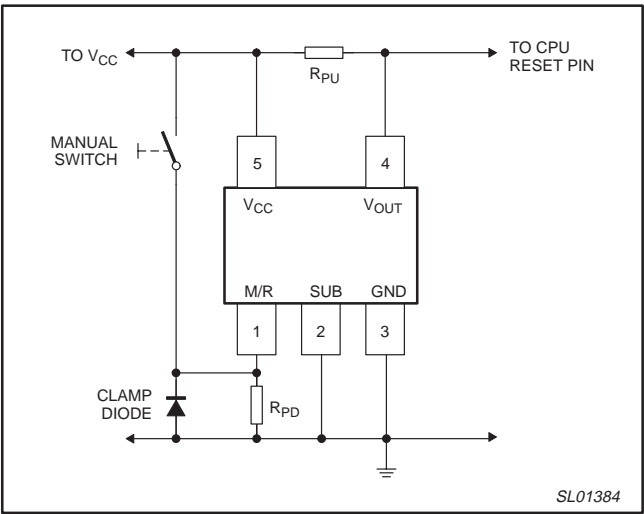


Figure 19. Manual Reset circuit

When a manual reset is used, it is suggested a resistor ( $R_{PU}$ ) be connected from the M/R pin to ground so as to provide a pull-down ground reference for the M/R pin when not in use. This will reduce the possibility of an induced erroneous voltage being imposed on the M/R pin. This can be a solution in noisy applications where the manual reset line is of considerable length and subject to picking up induced voltages. The M/R pin can be pulled to a HIGH voltage state whenever a manual reset is imposed. The only disadvantage to this is a small amount of additional current flow through the pull-down ground reference resistor when the M/R pin is pulled to a HIGH state.

## TEST CIRCUITS

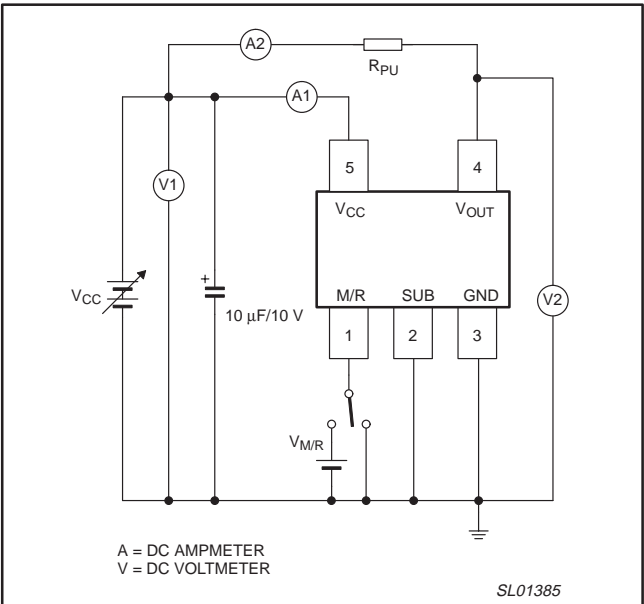


Figure 20. Test circuit 1

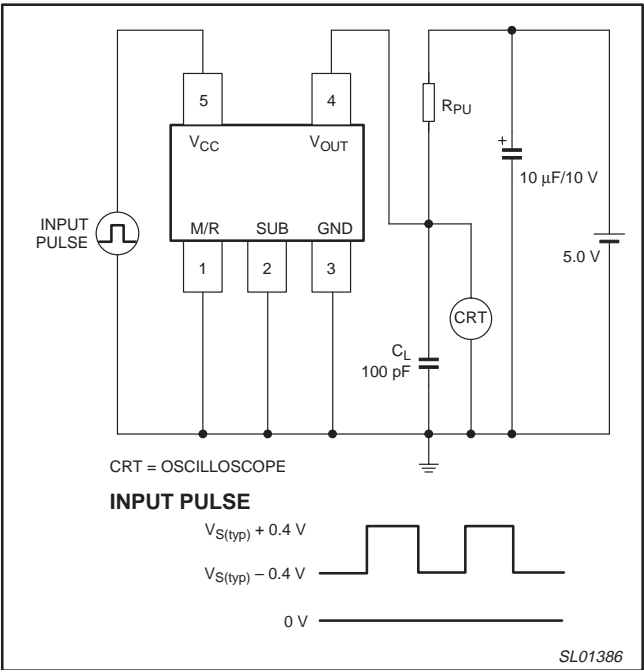


Figure 21. Test circuit 2

## System reset

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**PACKING METHOD**

The NE56610/11/12 is packed in reels, as shown in Figure 22.

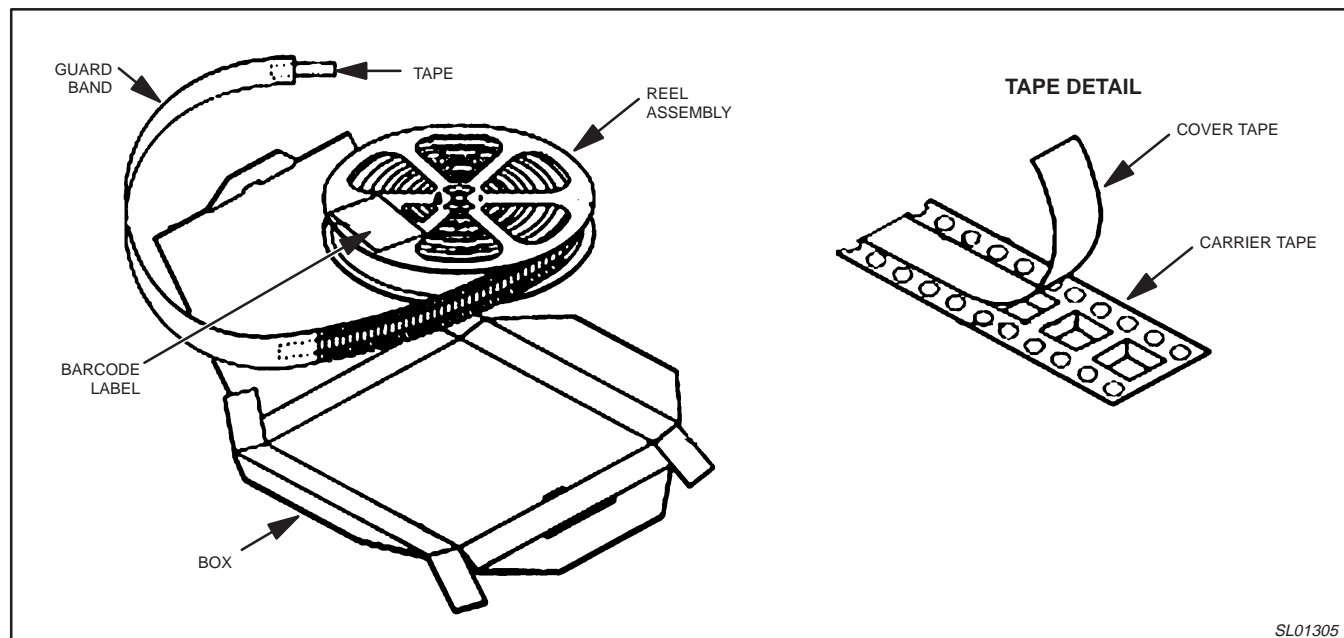
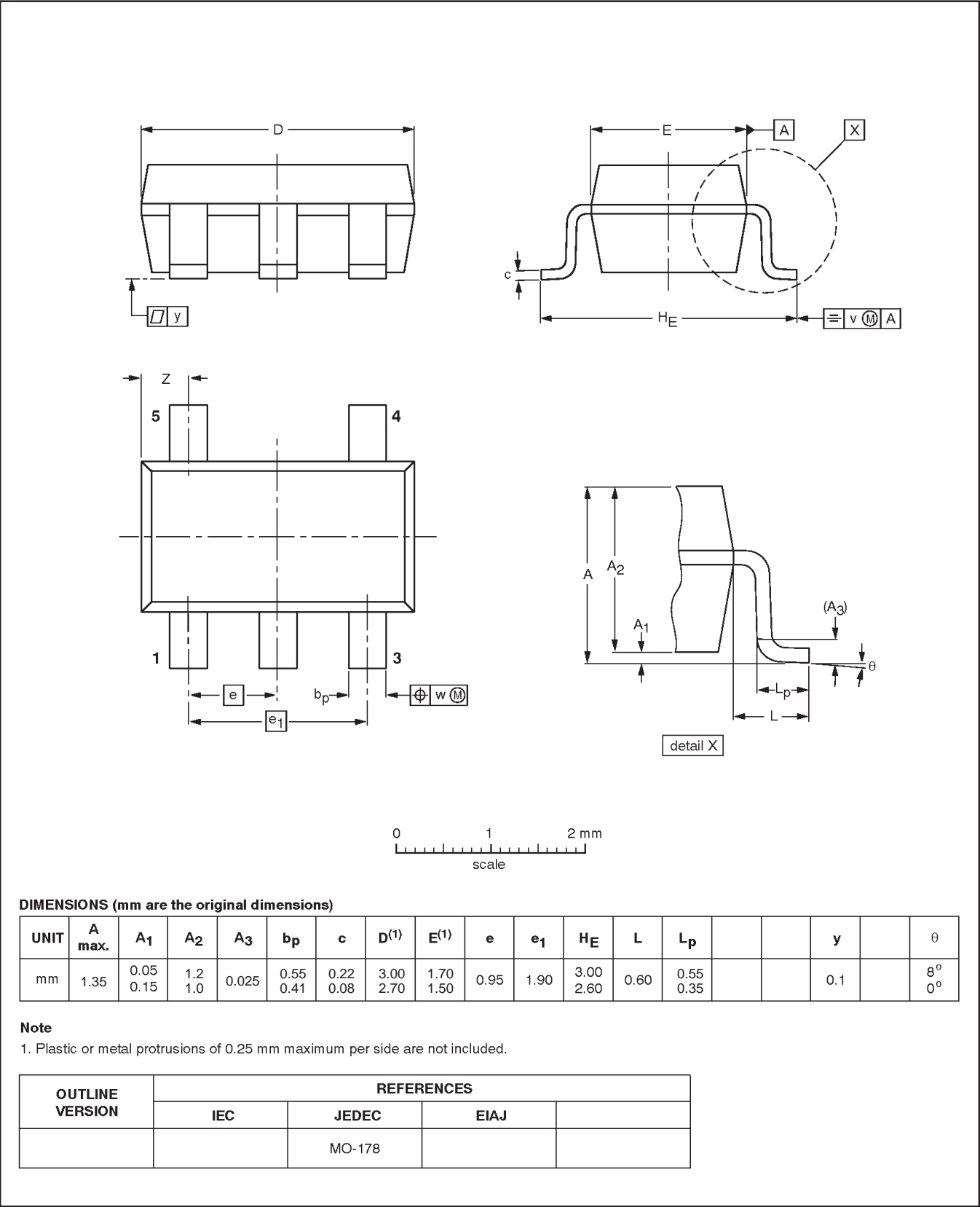


Figure 22. Tape and reel packing method

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SOT23-5: plastic small outline package; 5 leads; body width 1.5 mm



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**NOTES**

## System reset

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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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