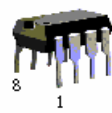


The PJ34063 Series is a monolithic control circuit containing the primary functions required for DC to DC onverters. These devices consist of an internal duty cycle oscillator with an active current limit circuit, drive and a high current output switch. This series was specifically designed to be incorporated in step-up, step-down and voltage-inverting applications with a minimum number of external components. temperature compensated reference,comparator,controlled.


FEATURES

- Operation from 3 to 40V input
- Low standby current
- Current limiting
- Output switch current to 1.5A
- Precision 2% reference
- Output - voltage adjustable
- Frequency of operation from 100Hz to 100KHz

DIP-8



SOP-8



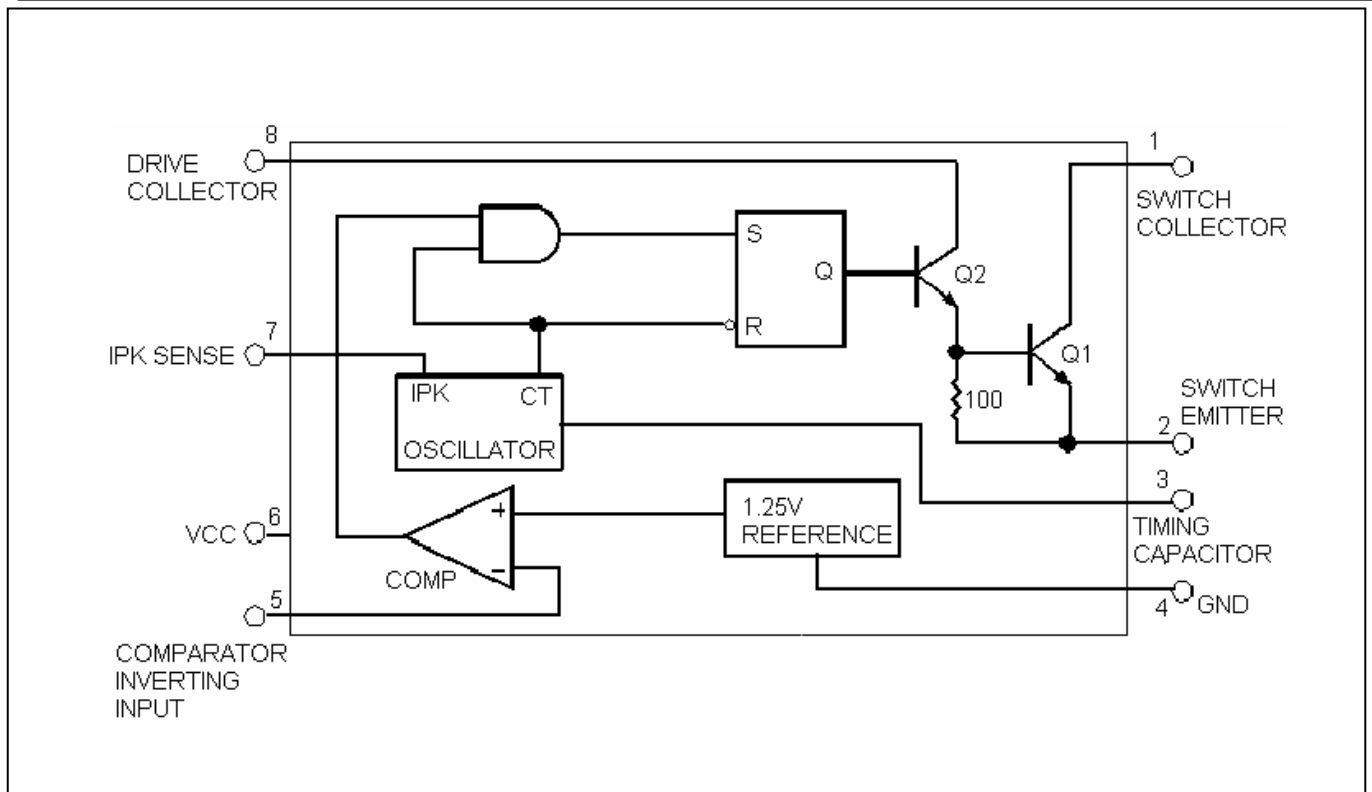
Pin : 1. Switch Collector
 3. Timing Capacitor
 5. Comparator Inverting Input
 7. IPK Sense

2. Switch Emitter
 4. Gnd
 6. Vcc
 8. Driver Collector

ORDERING INFORMATION

Device	Operating temperature (Ambient)	Package
PJ34063CD	-20°C ~ +85°C	DIP-8
PJ34063CS		SOP-8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 ~ +40	Vdc
Switch Collector Voltage	$V_{C(SW)}$	40	Vdc
Switch Emitter Voltage	$V_{E(SW)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(SW)}$	40	Vdc
Driver Collector Voltage	$V_{C(drive)}$	40	Vdc
Drive Collector Current (Note 1)	$I_{C(drive)}$	100	mA
Switch Current	I_{sw}	1.5	A
Operating Junction Temperature	T_J	0 to +125	°C
Operating Ambient Temperature Range	T_A	-20 to +85	°C
Storage Temperature Range	T_{stg}	-25 to +150	°C

ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0V$, $T_A = T_{low}$ to T_{high} , unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OSCILLATOR

Frequency	f_{osc}	$V_{PIN5}=0V$, $C_T=1.0nF$, $T_A=25^\circ C$	24	33	42	KHz
Charging Current	I_{chg}	$V_{CC}=5$ to $40V$, $T_A=25^\circ C$	24	35	42	μA
Discharge Current	I_{dischg}	$V_{CC}=5$ to $40V$, $T_A=25^\circ C$	140	220	260	μA
Discharge To Charge Current Ratio	I_{dischg}/I_{chg}	Pin7 to V_{CC} , $T_A=25^\circ C$	5.2	6.5	7.5	-
Current Limit Sense Voltage	$V_{IPK(sense)}$	$I_{chg} = I_{dischg}$, $T_A=25^\circ C$	250	300	350	mV

OUTPUT SWITCH(NOTE 2)

Saturation Voltage , Darlington Connection	$V_{CE(sat)}$	$I_{sw}=1.0A$, Pins1,8 connected	-	1.0	1.3	V
Saturation Voltage , Darlington Connection	$V_{CE(sat)}$	$I_{sw}=1.0A$, $R_{PIN8}=82\Omega$ to V_{cc} , Forced $\beta \leq 20$	-	0.45	0.7	V
DC Current Gain	h_{FE}	$I_{sw}=1.0A$, $V_{CE} = 5.0V$, $T_A=25^\circ C$	50	75	-	-
Collector Off- State Current	$I_{C(off)}$	$V_{CE} = 40V$	-	40	100	μA

COMPARATOR

Threshold Voltage	V_{TH}	$T_A=25^\circ C$	1.23	1.25	1.27	V
Threshold Voltage Line Regulation	Regline	$V_{CC} = 3$ to $40V$		1.4	5.0	mV
Input Bias Current	I_{IB}	$V_{IN}=0V$		-20	-400	nA

TOTAL DEVICE

Supply Current	I_{CC}	$V_{CC}=5$ to $40V$, $C_T=1.0nF$, Pin7= V_{cc} , $V_{PIN5}>V_{th}$ Pin 2 =GND, remaining pins open	-	-	4.0	mA
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Notes : 1.Maximum package power dissipation limits must be observed.

2.Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

FIGURE 1.OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

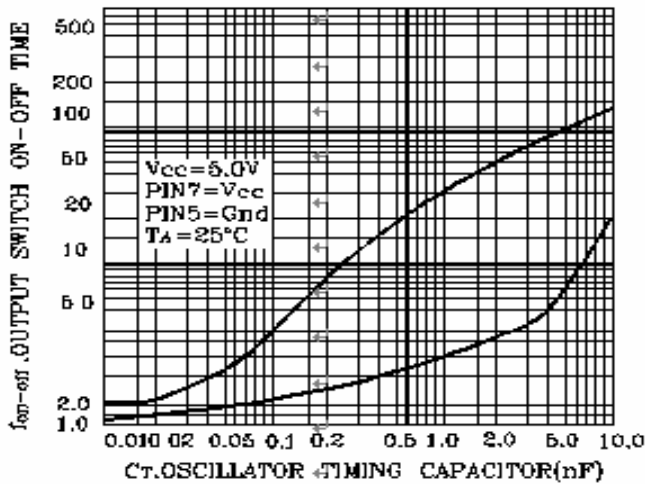


FIGURE 2.TIMING CAPACITOR WAVEFORM

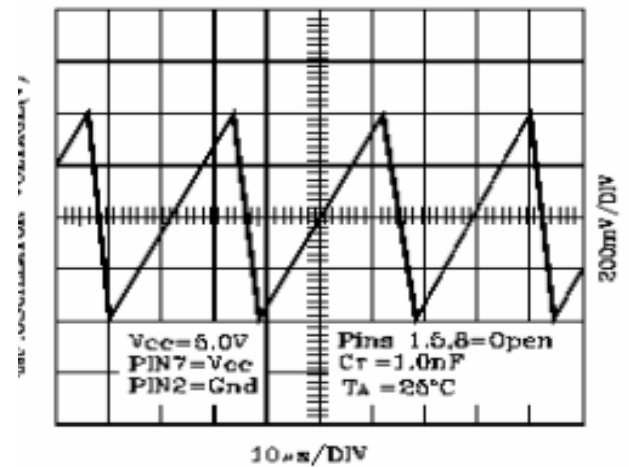


FIGURE 3.EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

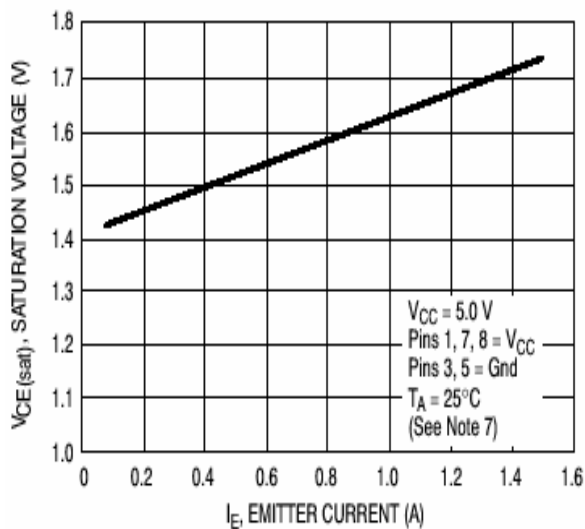


FIGURE 4.COMMON EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

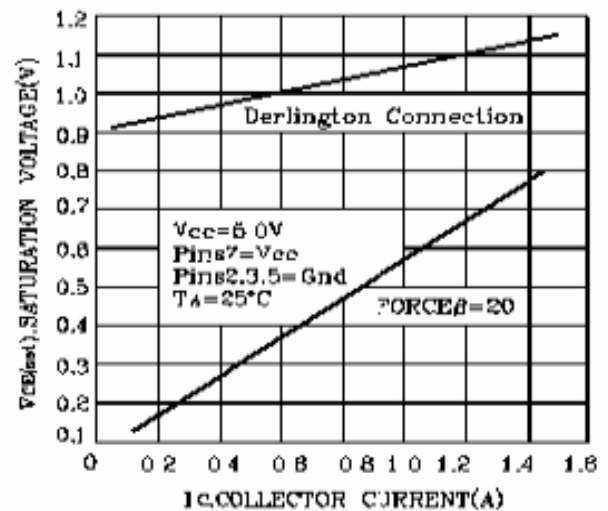


FIGURE 5.CURRENT LIMIT SENSE VOLTAGE versus TEMPERATURE

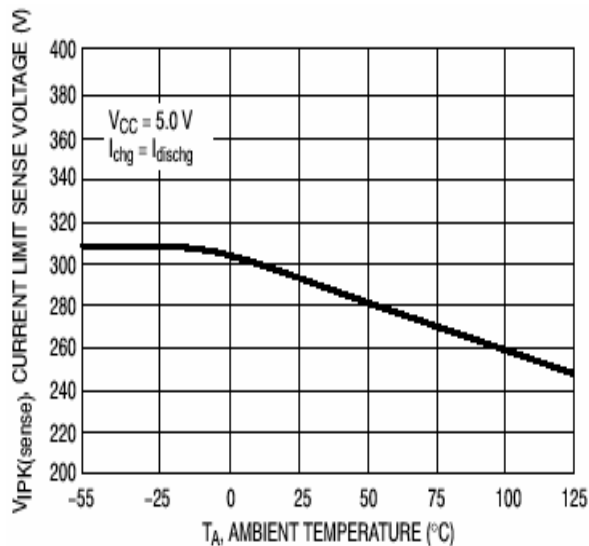
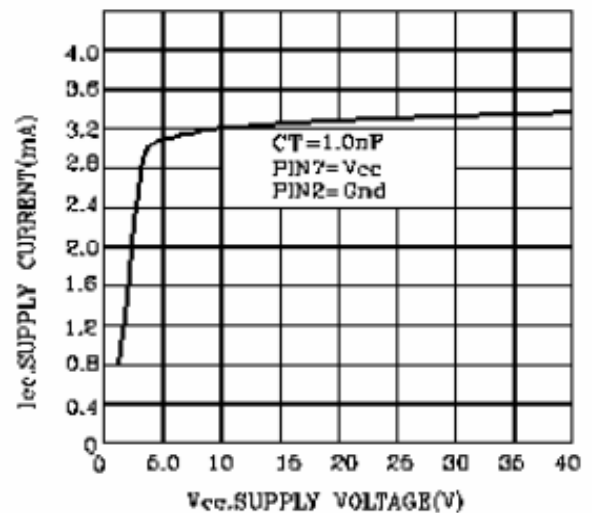
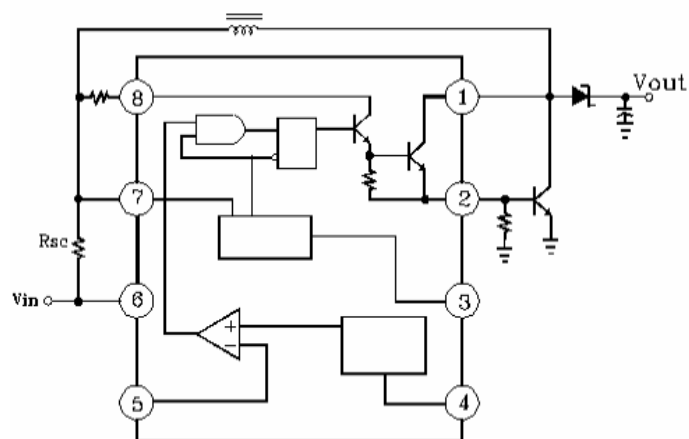


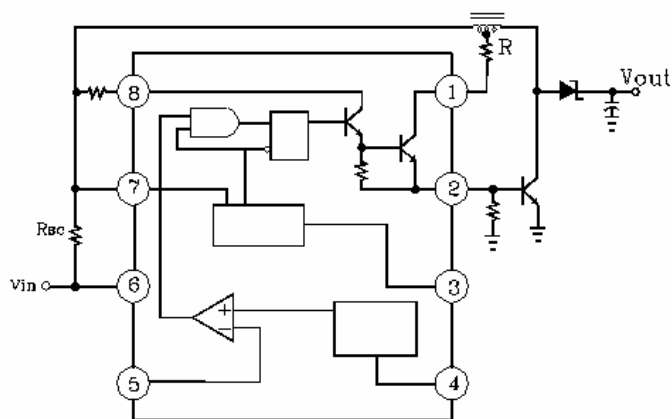
FIGURE 6.STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE



2a.EXTERNAL NPN SWITCH



2b.EXTERNAL NPN SATURATED SWITCH



2002.ver.A

FIGURE 3.STEP-DOWN CONVERTER

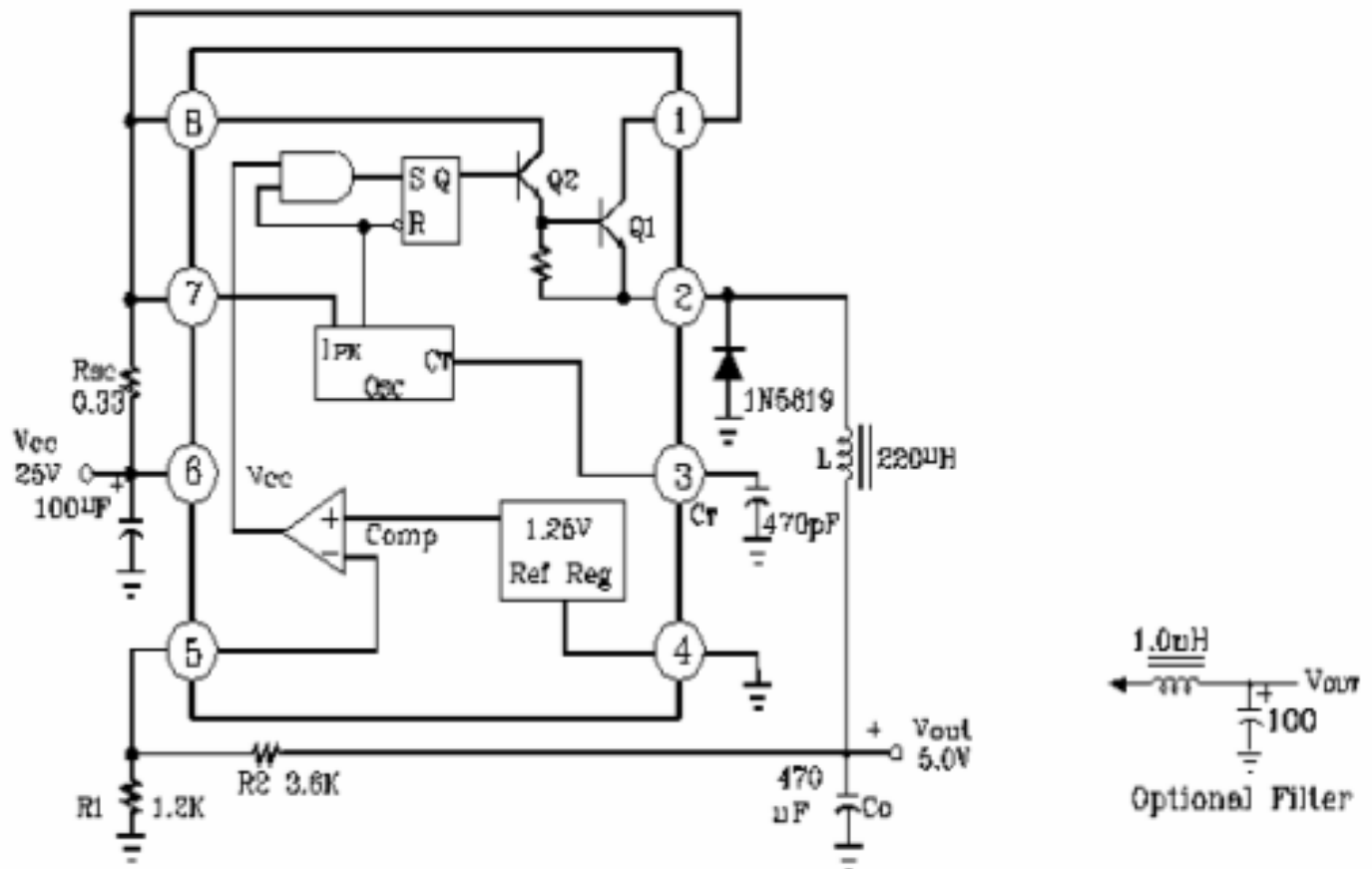
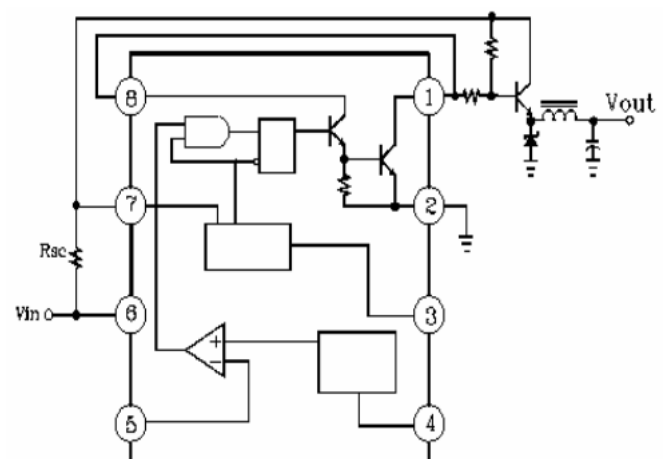
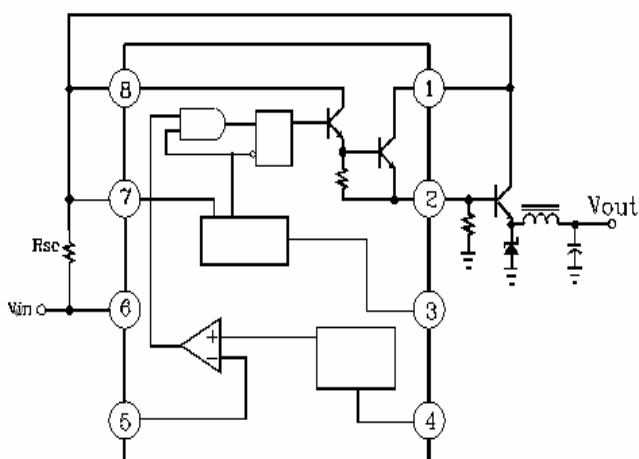


FIGURE 4.EXTERNAL CURRENT BOOST CONNECTIONS FOR I_c PEAK GREATER THAN 1.5A

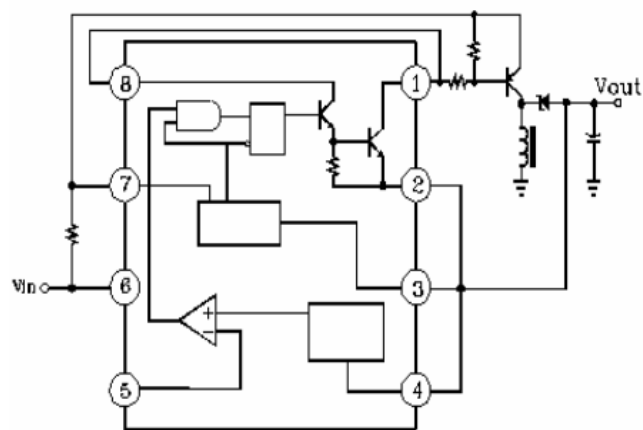
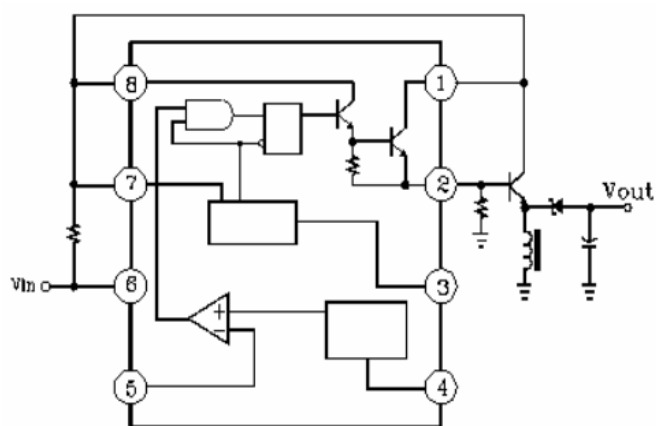
4a.EXTERNAL NPN SWITCH

4b.EXTERNAL NPN SWITCH



The circuit diagram shows a -12V regulator. The input is V_{cc} (4.5V to 6.0V) connected to pin 6 through a 100nF capacitor. Pin 8 is connected to the input through a 0.24 resistor. Pin 7 is connected to the input through a 0.24 resistor. Pin 5 is connected to ground through an 8.2K resistor. Pin 4 is connected to the output through a 1000 resistor. Pin 3 is connected to the output through a 1000 resistor. Pin 2 is connected to the output through a 1000 resistor. Pin 1 is connected to the output through a 1000 resistor. The output is V_{out} (-12V 100mA). The circuit includes a 1.25V reference regulator, a 1PK oscillator, a 1N5819 diode, and a 1000 resistor. An optional filter is shown with a 1.0uH inductor and a 100 capacitor.

6b.EXTERNAL NPN SATURATED SWITCH



DC-To-DC Converter Controller

Table : Design Formula

Calculation	Step-Up	Step-Down	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out}+V_F-V_{in(min)}}{V_{CC(min)}-V_{sat}}$	$\frac{V_{OUT}+V_F}{V_{CC}-V_{sat}-V_{OUT}}$	$\frac{ V_{out} +V_F}{V_{CC}+V_{sat}}$
$(t_{on}+t_{off}) \text{ max}$	$\frac{1}{f \text{ min}}$	$\frac{1}{f \text{ min}}$	$\frac{1}{f \text{ min}}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk}(\text{switch})$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$0.3/I_{pk}(\text{switch})$	$0.3/I_{pk}(\text{switch})$	$0.3/I_{pk}(\text{switch})$
$L \text{ (min)}$	$\left(\frac{V_{in(min)}-V_{sat}}{I_{pk}(\text{switch})} \right) t_{on(max)}$	$\left(\frac{V_{in(min)}-V_{sat}-V_{out}}{I_{pk}(\text{switch})} \right) t_{on(max)}$	$\left(\frac{V_{in(min)}-V_{sat}}{I_{pk}(\text{switch})} \right) t_{on(max)}$
C_o	$\left(\frac{I_{outon}}{V_{ripple(pp)}} \right)$	$\left(\frac{I_{pk}(\text{switch})(t_{on}+t_{off})}{8V_{ripple(pp)}} \right)$	$\left(\frac{I_{outon}}{V_{ripple(pp)}} \right)$

TERMS AND DEFINITIONS

- ◆ V_{sat} = Saturation Voltage of the output switch.
- ◆ V_F = Forward Voltage drop of the rectifier.

The following power supply characteristics must be chosen:

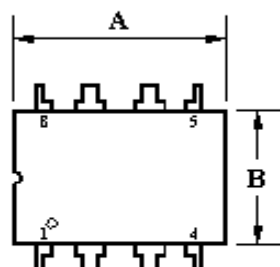
- ◆ V_{in} = Normal input voltage
- ◆ V_{out} : Desired Output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R_2}{R_1} \right)$
- ◆ I_{out} : Desired output current.
- ◆ f_{min} : Minimum desired output switching frequency at the selected values for V_{in} and I_o .
- ◆ $V_{ripple(p-p)}$: Desired peak-to-peak output ripple voltage. in practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout.

The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

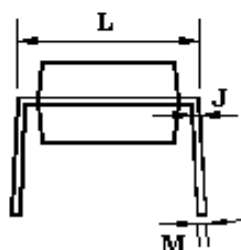
DIP-8 Mechanical drawing

DIP-8 Unit:mm

1. Top View



2. Side View

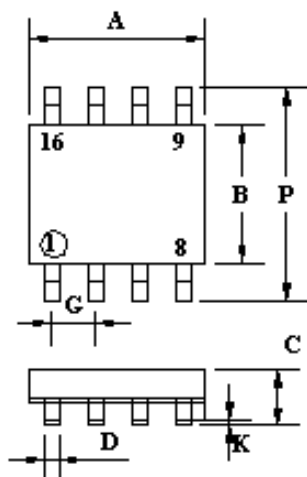


DIP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	8.75	0.357	0.367
B	6.22	4.00	0.245	0.255
C	3.18	1.75	0.125	0.135
D	0.35	0.49	0.019	0.020
G	2.54BSC		0.10BSC	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10°	-	10°

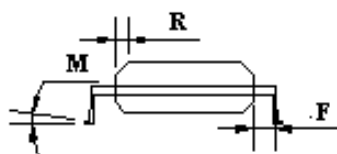
SOP-8 Mechanical drawing

SOP-8 Unit:mm

1. Top View



2. Side View



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019