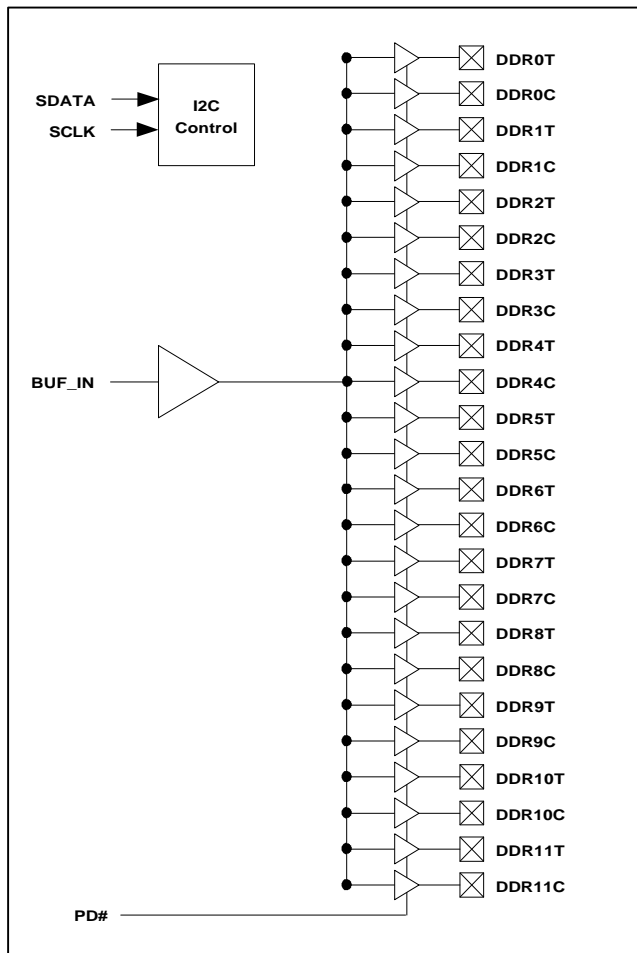


## DDR SDRAM Buffer for Desktop PCs with 4 DDR DIMMS

### FEATURES

- Generates 24 output buffer from one input.
- Supports up to four DDR DIMMS.
- Supports 266MHz DDR SDRAM.
- One additional output for feedback.
- Less than 5ns delay.
- Skew between any outputs is less than 100 ps.
- 2.5V Supply range.
- Enhanced DDR Output Drive selected by I2C.
- Available in 48 pin SSOP.

### BLOCK DIAGRAM



### PIN CONFIGURATION

FBOUT	1	48	N/C
VDD2.5	2	47	VDD2.5
GND	3	46	GND
DDR0T	4	45	DDR11T
DDR0C	5	44	DDR11C
DDR1T	6	43	DDR10T
DDR1C	7	42	DDR10C
VDD2.5	8	41	VDD2.5
GND	9	40	GND
DDR2T	10	39	DDR9T
DDR2C	11	38	DDR9C
VDD2.5	12	37	VDD2.5
BUF_IN	13	36	PD#
GND	14	35	GND
DDR3T	15	34	DDR8T
DDR3C	16	33	DDR8C
VDD2.5	17	32	VDD2.5
GND	18	31	GND
DDR4T	19	30	DDR7T
DDR4C	20	29	DDR7C
DDR5T	21	28	DDR6T
DDR5C	22	27	DDR6C
VDD2.5	23	26	GND
SDATA	24	25	SCLK

Note: #: Active Low

### DESCRIPTIONS

The PLL103-02 Rev.D is designed as a 2.5V buffer to distribute high-speed clocks in PC applications. The device has 24 outputs. These outputs can be configured to support four unbuffered DDR DIMMS. The PLL103-02 Rev.D can be used in conjunction with the PLL202-04 or similar clock synthesizer for the VIA Pro 266 chipset.

The PLL103-02 Rev.D also has an I2C interface, which can enable or disable each output clock. When power up, all output clocks are enabled (has internal pull up).

**DDR SDRAM Buffer for Desktop PCs with 4 DDR DIMMS****PIN DESCRIPTIONS**

Name	Number	Type	Description
FBOUT	1	O	Feedback clock for chipset.
BUF_IN	13	I	Reference input from chipset.
PD	36	I	Power Down Control input. When low, it will tri-state all outputs.
N/C	48		Not connected.
DDR[0:11]T	4,6,10,15,19, 21,28,30,34, 39,43,45	O	These outputs provide True copies of BUF_IN.
DDR[0:11]C	5,7,11,16,20, 22,27,29,33, 38,42,44	O	These outputs provide complementary copies of BUF_IN.
VDD2.5	2,8,12,17,23, 32,37,41,47	P	2.5V power supply.
GND	3,9,14,18,26, 31,35,40,46	P	Ground.

**DDR SDRAM Buffer for Desktop PCs with 4 DDR DIMMS**

**I2C BUS CONFIGURATION SETTING**

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	—
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	<p>This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).</p> <p>Following the acknowledge of this address byte, in <b>Write Mode</b>: the <b>Command Byte</b> and <b>Byte Count Byte</b> must be sent by the master but ignored by the slave, in <b>Read Mode</b>: the <b>Byte Count Byte</b> will be read by the master then all other <b>Data Byte</b>. <b>Byte Count Byte</b> default at power-up is = (0x09).</p>							

**I2C CONTROL REGISTERS**

**1. BYTE 6: Outputs Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	48	1	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Enhanced DDR Drive. 1 = Enhanced 25%
Bit 4	-	0	Reserved
Bit 3	45, 44	1	DDR11T, DDR11C
Bit 2	43, 42	1	DDR10T, DDR10C
Bit 1	39, 38	1	DDR9T, DDR9C
Bit 0	34, 33	1	DDR8T, DDR8C

**DDR SDRAM Buffer for Desktop PCs with 4 DDR DIMMS****2. BYTE 7: Outputs Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	30, 29	1	DDR7T, DDR7C
Bit 6	28, 27	1	DDR6T, DDR6C
Bit 5	21, 22	1	DDR5T, DDR5C
Bit 4	19, 20	1	DDR4T, DDR4C
Bit 3	15, 16	1	DDR3T, DDR3C
Bit 2	10, 11	1	DDR2T, DDR2C
Bit 1	6, 7	1	DDR1T, DDR1C
Bit 0	4, 5	1	DDR0T, DDR0C

**DDR SDRAM Buffer for Desktop PCs with 4 DDR DIMMS**

**ELECTRICAL SPECIFICATIONS**

**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$	$V_{SS}-0.5$	7.0	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature	$T_A$	0	70	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

**2. Operating Conditions**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD2.5}$	2.375	2.625	V
Input Capacitance	$C_{IN}$		5	pF
Output Capacitance	$C_{OUT}$		6	pF

**3. Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	$V_{IH}$	All Inputs except I2C	2.0		$V_{DD}+0.3$	V
Input Low Voltage	$V_{IL}$	All inputs except I2C	$V_{SS}-0.3$		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$			TBM	μA
Input Low Current	$I_{IL}$	$V_{IN} = 0$			TBM	μA
Output High Voltage	$V_{OH}$	$I_{OL} = -12mA$ , $V_{DD} = 2.375V$	1.7			V
Output Low Voltage	$V_{OL}$	$I_{OL} = 12mA$ , $V_{DD} = 2.375V$			0.6	V
Output High Current	$I_{OH}$	$V_{DD} = 2.375V$ , $V_{OUT}=1V$	-18	-32		mA
Output Low Current	$I_{OL}$	$V_{DD} = 2.375V$ , $V_{OUT}=1.2V$	26	35		mA

**Note:** TBM: To be measured

**DDR SDRAM Buffer for Desktop PCs with 4 DDR DIMMS**

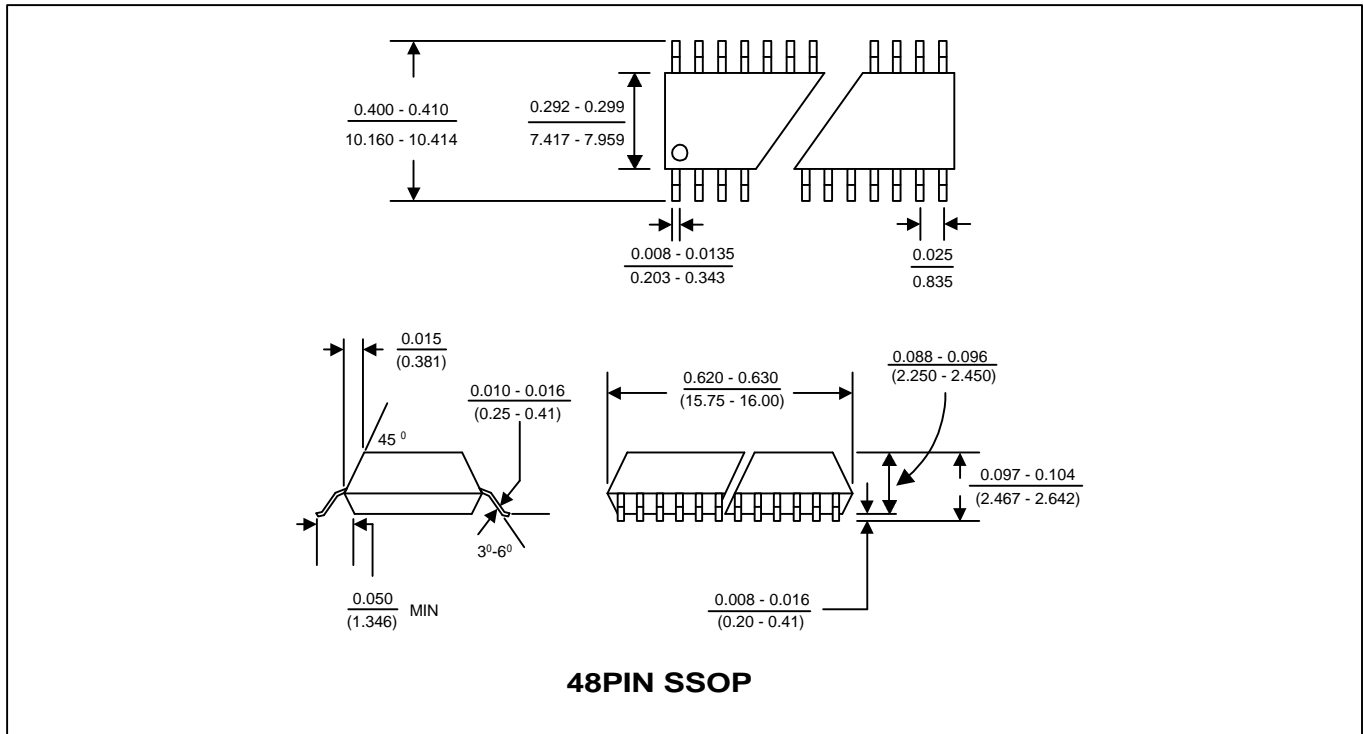
**3. Electrical Specifications (Continued)**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I <sub>DDs</sub>	PD = 0			TBM	mA
Output Crossing Voltage	V <sub>OC</sub>		(V <sub>DD</sub> /2) - 0.1	V <sub>DD</sub> /2	(V <sub>DD</sub> /2) + 0.1	V
Output Voltage Swing	V <sub>OUT</sub>		1.1		V <sub>DD</sub> -0.4	V
Duty Cycle	D <sub>T</sub>	Measured @ 1.5V	45	50	55	%
Max. Operating Frequency			66		170	MHz
Rising Edge Rate	T <sub>OR</sub>	Measured @ 0.4V ~ 2.4V	1.0	1.5	2.0	V/ns
Falling Edge Rate	T <sub>OF</sub>	Measured @ 2.4V ~ 0.4V	1.0	1.5	2.0	V/ns
Clock Skew ( pin to pin )	T <sub>SKEW</sub>	All outputs equally loaded			100	ps
Stabilization Time	T <sub>ST</sub>				0.1	ms

**Note:** TBM: To be measured

**DDR SDRAM Buffer for Desktop PCs with 4 DDR DIMMS**

**PACKAGE INFORMATION**



**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range

**PLL103-02 X C**

PART NUMBER

TEMPERATURATURE  
C=COMMERCIAL  
M=MILITARY  
I=INDUSTRIAL  
PACKAGE TYPE  
X=SSOP

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