

High-Performance Surface-Mount TTL Delay Lines

CTTLDL,
BJTTLDL,
GBTTLDL,
BTTLDL

- Five equal taps in 20% increments of total delay.
- Lumped constant, active series.
- Transfer-molded packaging for highest reliability.
- Designed for leading edge timing. Trailing edge timing available.
- Supports Schottky TTL, FAST, and FACT logics.
- Fanout 1 -- 20 loads; logic 0 -- 10 loads.
- Temperature coefficient ± 2 ns or $\pm 4\%$ (whichever is greater) at maximum delay, 0 to 70°C.
- Military models with temperature range -55 to +125°C and ceramic package IC to meet MIL-STD-883C, but not screened to that specification, add suffix "M" to part number.
- Military models as above, but with ceramic package IC screened to MIL-STD 883C and 38510, add suffix "MX" to part number.
- Military models as "MX" above, but with in-house burn-in and thermal shock, add suffix "MY".

LOW PROFILE SURFACE-MOUNT 5-TAP TTL DELAY LINES

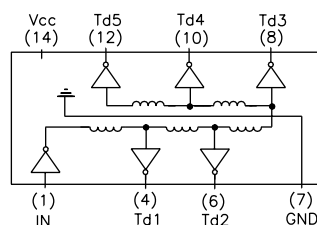
| TECHNITROL PART NO. | TAP DELAYS (ns) | | | | | ALL TAPS | |
|------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| | T _{D1} | T _{D2} | T _{D3} | T _{D4} | T _{D5} | T _{RO} | T _{FO} |
| CTTLDL025 | 5.0 | 10.0 | 15.0 | 20.0 | 25.0 | 2.0 | 2.0 |
| CTTLDL050 | 10.0 | 20.0 | 30.0 | 40.0 | 50.0 | 2.0 | 2.0 |
| CTTLDL075 | 15.0 | 30.0 | 45.0 | 60.0 | 75.0 | 2.0 | 2.0 |
| CTTLDL100 | 20.0 | 40.0 | 60.0 | 80.0 | 100.0 | 2.0 | 5.0 |
| CTTLDL125 | 25.0 | 50.0 | 75.0 | 100.0 | 125.0 | 2.0 | 5.0 |
| CTTLDL150 | 30.0 | 60.0 | 90.0 | 120.0 | 150.0 | 2.0 | 6.0 |
| CTTLDL200 | 40.0 | 80.0 | 120.0 | 160.0 | 200.0 | 2.0 | 7.0 |

0.175"
MAX
HEIGHT

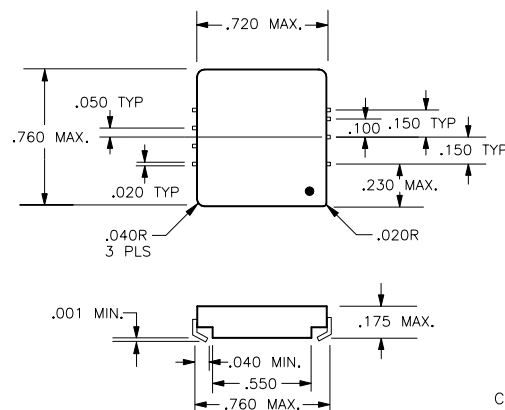
For TTL delay lines qualified to MIL-D-83532, refer to PSC information sheet entitled "QPL Active Delay Lines."

Delay Characteristics measured at $V_{CC} = 5.0V$, 25°C, no load.
Delay Tolerance ± 2 ns or 5%, whichever is greater.
Rise time measured @ 0.8V to 2.0V levels.
For minimum input pulse width -- contact factory.

SCHEMATIC



MECHANICAL OUTLINE



CTTLDL-19

Notes

- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.



CTTDL,
BJTTDL,
GBTTDL,
BTTLDL

SURFACE-MOUNT 5-TAP TTL DELAY LINES -- 1/2" SQ.

| TECHNITROL PART NO. | PART NO. | PART NO. | TAP DELAYS (ns) | | | | | ALL TAPS (Max.) | |
|------------------------|-----------|-----------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|-----------------|
| | | | T _{D1} | T _{D2} | T _{D3} | T _{D4} | T _{D5} | T _{RO} | T _{FO} |
| BJTTDL025 | GBTTDL025 | BTTLDL025 | 5.0 | 10.0 | 15.0 | 20.0 | 25.0 | 2.0 | 2.0 |
| BJTTDL050 | GBTTDL050 | BTTLDL050 | 10.0 | 20.0 | 30.0 | 40.0 | 50.0 | 2.0 | 2.0 |
| BJTTDL075 | GBTTDL075 | BTTLDL075 | 15.0 | 30.0 | 45.0 | 60.0 | 75.0 | 2.0 | 2.0 |
| BJTTDL100 | GBTTDL100 | BTTLDL100 | 20.0 | 40.0 | 60.0 | 80.0 | 100.0 | 2.0 | 5.0 |
| BJTTDL125 | GBTTDL125 | BTTLDL125 | 25.0 | 50.0 | 75.0 | 100.0 | 125.0 | 2.0 | 6.0 |
| BJTTDL150 | GBTTDL150 | BTTLDL150 | 30.0 | 60.0 | 90.0 | 120.0 | 150.0 | 2.0 | 7.0 |
| BJTTDL200 | GBTTDL200 | BTTLDL200 | 40.0 | 80.0 | 120.0 | 160.0 | 200.0 | 2.0 | 8.0 |

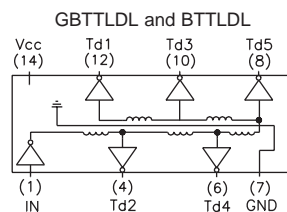
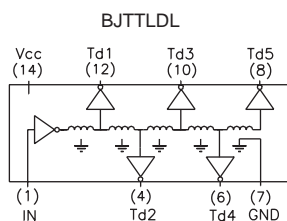
Delay Characteristics measured at $V_{CC} = 5.0V$, $25^{\circ}C$, no load.

Delay Tolerance ± 2 ns or 5%, whichever is greater.

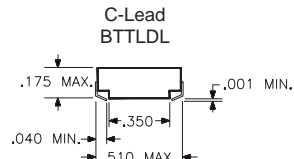
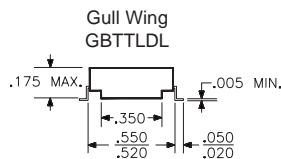
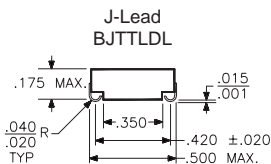
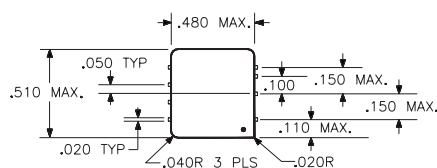
Rise time measured @ 0.8V to 2.0V levels.

For minimum input pulse width -- contact factory.

SCHEMATICS



MECHANICAL OUTLINES



BJ-19

Notes

- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.