

P4C1024 MILITARY HIGH SPEED 128K x 8 CMOS STATIC RAM

ADVANCE INFORMATION



FEATURES

- High Speed (Equal Access and Cycle Times)
— 20/25/35/45/55/70 ns
- Single 5 Volts $\pm 10\%$ Power Supply
- Easy Memory Expansion Using \overline{CE}_1 , CE_2 and \overline{OE} Inputs
- Common Data I/O
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Fast t_{OE}
- Automatic Power Down
- Packages
 - 32-Pin 400 mil and 600 mil Ceramic DIP
 - 32-Pin CERPACK
 - 32-Pin LCC



DESCRIPTION

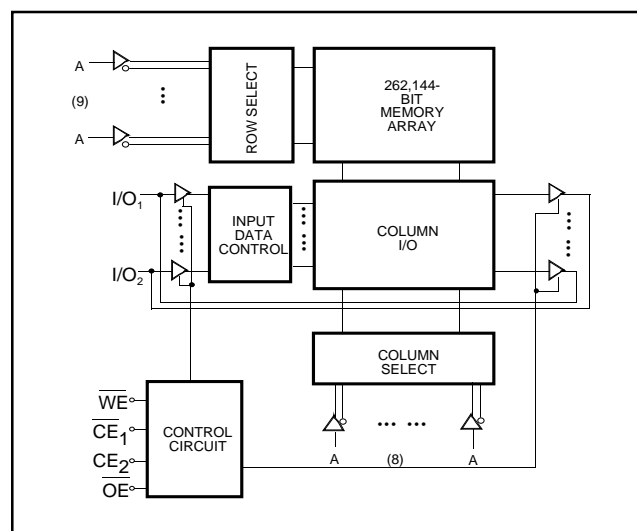
The P4C1024 is a 1,048,576-bit high-speed CMOS static RAM organized as 128Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V $\pm 10\%$ tolerance power supply.

Access times of 20 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1024 is a member of a family of PACE RAM™ products offering fast access times.

The P4C1024 device provides asynchronous operations with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{16} . Reading is accomplished by device selection (\overline{CE}_1 low and CE_2 high) and output enabling (\overline{OE}) while write enable (\overline{WE}) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either \overline{CE}_1 or \overline{OE} is HIGH or \overline{WE} or CE_2 is LOW.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

