

CLDP SERIES: CLOCK OSCILLATOR, LVDS, +2.5 VDC, 7x5mm Package

DESCRIPTION: A crystal controlled, high frequency, highly stable oscillator, adhering to Low Voltage Differential Signaling (LVDS) Standards. The output can be Tri-stated to facilitate testing or combined multiple clocks. The device is contained in a sub-miniature, very low profile, leadless ceramic SMD package with 6 gold contact pads. This miniature oscillator is ideal for today's automated assembly environments.

APPLICATIONS AND FEATURES:

- Infiniband; 10GbE; Network Processors; SOHO Routing; Switches; WAN Interfaces
- Common Frequencies: 106.25 MHz; 125 MHz; 150 MHz; 155.52 MHz; 156.25 MHz; 161.1328 MHz
- +2.5 VDC LVDS
- Frequency Range from 80 to 250 MHz
- Miniature Ceramic SMD Package Available on Tape and Reel
- Lead Free

■ ELECTRICAL PARAMETERS:

PARAMETER	SYMBOL	TEST CONDITIONS ^{*1}	VALUE	UNIT
Nominal Frequency	f _o		80.000 ~ 250.000	MHz
Supply Voltage	V _{cc}		+2.5 ±5%	VDC
Supply Current	I _s		60.0 MAX	mA
Output Logic Type			LVDS	
Load		Connected between OUTPUT and COMP. OUTPUT	100	Ω
Output Voltage Levels	V _{oh} V _{ol}		1.43 TYP; 1.60 MAX 0.90 MIN; 1.10 TYP	VDC VDC
Duty Cycle	DC	Measured at 50% of V _{cc}	40/60 to 60/40 or 45/55 to 55/45	%
Rise / Fall Time	t _r / t _f	Measured at 20/80% and 80/20% V _{cc} Levels	1.0 TYP ^{*2}	ns
Jitter	J	RMS, F _j = 12 kHz...20 MHz	1 TYP	ps
Overall Frequency Stability	Δf/f _c	Op. Temp., Aging, Load, Supply and Cal. Variations	±25, ±50, or ±100 MAX ^{*3}	ppm
Pin 1 Output Enabled Output Disabled	E _n D _{is}	High Voltage or No Connect Ground	0.7•V _{cc} MIN 0.3•V _{cc} MAX	VDC VDC
Absolute voltage range	V _{cc} (abs)	Non-Destructive	-0.5...+7.0	VDC

*1 Test Conditions Unless Stated Otherwise: Nominal V_{cc}, Nominal Load, +25 ±3°C

*2 Frequency Dependent

*3 Not All Stabilities Available With All Temperature Ranges—Consult Factory For Availability

■ ENVIRONMENTAL PARAMETERS:

PARAMETER	SYMBOL	TEST CONDITIONS ^{*1}	VALUE	UNIT
Operating temperature range	T _a		SEE PART NUMBER TABLE	°C
Storage temperature range	T(stg)		-55...+90	°C

■ PART NUMBERING SYSTEM:

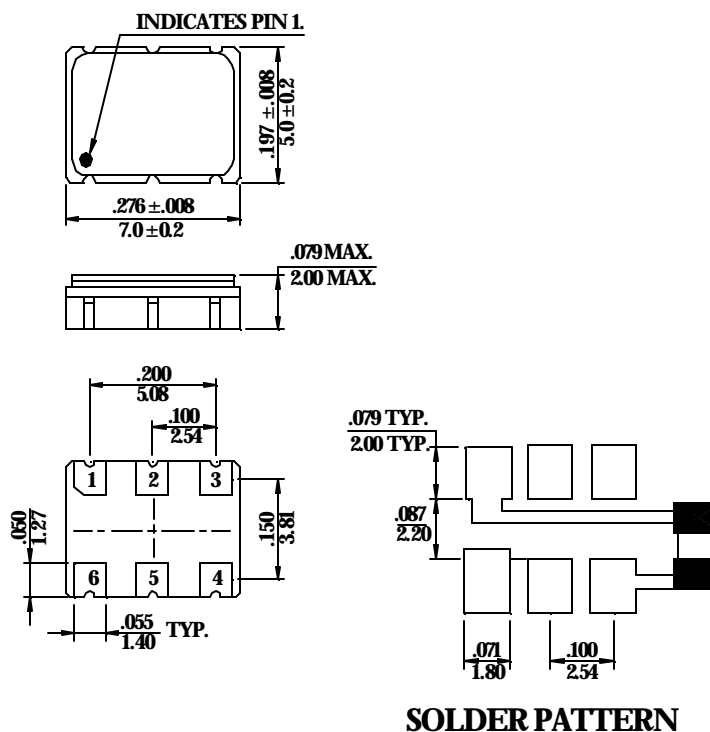
SERIES	SYMMETRY	TEMPERATURE RANGE (°C)	FREQUENCY STABILITY (Overall)	FREQUENCY (MHz)
CLDP: Clock with LVDS Comp. Output	A: 40/60 to 60/40% T: 45/55 to 55/45%	R: 0...+50 S: 0...+70 U: -20...+70 V: -40...+85	I: ±25 ppm H: ±50 ppm J: ±100 ppm	80.000...250.000

EXAMPLE: CLDPASH-155.520

Clock Oscillator, 7x5mm Package, +2.5 VDC Supply Voltage, LVDS Output, 40/60% Symmetry, 0...+70°C Operating Temperature Range, ±50 ppm Total Frequency Stability, 155.520 MHz

Consult the factory for any custom requirements.

■ **MECHANICAL PARAMETERS:**



***0.01mF external by-pass filter is recommended as shown on solder pattern.**

OUTLINE TOLERANCE:

±0.006" / 0.15mm

(Unless otherwise specified)

PIN FUNCTIONS:

- [1] ENABLE/ DISABLE
- [2] NO CONNECT
- [3] CASE GROUND
- [4] OUTPUT
- [5] COMP. OUTPUT
- [6] SUPPLY VOLTAGE

TYP. MARKING:

CLDPASH

155.52

RAL D/C