

CS9L/CSPL SERIES: ULTRA HF CLOCK OSCILLATOR, PECL, +3.3 VDC or +2.5VDC

DESCRIPTION: A crystal controlled, high frequency, highly stable oscillator, adhering to Positive Emitter Coupled Logic (PECL) Standards and fundamental crystal or analog multiplication technologies. The output can be Tri-stated to facilitate testing or combined multiple clocks. The device is contained in a sub-miniature, very low profile, leadless ceramic SMD package with 6 gold contact pads. This miniature oscillator is ideal for today's automated assembly environments.

APPLICATIONS AND FEATURES:

- Infiniband; Fiber Channel; SATA; 10GbE; Network Processors; SOHO Routing; Switches;
- Common Frequencies: 150 MHz; 156.25 MHz; 155.52 MHz; 161.1328 MHz; 212.5MHz; 312.5MHz
- +3.3 VDC or +2.5VDC PECL
- Frequency Range from 150.000 to 700 MHz
- Analog multiplication
- Miniature Ceramic SMD Package Available on Tape and Reel
- Lead Free and ROHS Compliant

■ ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
Operating temperature range	Ta	-40...+85	°C
Storage temperature range	T(stg)	-55...+90	°C
Supply voltage	Vcc	+4.6	VDC
Maximum Input Voltage	Vi	Vss-0.5...Vcc+0.5	VDC
Maximum Output Voltage	Vo	Vss-0.5...Vcc+0.5	VDC

■ ELECTRICAL PARAMETERS:

PARAMETER	SYMBOL	TEST CONDITIONS ^{*1}		VALUE	UNIT
Nominal Frequency	f _o			150.000 ~ 700.00**	MHz
Supply Voltage	V _{cc}			+3.3 or +2.5 ±5%	VDC
Supply Current	I _s			80.0 MAX	mA
Output Logic Type				PECL	
Load		Connected between each output and V _{cc} – 2.0 VDC		50	Ω
Output Voltage Levels	V _{oh} V _{ol}	min max		V _{cc} -1.025 V _{cc} -1.620	VDC VDC
Duty Cycle	DC	Measured at 50% of V _{cc}		40/60 to 60/40 or 45/55 to 55/45	%
Rise / Fall Time	t _r / t _f	Measured at 20/80% and 80/20% V _{cc} Levels		0.7 TYP 1.0 MAX ^{*2}	ns
Jitter	J	Integrated Phase t _{ji} RMS, F _j = 12 kHz...20 MHz ⁵		0.3 TYP**	ps
		Integrated Phase RMS t _{ii} offset frequency 50KHz to 80MHz ⁵		0.5 TYP**	ps
		Deterministic period Jitter D _j using wavecrest analyzer ⁴	F _o <320MHz.	1 TYP **	ps
			F _o >320MHz.	8 TYP **	
		Random period Jitter R _j using wavecrest analyzer ⁴	F _o <320MHz.	2.5 TYP **	ps
			F _o >320MHz.	2.5 TYP**	
Acumm. Peak to Peak Jitter T _{p-p} using wavecrest analyzer ⁴	F _o <320MHz.	25 TYP**	ps		
	F _o >320MHz.	27 TYP**			
Phase Noise	£(Δf)	typ. @212.5MHz ⁶	Δf=10 Hz Δf=100 Hz Δf=1 KHz Δf=10 KHz Δf=100 KHz Δf≥1M Hz	-65 -95 -125 -140 -145 -148	dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Sub Harmonics	f _{sub}	Load, nom, Supply nom	F _o <320MHz. F _o >320MHz.	-50 -35	dBc
Overall Frequency Stability	Δf/f _c	Op. Temp., Aging, Load, Supply and Cal. Variations		±20, ±25, ±50, or ±100 MAX ^{*3}	ppm
Pin 1 Output Enabled Output Disabled	En Dis	High Voltage or No Connect Ground		0.7•V _{cc} MIN 0.3•V _{cc} MAX	VDC VDC

*1 Test Conditions Unless Stated Otherwise: Nominal Vcc, Nominal Load, +25 ±3°C

*2 Frequency Dependent

*3 Not All Stabilities Available With All Temperature Ranges—Please Consult Factory For Availability

*4 Measured with Wavcrest SIA-3000A 1,000,000 Hits no filtering

*5 Calculated from Agilent 5500 phase noise measurements

*6 Measured with Agilent 5500

■ PART NUMBERING SYSTEM:

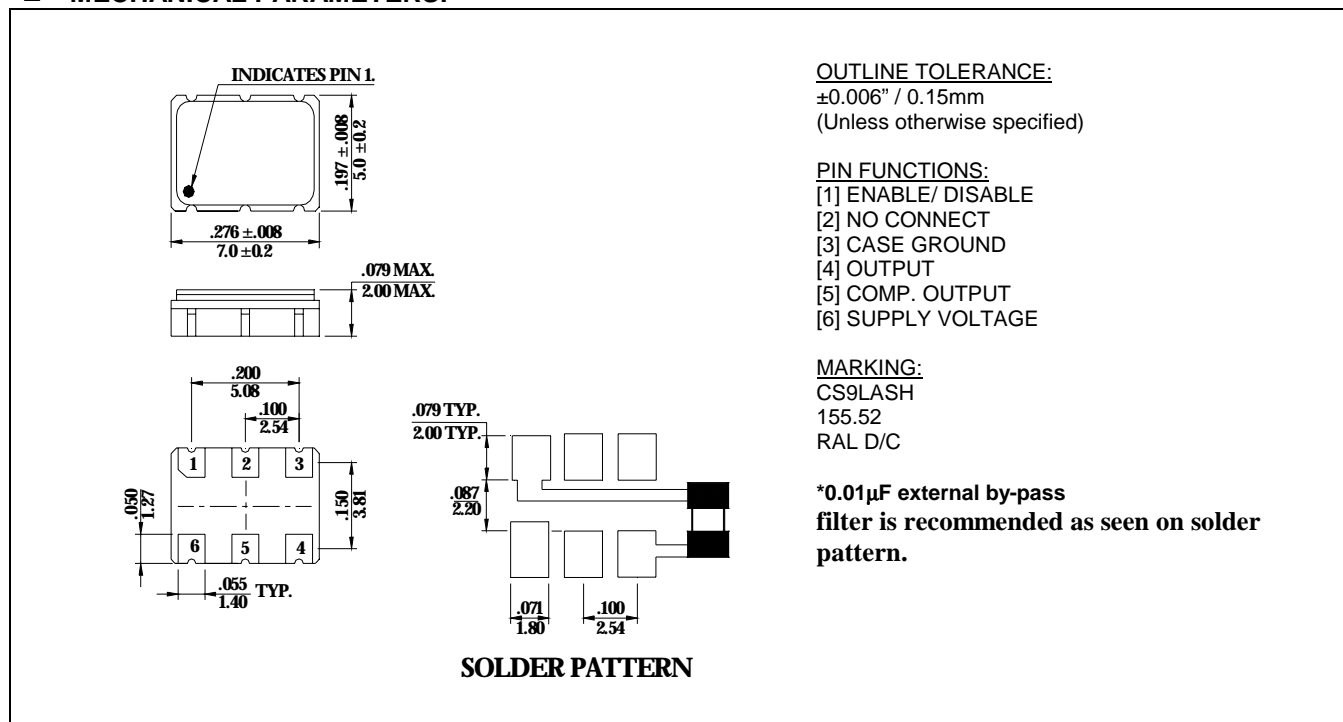
SERIES	SYMMETRY	TEMPERATURE RANGE (°C)	FREQUENCY STABILITY (Overall)	FREQUENCY (MHz)
CS9L: UHF +3.3Vdc Clock with PECL Comp. Output CSPL: UHF +2.5Vdc Clock with PECL Comp. Output	A: 40/60 to 60/40% T: 45/55 to 55/45%	R: 0...+50 S: 0...+70 U: -20...+70 V: -40...+85**	K: ±20 ppm** L: ±25 ppm** H: ±50 ppm J: ±100 ppm	150.000...700.000

EXAMPLE: CS9LASH-155.520

Clock Oscillator, 7x5mm Package, +3.3 VDC Supply Voltage, PECL Output, Standard Symmetry, 0...+70°C Operating Temperature Range, ±50 ppm Total Frequency Stability, 155.520 MHz

**Above 300MHz extended temp range and ±25ppm stability may not be available, jitter may vary upon spec requirements. Please consult the factory for any custom requirements.

■ MECHANICAL PARAMETERS:



■ **REFLOW PROFILE:**